



SPECIFICATION



ED312TT3

31.2"

Version: 1.0

Date: 14.11.2018

Note: This specification is subject to change without prior notice

www.data-modul.com

Version: 1.0

TECHNICAL SPECIFICATION

MODEL NO: ED312TT3

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

Customer's Confirmation

Customer _____

Date _____

By _____

E Ink's Confirmation

Approve by Man Chih

Confirm by Winyang Lee

Prepare by Han Wang

Revision History

Rev.	Issued Date	Revised Contents
1.0	2018/11/14	• 1 st formal version.

TECHNICAL SPECIFICATION

CONTENTS

<i>NO.</i>	<i>ITEM</i>	<i>PAGE</i>
-	Cover	1
-	Revision History	2
-	Contents	3
1	General Description	4
2	Features	4
3	Mechanical Specifications	4
4	Mechanical Drawing of EPD module	5
5	Input/Output Terminals	7
6	Electrical Characteristics	12
7	Power on Sequence	19
8	Optical Characteristics	21
9	Handling, Safety and Environment Requirements and Remark	22
10	Reliability Test	24
11	Block Diagram	25
12	Packing	26
13	Bar Code Definition	29

1. General Description

ED312TT3 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 31.2” active area with 2560 x 1440 pixels and 16:9 aspect ratios. The display is capable to display images at 2 to 16 gray levels (1 to 4 bits) depending on the display controller and the associated waveform file it used.

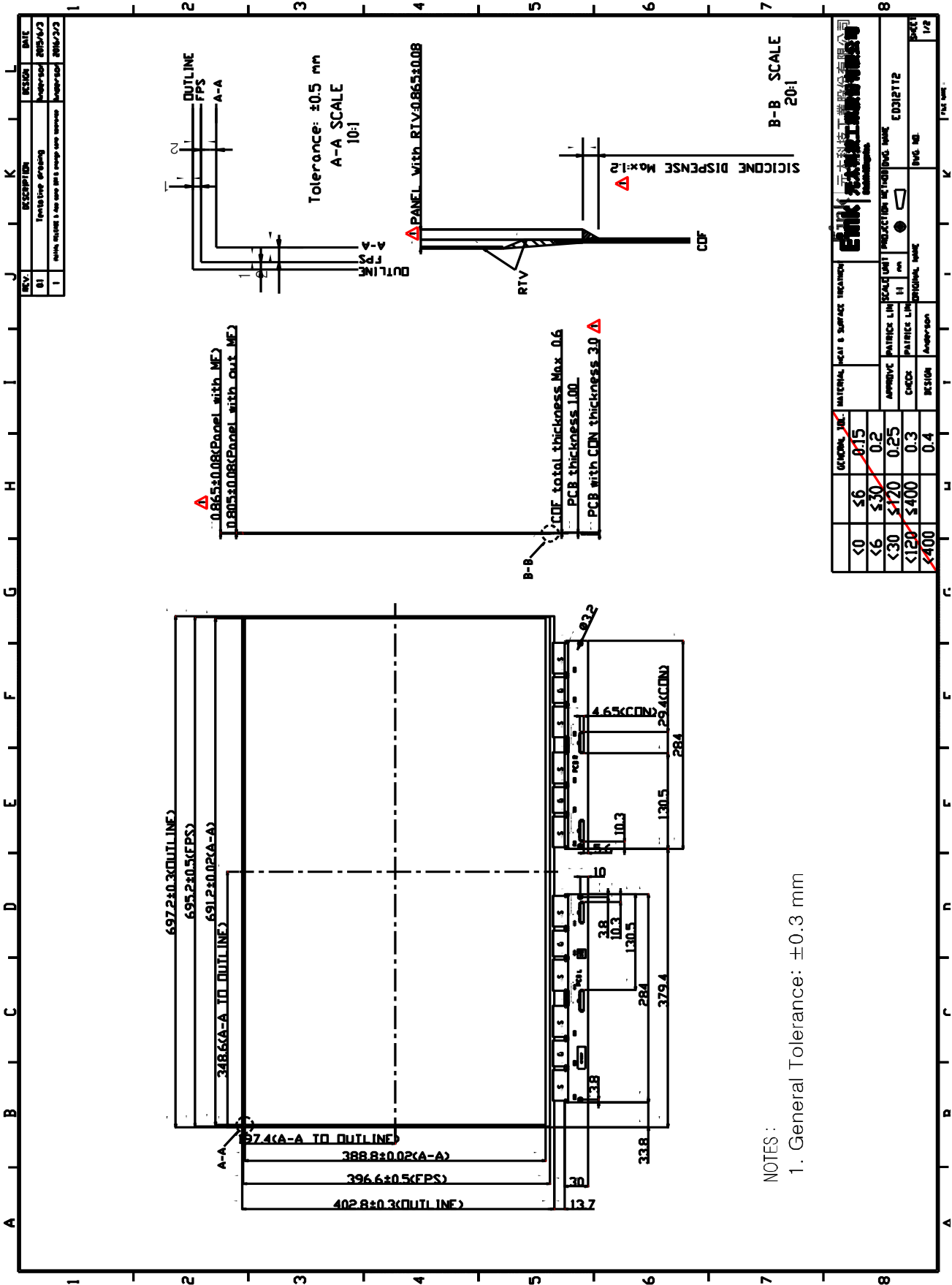
2. Features

- High contrast electrophoretic imaging film
- 2560 x 1440 display
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode

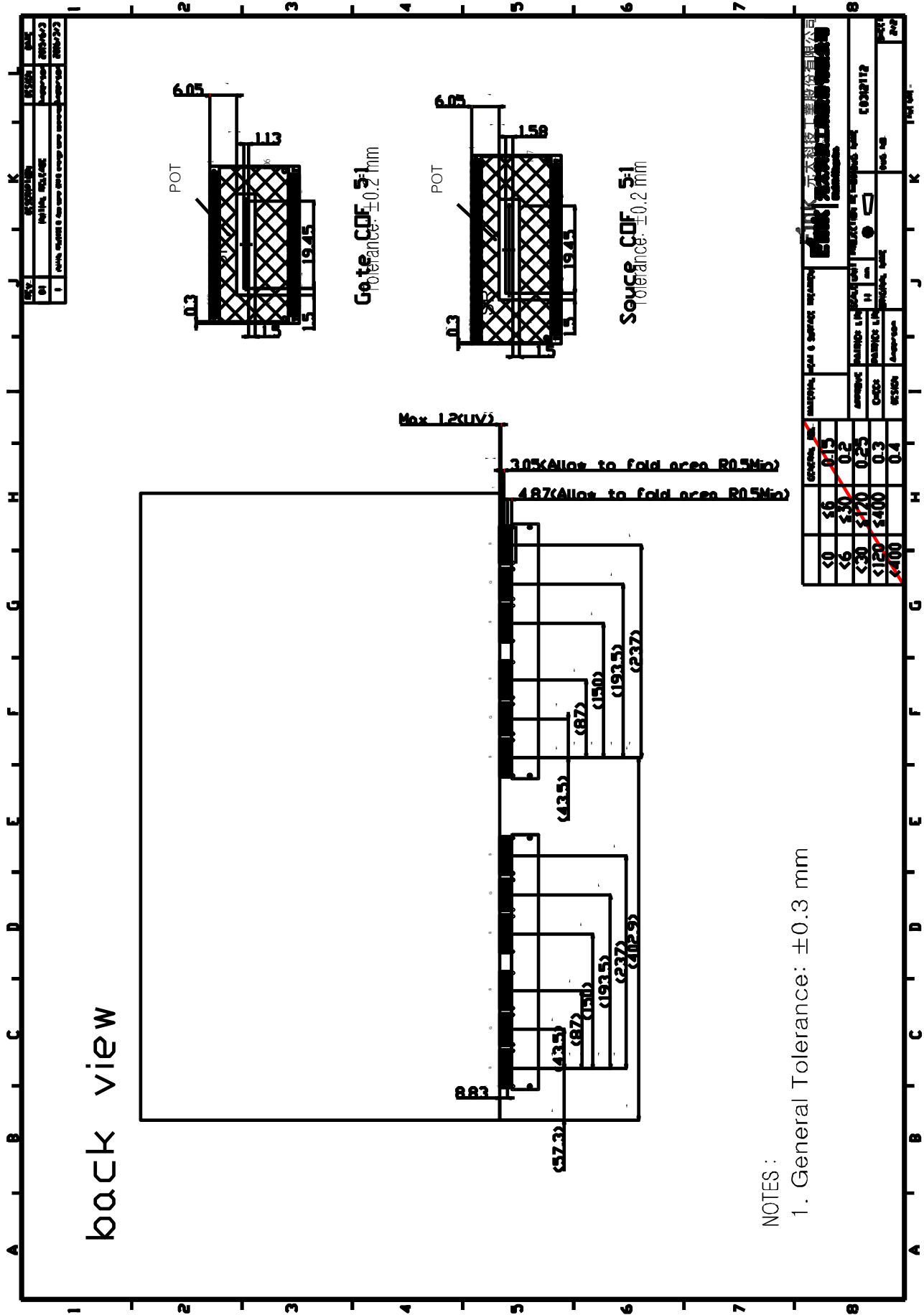
3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	31.2	Inch	
Display Resolution	2560 (H) × 1440 (V)	Pixel	16:9
Active Area	691.2 (H) × 388.8 (V)	mm	94 dpi
Outline Dimension	697.2(H) × 402.8(V) × 0.805(D)	mm	
Pixel Pitch	0.27	mm	
Pixel Configuration	Square		
Module Weight	494	g	
Number of Gray	16 Gray Level (monochrome)		
Display operating mode	Reflective mode		
Glass Substrate	0.5	mm	
Surface Treatment	Hard Coating		
FPL	E Ink Pearl®		

4. Mechanical Drawing of EPD Module



NOTES:
1. General Tolerance: ±0.3 mm



5. Input/output Interface

5-1) Connector type : P-TWO 196033-50041 compatible

5-2) Pin Assignments

Connector L2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2 L2	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1 L2	Output enable gate driver
7	CKV L2	Clock gate driver
8	SPV L2	Start pulse gate driver
9	VSS	Ground
10	VCOM TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL L2	Clock source driver
14	D0 L2	Data signal source driver
15	D1 L2	Data signal source driver
16	D2 L2	Data signal source driver
17	D3 L2	Data signal source driver
18	D4 L2	Data signal source driver
19	D5 L2	Data signal source driver
20	D6 L2	Data signal source driver
21	D7 L2	Data signal source driver
22	VSS	Ground
23	D8 L2	Data signal source driver
24	D9 L2	Data signal source driver
25	D10 L2	Data signal source driver
26	D11 L2	Data signal source driver
27	D12 L2	Data signal source driver
28	D13 L2	Data signal source driver
29	D14 L2	Data signal source driver
30	D15 L2	Data signal source driver
31	XSTL L2	Start pulse source driver
32	XLE L2	Latch enable source driver
33	XOE_L2	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM FPL	Common Voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	Detect1	Detection function pin
43	Detect2	Detection function pin
44	Detect3	Detection function pin
45	NC	NO Connection
46	Detect4	Detection function pin
47	Detect5	Detection function pin
48	Detect6	Detection function pin
49	NC	NO Connection
50	NC	Please keep the pin floating

Connector L1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2_L1	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_L1	Output enable gate driver
7	CKV_L1	Clock gate driver
8	SPV_L1	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_L1	Clock source driver
14	D0_L1	Data signal source driver
15	D1_L1	Data signal source driver
16	D2_L1	Data signal source driver
17	D3_L1	Data signal source driver
18	D4_L1	Data signal source driver
19	D5_L1	Data signal source driver
20	D6_L1	Data signal source driver
21	D7_L1	Data signal source driver
22	VSS	Ground
23	D8_L1	Data signal source driver
24	D9_L1	Data signal source driver
25	D10_L1	Data signal source driver
26	D11_L1	Data signal source driver
27	D12_L1	Data signal source driver
28	D13_L1	Data signal source driver
29	D14_L1	Data signal source driver
30	D15_L1	Data signal source driver
31	XSTL_L1	Start pulse source driver
32	XLE_L1	Latch enable source driver
33	XOE_L1	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	NC	Please keep the pin floating
42	NC	NO Connection
43	NC	NO Connection
44	NC	NO Connection
45	NC	NO Connection
46	NC	NO Connection
47	NC	NO Connection
48	NC	NO Connection
49	NC	NO Connection
50	NC	Please keep the pin floating

Connector R1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2_R1	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_R1	Output enable gate driver
7	CKV_R1	Clock gate driver
8	SPV_R1	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_R1	Clock source driver
14	D0_R1	Data signal source driver
15	D1_R1	Data signal source driver
16	D2_R1	Data signal source driver
17	D3_R1	Data signal source driver
18	D4_R1	Data signal source driver
19	D5_R1	Data signal source driver
20	D6_R1	Data signal source driver
21	D7_R1	Data signal source driver
22	VSS	Ground
23	D8_R1	Data signal source driver
24	D9_R1	Data signal source driver
25	D10_R1	Data signal source driver
26	D11_R1	Data signal source driver
27	D12_R1	Data signal source driver
28	D13_R1	Data signal source driver
29	D14_R1	Data signal source driver
30	D15_R1	Data signal source driver
31	XSTL_R1	Start pulse source driver
32	XLE_R1	Latch enable source driver
33	XOE_R1	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	NC	Please keep the pin floating
42	NC	NO Connection
43	NC	NO Connection
44	NC	NO Connection
45	NC	NO Connection
46	NC	NO Connection
47	NC	NO Connection
48	NC	NO Connection
49	NC	NO Connection
50	NC	Please keep the pin floating

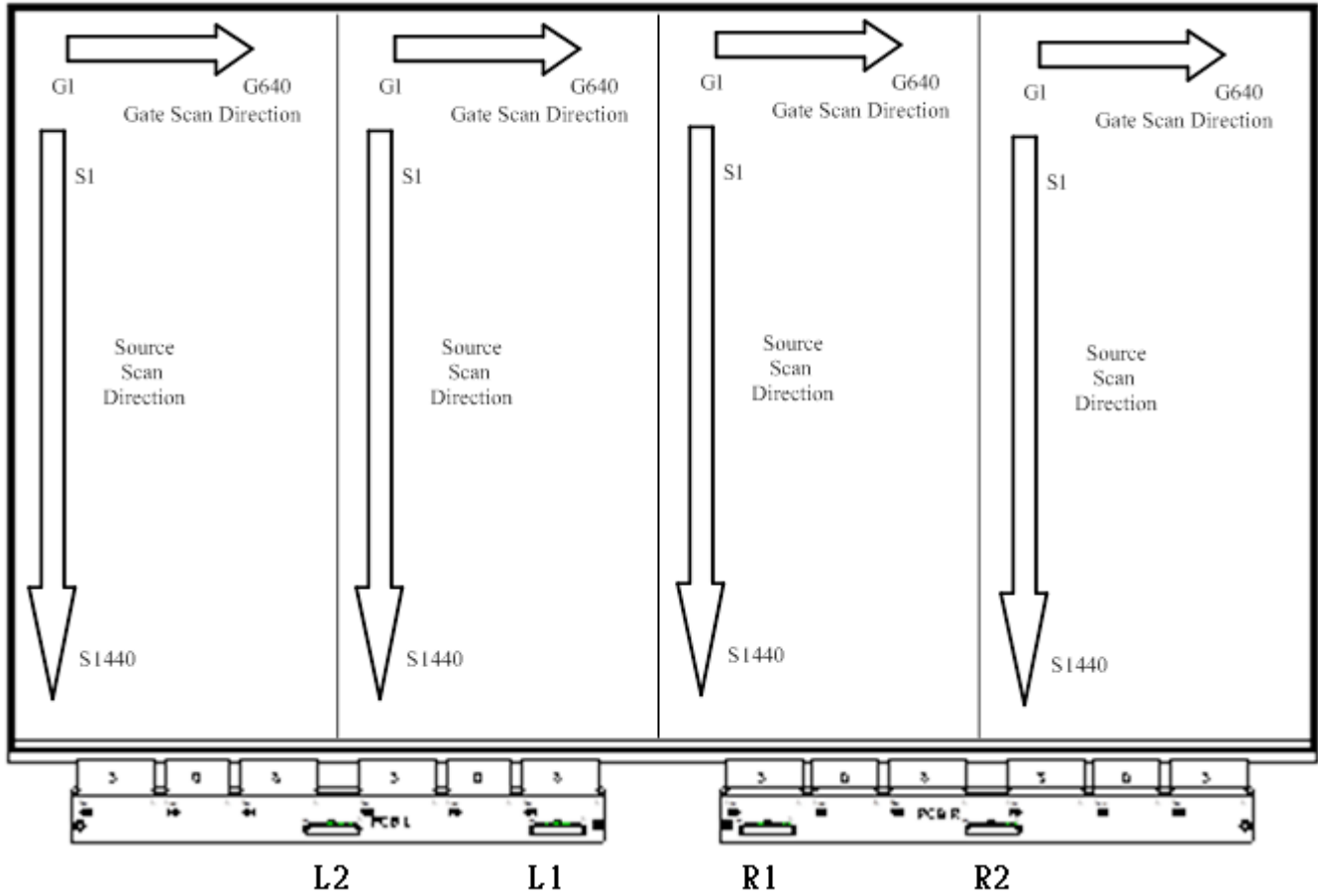
Connector R2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2_R2	Output enable gate driver
5	VDD	Digital power supply drivers
6	Mode1_R2	Output enable gate driver
7	CKV_R2	Clock gate driver
8	SPV_R2	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL_R2	Clock source driver
14	D0_R2	Data signal source driver
15	D1_R2	Data signal source driver
16	D2_R2	Data signal source driver
17	D3_R2	Data signal source driver
18	D4_R2	Data signal source driver
19	D5_R2	Data signal source driver
20	D6_R2	Data signal source driver
21	D7_R2	Data signal source driver
22	VSS	Ground
23	D8_R2	Data signal source driver
24	D9_R2	Data signal source driver
25	D10_R2	Data signal source driver
26	D11_R2	Data signal source driver
27	D12_R2	Data signal source driver
28	D13_R2	Data signal source driver
29	D14_R2	Data signal source driver
30	D15_R2	Data signal source driver
31	XSTL_R2	Start pulse source driver
32	XLE_R2	Latch enable source driver
33	XOE_R2	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".
34	ISEL	Input data bus width selection. L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid inputs. D15 ~ D8 are internal pull down, and user should connect to logic "L" levels or let them open. H: input data bus width is 16-bit.
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	Please keep the pin floating
41	NC	Please keep the pin floating
42	Detect7	Detection function pin
43	Detect8	Detection function pin
44	Detect9	Detection function pin
45	NC	NO Connection
46	NC	NO Connection
47	Detect10	Detection function pin
48	Detect11	Detection function pin
49	Detect12	Detection function pin
50	NC	Please keep the pin floating

NOTE1: Detection function pin is for checking IC & Panel status.

5-3) Panel Scan direction

When panel replace the image, the each sub panel need active at same time



6. Electrical Characteristics

6-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +7	V	--
Positive Supply Voltage	V _{POS}	-0.3 to +18	V	--
Negative Supply Voltage	V _{NEG}	+0.3 to -18	V	--
Max .Drive Voltage Range	V _{POS} - V _{NEG}	36	V	--
Supply Voltage	VGH	-0.3 to +55	V	--
Supply Voltage	VGL	-32 to +0.3	V	--
Supply Range	VGH-VGL	-0.3 to +55	V	--
Operating Temp. Range	TOTR	0 to +50	°C	--
Storage Temperature	TSTG	-25 to +70	°C	--

6-2) Panel DC characteristics

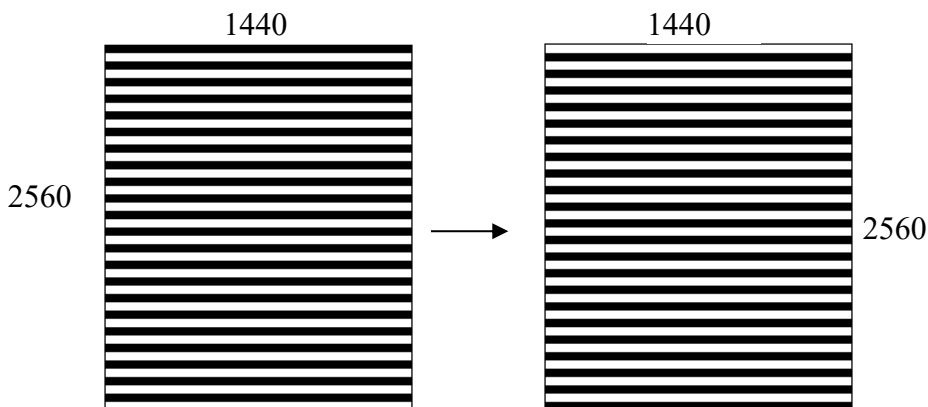
this is the total current for 4 sub panel

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V _{SS}		-	0	-	V
Logic Voltage supply	V _{DD}		2.7	3.3	3.6	V
	I _{VDD}	V _{DD} = 3.3V	-	3	7	mA
Gate Negative supply	V _{GL}		-21	-20	-19	V
	I _{GL}	V _{GL} = -20V	-	4	9	mA
Gate Positive supply	V _{GH}		21	22	23	V
	I _{GH}	V _{GH} = 22V	-	3	6	mA
Source Negative supply	V _{NEG}		-15.4	-15	-14.6	V
	I _{NEG}	V _{NEG} = -15V	-	7	415	mA
Source Positive supply	V _{POS}		14.6	15	15.4	V
	I _{POS}	V _{POS} = 15V	-	7	445	mA
Asymmetry source	V _{Asym}	V _{POS} +V _{NEG}	-800	-	+800	mV
Common voltage	V _{COM}		-2.96	Adjusted	-2.04	V
	I _{COM}		-	1.2	-	mA
Panel power	P		-	370	13300	mW
Standby power panel	P _{STBY}		-	-	1.32	mW
Rush current	I _{DD}	VDD=3.3V	-260		260	mA
	I _{GL}	VGL=-20V	-2700		2700	mA
	I _{GH}	VGH=22V	-230		230	mA
	I _{NEG}	V _{NEG} =-15V	-2000			mA
	I _{POS}	V _{POS} =15V			2000	mA
	I _{com}		-800		800	mA

- The maximum power consumption is measured using 50Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)
- The Typical power consumption is measured using 50Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink.
- Vcom is recommended to be set in the range of assigned value $\pm 0.1V$.
- The maximum I_{COM} inrush current is about 2 A
- The rush current is for reference only

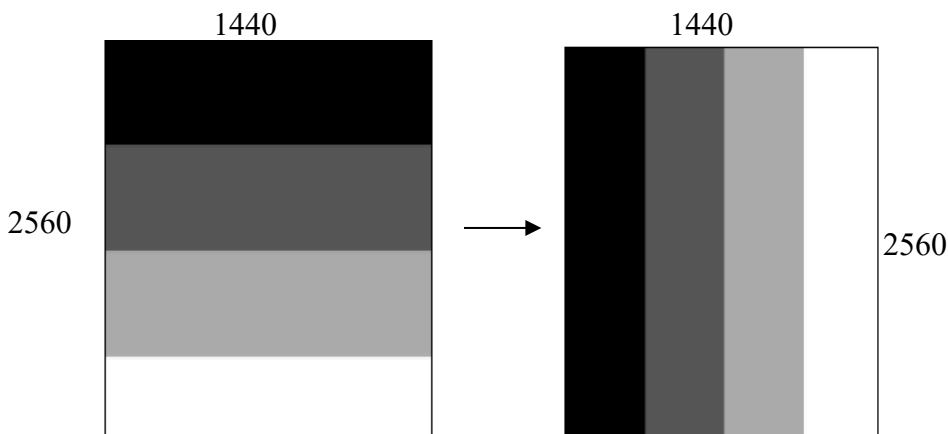
Note 6-1

The maximum power consumption



Note6-2

The Typical power consumption



6-3) Refresh Rate

The module ED312TT3 is applied at a maximum screen refresh rate of 50Hz.

	Min	Max
Refresh Rate	-	50Hz

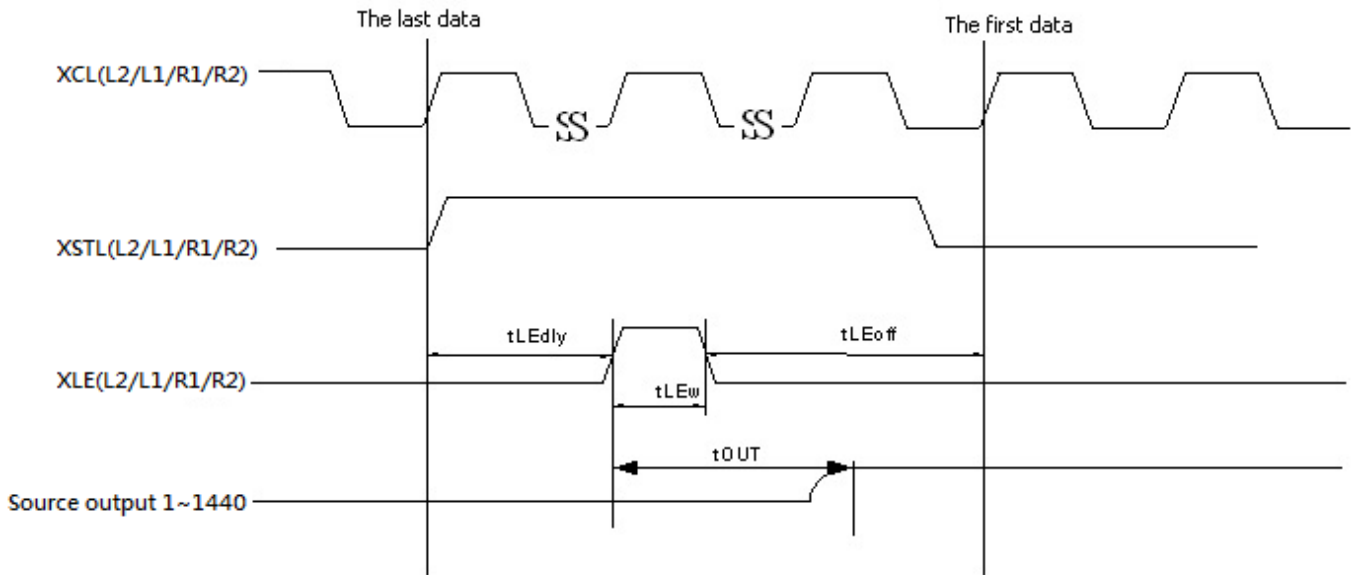
6-4) Panel AC characteristics

VDD=2.7 V to 3.6V, unless otherwise specified.

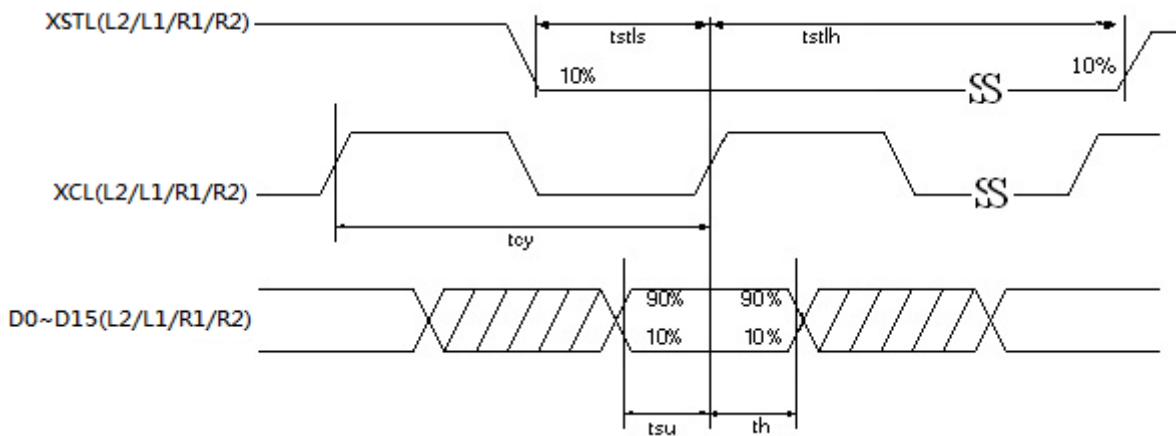
For 1/4 panel (the timing parameter for each sub panel)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum “L” clock pulse width	twL	0.5	-	-	us
Minimum “H” clock pulse width	twH	0.5	-	-	us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.7	20	-	ns
D0 .. D15 setup time	tsu	8	-	-	ns
D0 .. D15 hold time	th	8	-	-	ns
XSTL setup time	tstls	8	-	-	ns
XSTL hold time	tstlh	8	-	-	ns
XLE on delay time	tLEdly	40	-	-	ns
XLE high-level pulse width (When VDD=2.7V to 3.6V)	tLEw	40	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C _{load} =200pF)	tout	-	-	12	us

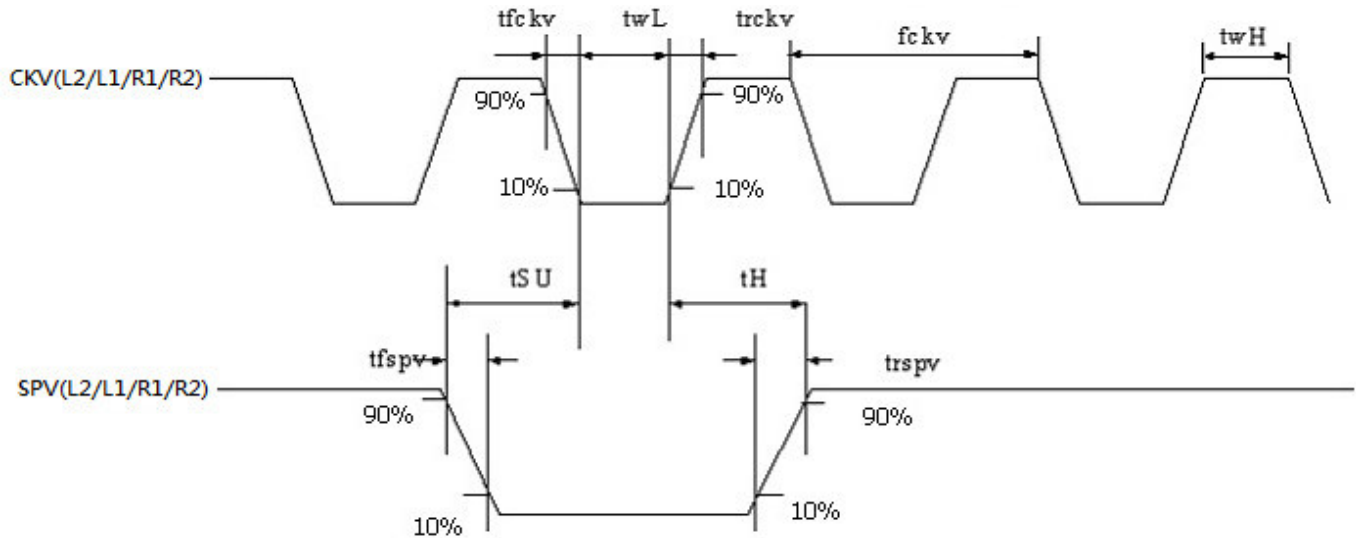
OUTPUT LATCH CONTROL SIGNALS



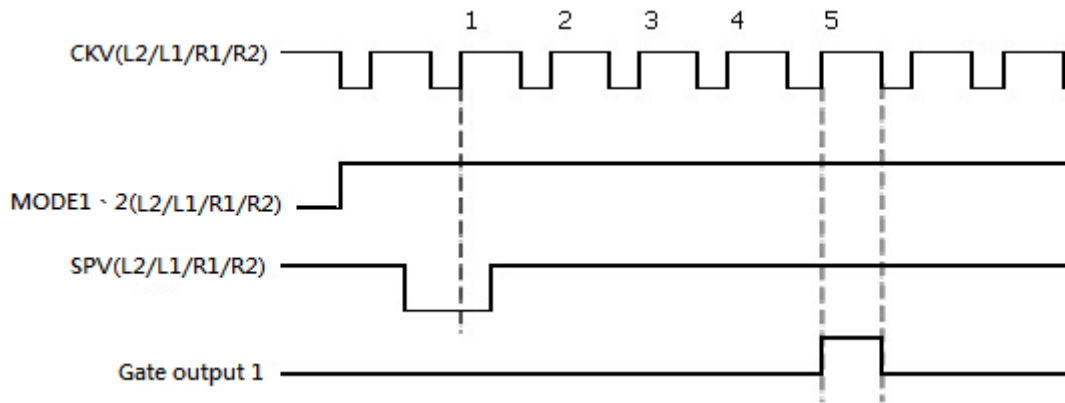
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note : First gate line on timing
After 5CKV, Gate output 1 is on.

6-5) Controllers Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE)⁽³⁾ and Gate Driver Clock (GDCK)⁽³⁾. Note, that in this mode LGON follows GDCK timing.

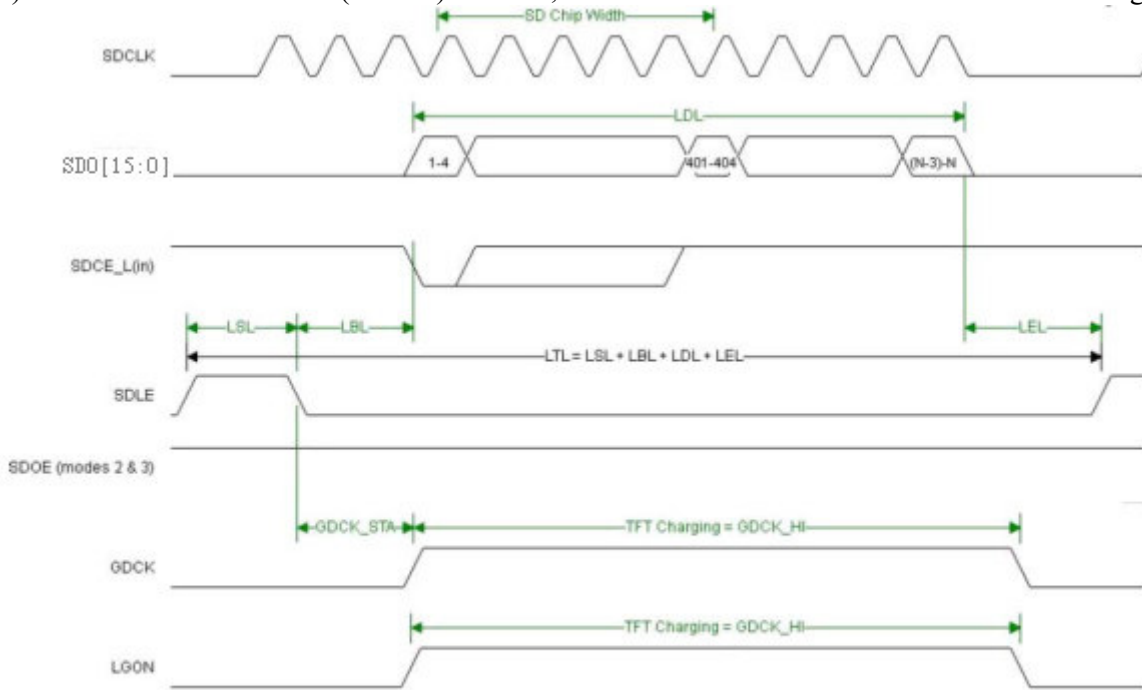


Figure 1 Line Timing in Mode 3

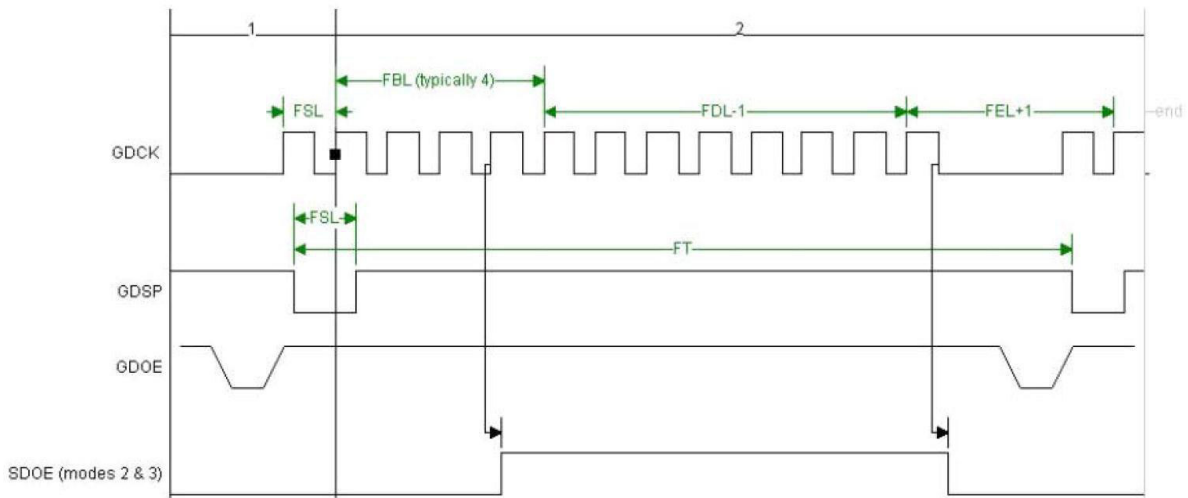


Figure 2 Frame Timing in Mode 3

Table Timing Parameters Table

For 1/4 panel

Mode	3	Resolution 1440x640				
SDCLK [MHz]	10.00					
Pixels per SDCLK	8					
Line Parameters [SDCLK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	11	11	180	101	11	280
Line Parameters [us]	-	-	-	-	-	-
	1.10	1.10	18.00	10.10	1.10	28.00
Frame Parameters [Lines]	FSL	FBL	FDL	FEL	-	FR[Hz]
	1	4	640	14	-	50.08
Frame Parameters[us]	-	-	-	-	-	-
	30.30	121.20	19392.00	424.20	-	-

Note 1: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL.

Note 2:

$SDCLK = XCL(L2/L1/R1/R2)$

$SDD[15:0] = D0\sim D15(L2/L1/R1/R2)$

$SDCE_L(in) = XSTL(L2/L1/R1/R2)$

$GDCK = CKV(L2/L1/R1/R2)$

$GDSP = SPV(L2/L1/R1/R2)$

$GDOE = Mode1 \cdot 2(L2/L1/R1/R2)$

$SDOE = XOE(L2/L1/R1/R2)$

7. Power Sequence

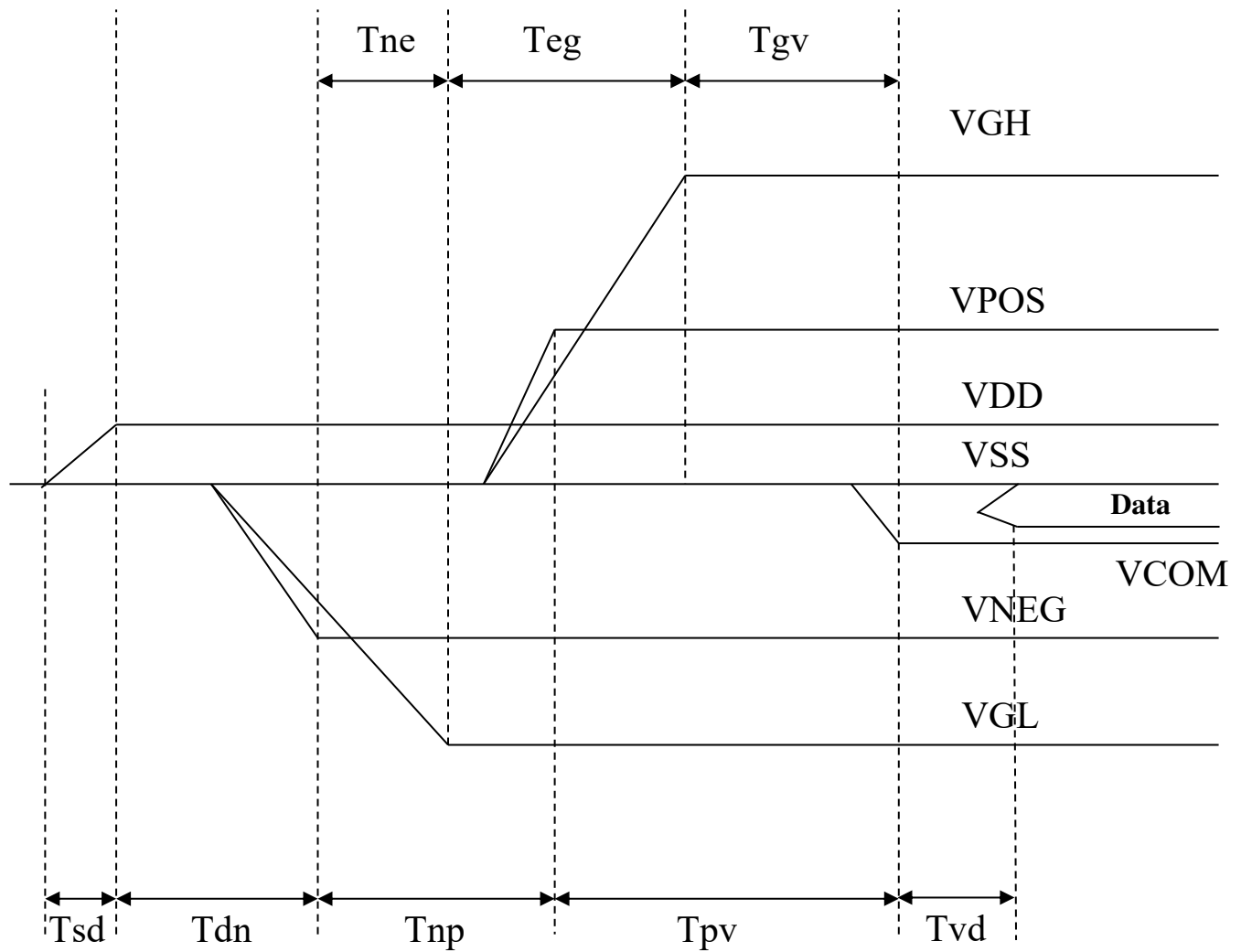
Power Rails must be sequenced in the following order:

1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

Note:

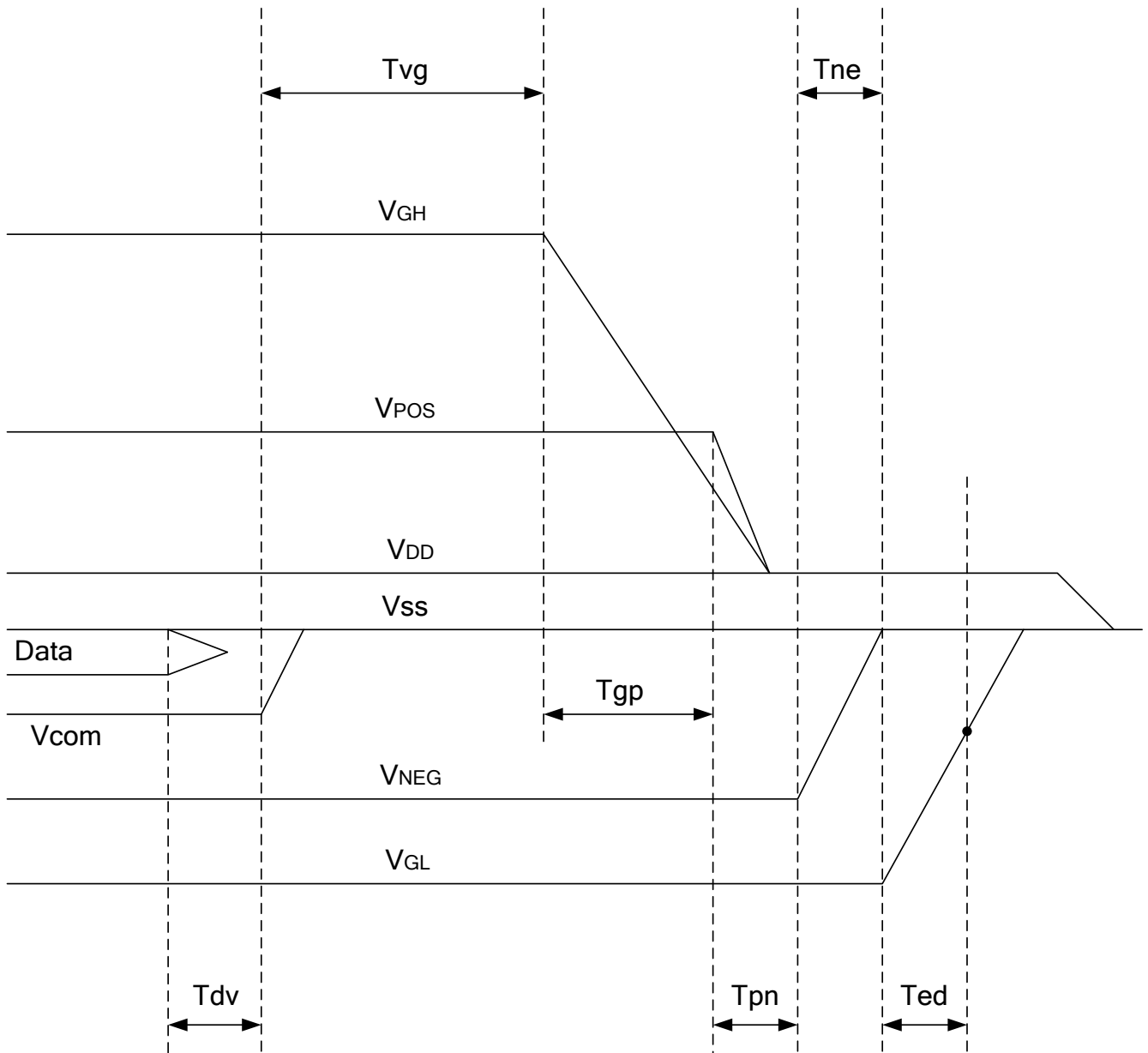
- VGL should be turned off after VNEG and VPOS have been turned off and returned to the ground state.
- VGL should be turned off after the Vcom has been turned off and returned to the ground state.
- All of Vcom/VNEG/VPOS/VGN/VGL MUST turn off right after data transfer completes.

Power on



	Min	Max
Tsd	30us	-
Tdn	100us	-
Tnp	1000us	-
Tpv	100us	-
Tvd	100us	-
Tne	0us	-
Teg	1000us	-
Tgv	100us	-

Power off



	Min	Max	
Tdv	100μs	-	
Tvg	0μs	-	
Tgp	0μs	-	
Tpn	0μs	-	
Tne	0μs	-	
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note1 : Supply voltages decay through pull-down resistors.

8. Optical characteristics

8-1) Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

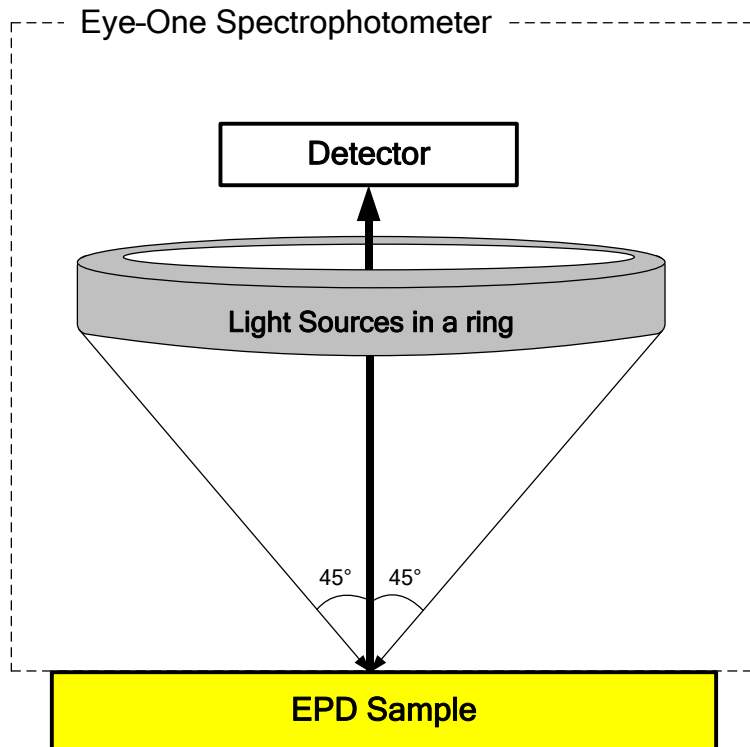
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	40	-	%	Note 8-1
Gn	N _{th} Grey Level	-	-	$DS+(WS-DS) \times n / (m-1)$	-	L*	-
CR	Contrast Ratio	-	10	12	-		

WS: White state, DS: Dark state, Gray state from Dark to White: DS、G1、G2...、Gn...、Gm-2、WS
m: 4、8、16 when 2、3、4 bits mode.

Note 8-1: Luminance meter: Eye – One Pro Spectrophotometer.

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): $CR = Rl/Rd$.



8-3) Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety, and Environment Requirements and Remark

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status
Product specification
This data sheet contains Preliminary product specifications.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Remark

All the specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any post-assembly operation.

10. Reliability Test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +65°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = -15°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
6	High Temperature, High- Humidity Storage	T = +60°C, RH=80% for 168 hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25°C → +70°C, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
8	Solar radiation test	765 W/m ² for 168hrs, 40°C Test in white pattern	IEC60 068-2-5Sa	
9	Package Vibration	Random wave(1.5Grms 10~200Hz) Direction: X,Y,Z 30mins per axes	Full packed for shipment	
10	Package Drop Impact	Height: 15.2 cm. 6 faces	Full packed for shipment	
11	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	

Actual EMC level to be measured on customer application

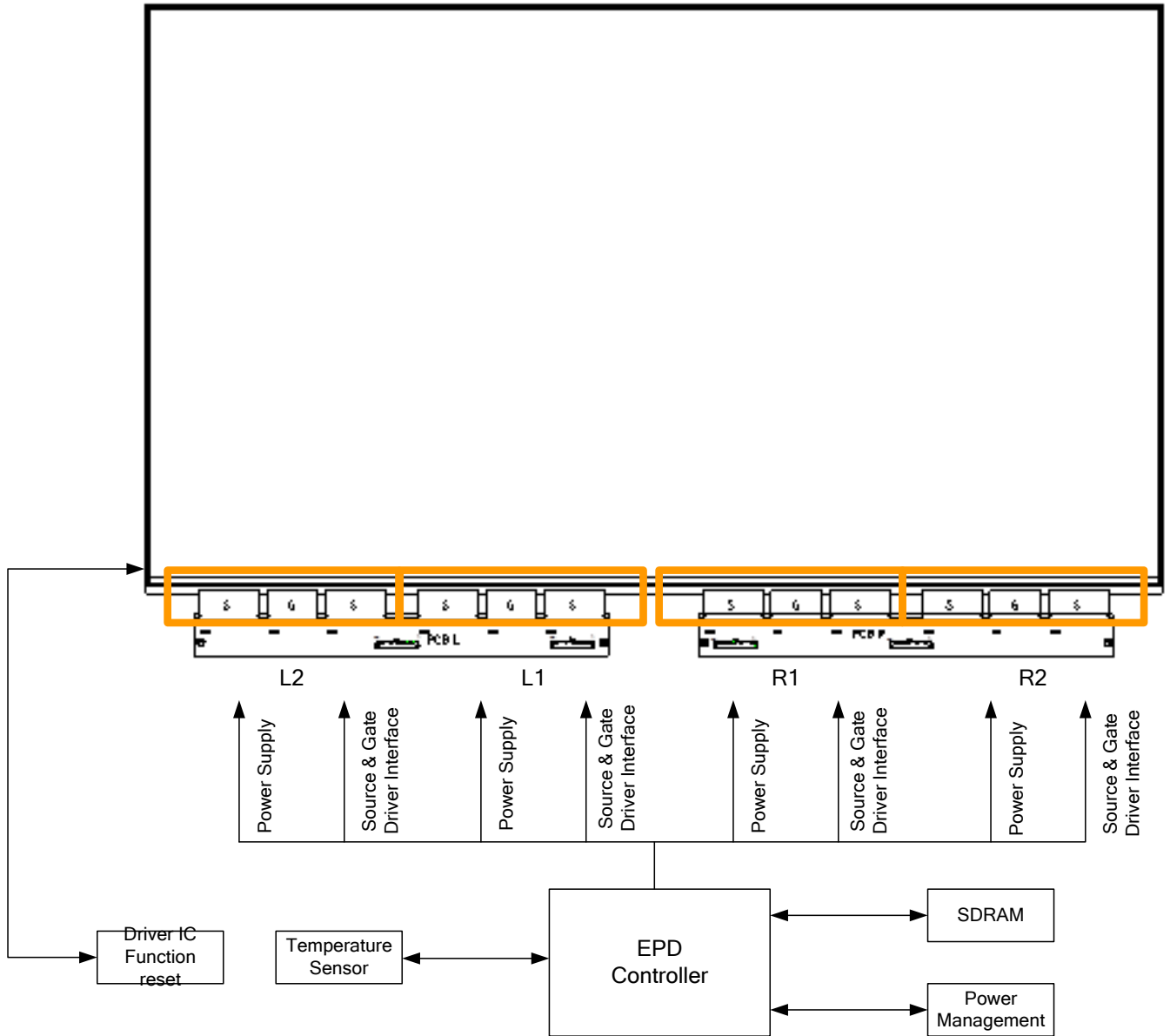
Note: The protective film must be removed before temperature test.

< Criteria >

In the standard conditions, there is not display function NG issue occurred. (Line defect, no image).

All the cosmetic specification is judged before the reliability stress.

11. Block Diagram



12. Packing

12-1) packing drawing

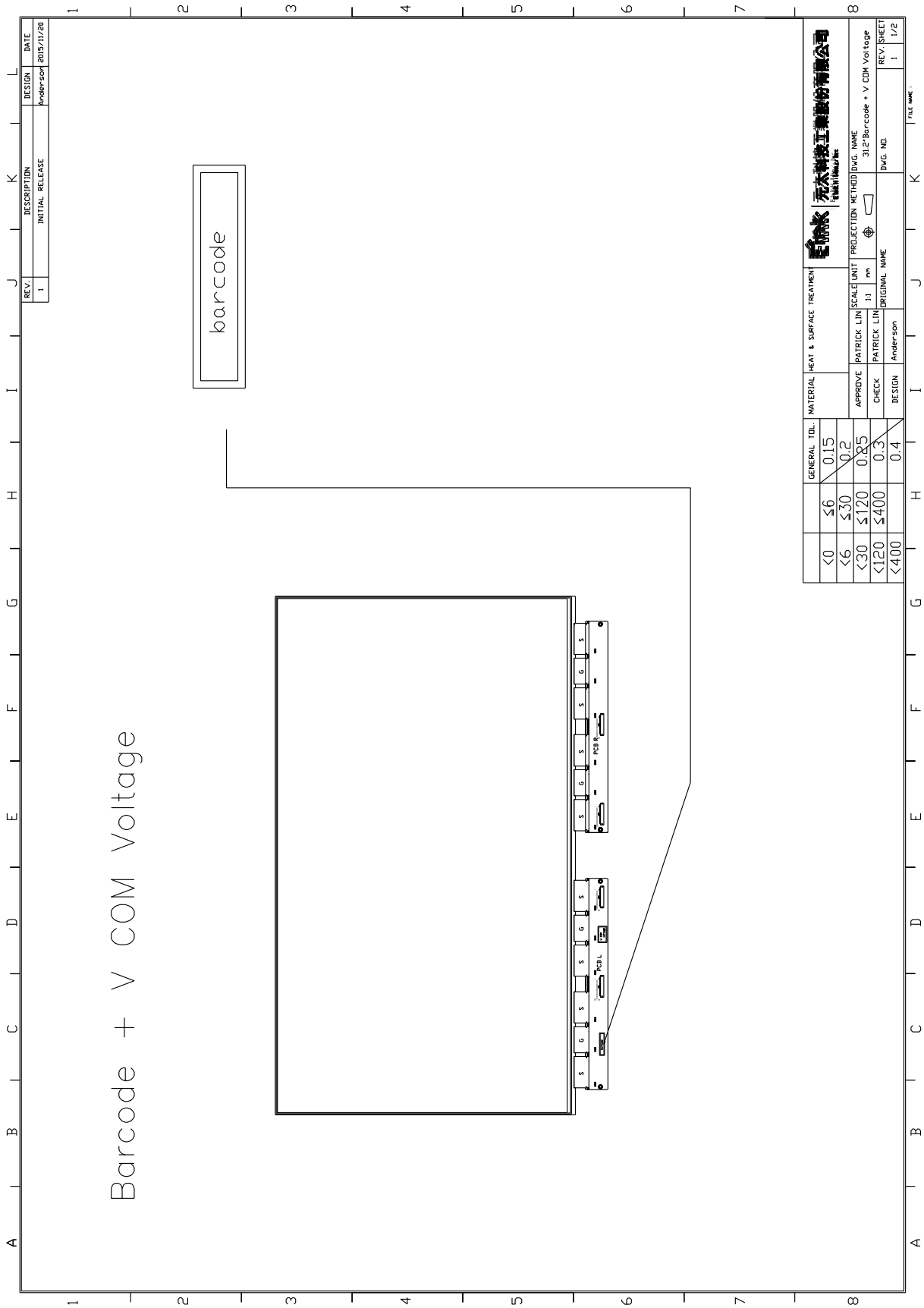
REV.	DESCRIPTION	DESIGN	DATE
10	INITIAL RELEASE	Anderson Tung	20160114
20	Delete RUST INHIBITOR	Anderson Tung	20180921

Note:

- Q'ty: 10pcs EPD/PP BOX
- Dimension: 831.2*590*138mm
- Wight: 8.0Kg

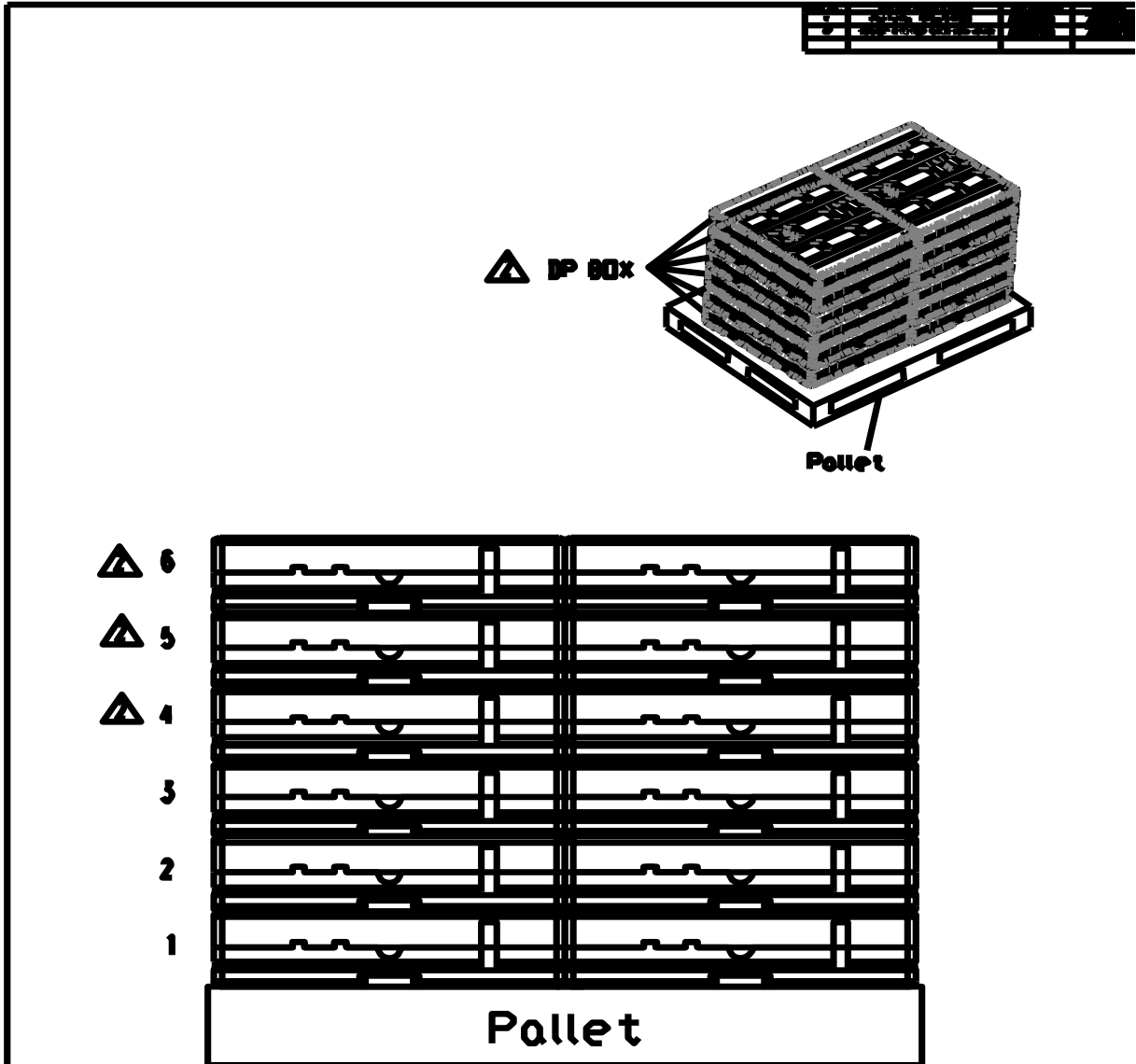
MATERIAL	HEAT & SURFACE TREATMENT	Eink 元太科技工業股份有限公司				
APPROVE	CC Chen	SCALE	UNIT	PROJECTION METHOD	DWG. NAME	
CHECK	CC Chen	5/1	mm		ED312TT2 Packing drawing	
DESIGN	Anderson Tung	ORIGINAL NAME			DWG. NO.	SHEET
						1/1


12-2) Label position




12-3) Pallet Stacking

Note: Stacking layer limitation: 6 layers.



NOTE=
 1.Pallet Dimension 1200*1000*145 mm
 2. 2*6=12 Boxes/Pallet. 
 3.DP Box Dimension :831.2*590.5*138 mm

2	DP BOX	12	
1	Pallet	1	
INVPART NO.	DESCRIPTION	QTY	REMARK

UNSPEC.		UNSPECIFIED TOL'S		REMARK		 元太科技工業股份有限公司 E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.		
		NGLS						
		REWORKS						
APPROV	CC Chen	20180130	SCALE	1:1	UNIT	mm	SHEET	1 of 1
CHECK	CC Chen	20180130			DESCRIPTION			
DESIGN	Anderson	20180130	DATE		ED312TT2 Boxes&Pallet			
				DATE				

13. Bar Code Definition

<u>ET1</u>	<u>00</u>	<u>6</u>	<u>01</u>	<u>1</u>	<u>I</u>	<u>7</u>	<u>4</u>	<u>00361</u>	<u>A</u>	<u>I</u>
<u>1</u>	<u>2</u>	<u>3</u>	<u>4</u>	<u>2</u>	<u>5</u>	<u>6</u>	<u>2</u>	<u>7</u>	<u>2</u>	<u>8</u>

1 : EPD model code

2 : Internal control codes

3 : Internal control codes

4 : Internal control codes

5 : Year:
T:2018 / U:2019 / V:2020 / ... / Z: 2024

6 : Month:
1:Jan. 2:Feb. ... 9:Sep. A:Oct. B:Nov. C:Dec.

7 : Serial number
00000-99999

8 : Internal control codes



ALL TECHNOLOGIES. ALL COMPETENCIES. ONE SPECIALIST.



DATA MODUL AG
Landsberger Straße 322
DE-80687 Munich
Phone: +49-89-56017-0

DATA MODUL WEIKERSHEIM GMBH
Lindenstraße 8
DE-97990 Weikersheim
Phone: +49-7934-101-0



More information and worldwide locations can be found at

www.data-modul.com