DATA MODUL

SPECIFICATION

ED280TT1

28”, 3840x1080

Version: 1.0
Date: 18.02.2021

Note: This specification is subject to change without prior notice

www.data-modul.com

Version: 1.0

TECHNICAL SPECIFICATION

MODEL NO: VB3300-PHA (ED280TT1)

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

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Revision History

Rev.	Issued Date	Revised Contents
0.1	2020.06.22	Tentative version.
0.2	2020.12.29	Modified Pin Assignment, Page 6. Modified Electrical Characteristics, Page 9. Modified Power Sequence, Page 17. Modified Packing, Page 24.
0.3	2021.02.18	Modified Mechanical Specifications, Page 4. Modified Mechanical Drawing of EPD Module, Page 5. Modified Pin Assignment, Page 6. Modified Electrical Characteristics, Page 9. Modified Packing, Page 26.
1.0	2021.02.18	First official version.

TECHNICAL SPECIFICATION

CONTENTS

1. General Description

ED280TT1 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 28” active area with 3840 x 1080 pixels and 32:9 aspect ratio. The display is capable to display images at 16 Gray levels (1 to 4 bits) depending on the display controller and the associated waveform file it used.

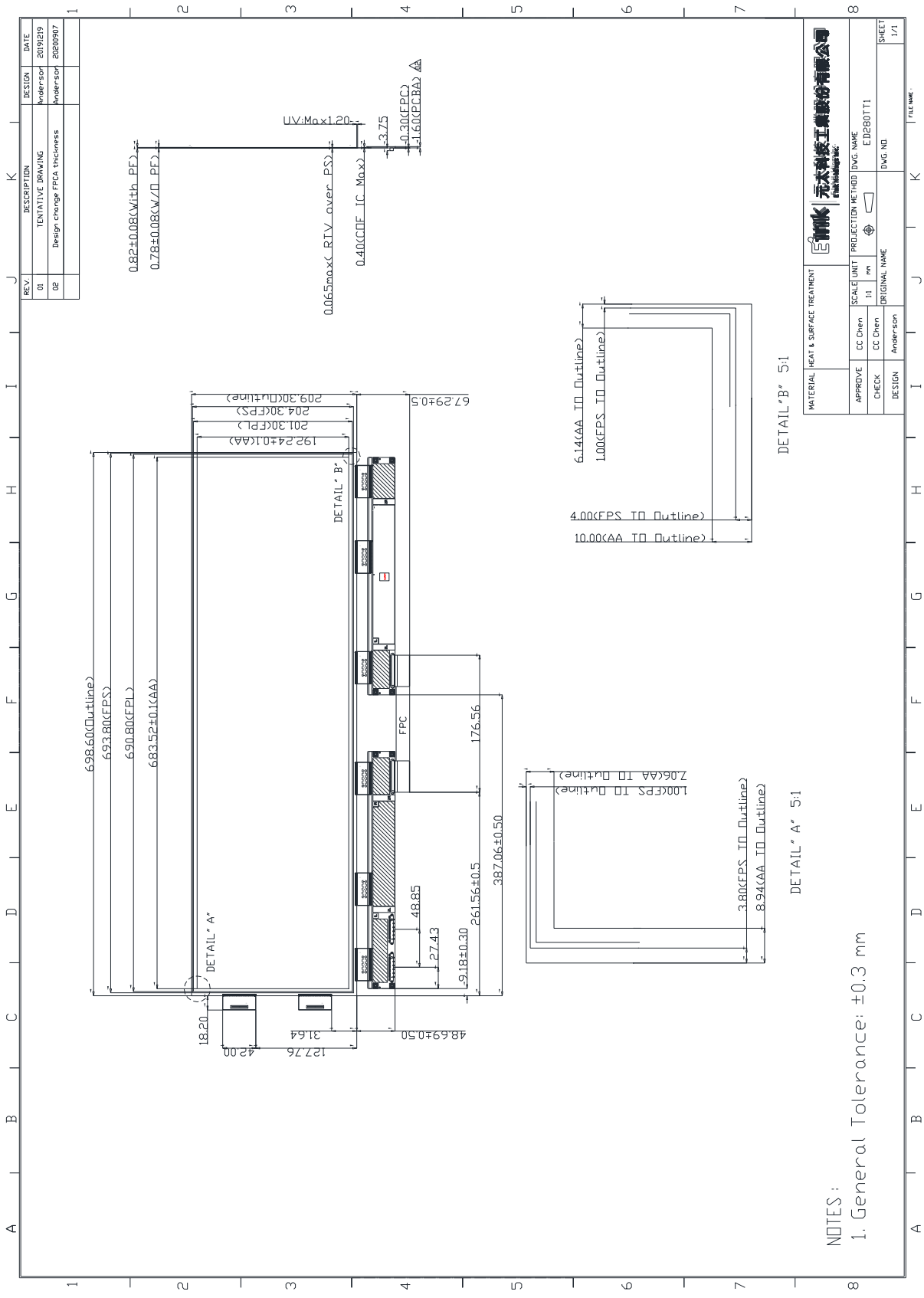
2. Features

- High contrast electrophoretic imaging film
- 3840 x 1080 display
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-stable
- Landscape mode

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	28”	inch	
Display Resolution	3840(H) x 1080(V)	Pixel	32:9
Active Area	683.52(H) x 192.24 (V)	mm	143dpi
Outline Dimension	698.6(H) x 209.3 (V) x 0.82(D)	mm	
Pixel Pitch	0.178	mm	
Pixel Configuration	Square		
Module Weight	320	g	
Number of Grey	16 Gray Level		
Display operating mode	Reflective mode		
Glass Substrate	0.5mm	mm	
Surface Treatment	Anti-glare		
FPL	E Ink Carta™		
Driver IC	Source COF: Himax HX-5271 Gate COF: Solomon SPD1652		

4. Mechanical Drawing of EPD Module



5. Input / Output Interface

5-1) Connector type:

Item	Pin numbers	Pitch (mm)	Connector	Note
CN1	51	0.5	P-TWO 187059-51221-1	LVDS Type
CN2	51	0.5	P-TWO 187059-51221-1	LVDS Type

5-2) Pin Assignment

Connector CN1

Pin #	Signal	I/O	Description	Remark
1	VCOM	P	Common Voltage.	
2	VCOM	P	Common Voltage.	
3	VCOM	P	Common Voltage.	
4	NC	-	NO Connection	
5	VCOM	P	Common Voltage.	
6	VCOM	P	Common Voltage.	
7	NC	-	NO Connection	
8	BORDER	P	Border connection	
9	NC	-	NO Connection	
10	VGH	P	Positive power supply gate driver.	
11	VGH	P	Positive power supply gate driver.	
12	NC	-	NO Connection	
13	VP3	P	Positive power supply source driver.	
14	VP3	P	Positive power supply source driver.	
15	VP3	P	Positive power supply source driver.	
16	NC	-	NO Connection	
17	VP2	P	Positive power supply source driver.	
18	VP2	P	Positive power supply source driver.	
19	VP2	P	Positive power supply source driver.	
20	NC	-	NO Connection	
21	VP1	P	Positive power supply source driver.	
22	VP1	P	Positive power supply source driver.	
23	VP1	P	Positive power supply source driver.	
24	NC	-	NO Connection	
25	VDD	P	Logic power.	
26	VDD	P	Logic power.	
27	NC	-	NO Connection	
28	VSS	P	Ground	
29	VSS	P	Ground	
30	NC	-	NO Connection	
31	VN1	P	Negative power supply source driver.	
32	VN1	P	Negative power supply source driver.	
33	VN1	P	Negative power supply source driver.	
34	NC	-	NO Connection	
35	VN2	P	Negative power supply source driver.	
36	VN2	P	Negative power supply source driver.	
37	VN2	P	Negative power supply source driver.	
38	NC	-	NO Connection	
39	VN3	P	Negative power supply source driver.	
40	VN3	P	Negative power supply source driver.	
41	VN3	P	Negative power supply source driver.	
42	NC	-	NO Connection	
43	VGL	P	Negative power supply gate driver.	
44	VGL	P	Negative power supply gate driver.	
45	NC	-	NO Connection	
46	NC	-	NO Connection	

47	NC	-	NO Connection	
48	NC	-	NO Connection	
49	STBYB	I	mini-LVDS enable.	
50	XON	I	XON signal gate driver	
51	MODE	I	Output enable gate driver	

Note: **P** in I/O: Power pin

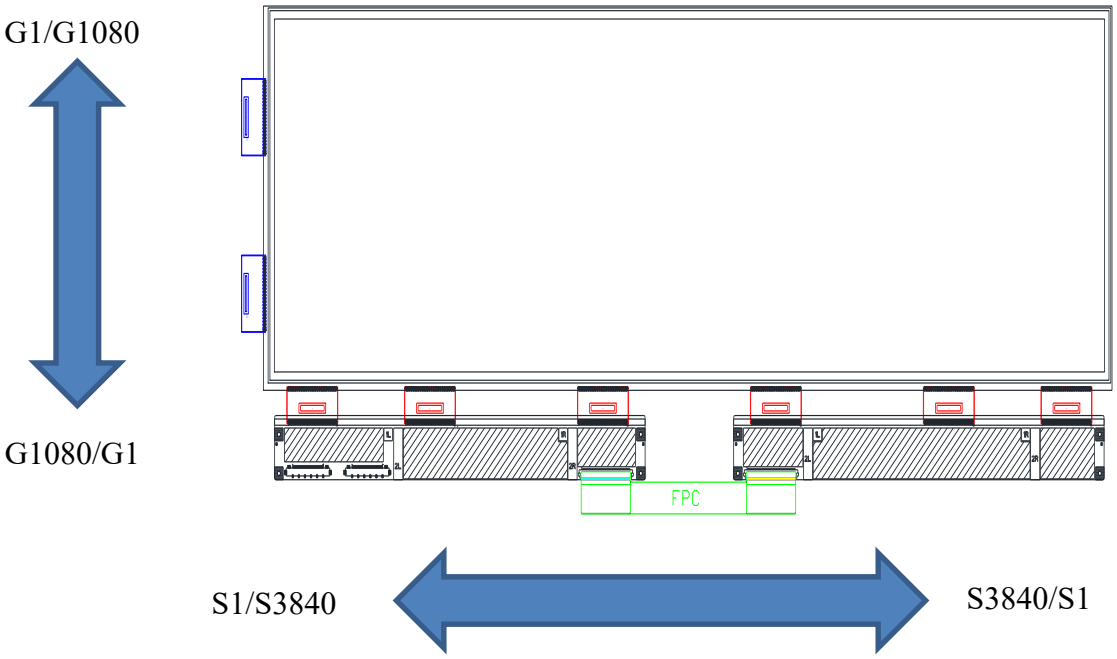
Connector CN2

Pin #	Signal	I/O	Description	Remark
1	DSEL	I	Data Input select	
2	LEH	I	Latch enable source driver	
3	OEH	I	Outputs enabled when OE is logic "H", Outputs forced to GND when OE is logic "L".	
4	UD	I	Shift direction control pin gate driver UD = H: Data shift direction from G1 to G800. UD = L: Data shift direction from G800 to G1.	
5	SHR	I	Shift direction control pin source driver SHR =H: Data inputs read sequentially from S800 to S1. SHR =L: Data inputs read sequentially from S1 to S800.	
6	SPV2	I/O	Start pulse gate driver UD / Start pulse input / Start pulse output H / SPV1 / SPV2 L / SPV2 / SPV1	
7	SPV1	I/O	Start pulse gate driver UD / Start pulse input / Start pulse output H / SPV1 / SPV2 L / SPV2 / SPV1	
8	SPH2	I/O	Start pulse source driver SHR / Start pulse input / Start pulse output H / SPH2 / SPH1 L / SPH1 / SPH2	
9	SPH1	I/O	Start pulse source driver SHR / Start pulse input / Start pulse output H / SPH2 / SPH1 L / SPH1 / SPH2	
10	VSS	P	Ground	
11	CKV	I	Clock gate driver	
12	VSS	P	Ground	
13	LV11N	I	Data signal source driver	
14	LV11P	I	Data signal source driver	
15	VSS	P	Ground	
16	LV10N	I	Data signal source driver	
17	LV10P	I	Data signal source driver	
18	VSS	P	Ground	
19	LV9N	I	Data signal source driver	
20	LV9P	I	Data signal source driver	
21	VSS	P	Ground	
22	LV8N	I	Data signal source driver	
23	LV8P	I	Data signal source driver	
24	VSS	P	Ground	
25	LV7N_D15	I	Data signal source driver	
26	LV7P_D14	I	Data signal source driver	
27	VSS	P	Ground	
28	LV6N_D13	I	Data signal source driver	
29	LV6P_D12	I	Data signal source driver	

30	VSS	P	Ground	
31	CLKN_GLOSTL	I	Data signal source driver	
32	CLKP_CKH	I	Data signal source driver	
33	VSS	P	Ground	
34	LV5N_D11	I	Data signal source driver	
35	LV5P_D10	I	Data signal source driver	
36	VSS	P	Ground	
37	LV4N_D9	I	Data signal source driver	
38	LV4P_D8	I	Data signal source driver	
39	VSS	P	Ground	
40	LV3N_D7	I	Data signal source driver	
41	LV3P_D6	I	Data signal source driver	
42	VSS	P	Ground	
43	LV2N_D5	I	Data signal source driver	
44	LV2P_D4	I	Data signal source driver	
45	VSS	P	Ground	
46	LV1N_D3	I	Data signal source driver	
47	LV1P_D2	I	Data signal source driver	
48	VSS	P	Ground	
49	LV0N_D1	I	Data signal source driver	
50	LV0P_D0	I	Data signal source driver	
51	VSS	P	Ground	

Note: **P** in I/O: Power pin

5-3) Panel Scan direction



6. Electrical Characteristics

6-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5.0	V	
Source Positive Supply Voltage	VP3	-0.3 to VN3+50	V	
Source Positive Supply Voltage	VP2	-0.3 to VP3	V	
Source Positive Supply Voltage	VP1	-0.3 to VP3	V	
Source Negative Supply Voltage	VN1	VN3 to + 0.3	V	
Source Negative Supply Voltage	VN2	VN3 to + 0.3	V	
Source Negative Supply Voltage	VN3	-25 to + 0.3	V	
Gate Positive Supply Voltage	VGH	-0.3 to +55	V	
Gate Negative Supply Voltage	VGL	-32 to +0.3	V	
Supply Range	VGH-VGL	-0.3 to +55	V	
Operating Temp. Range	TOTR	-15 to +65	℃	
Storage Temperature	TSTG	-25 to +70	℃	

6-2) Panel DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal Ground	VSS			0		V
Logic voltage Supply	VDD		2.7	3.3	3.6	V
	IDD	VDD=3.3V		30.88	45.34	mA
Gate Negative Supply	VGL		-21	-20	-19	V
	IGL	VGL=-20V		5.28	10.24	mA
Gate Positive Supply	VGH		26	27	28	V
	IGH	VGH=27V		2.41	2.89	mA
Source Negative Supply	VN1		-16	-15	-14	V
	IN1	VN1=15V		8.96	467.82	mA
Source Negative Supply	VN2		-13	-12	-11	V
	IN2	VN2=10V		0.43	1.21	mA
Source Negative Supply	VN3		-21	-20	-19	V
	IN3	VN3=20V		8.81	57.08	mA
Source Positive Supply	VP1		14	15	16	V
	IP1	VP1=-15V		5.51	455.59	mA
Source Positive Supply	VP2		11	12	13	V
	IP2	VP2=-10V		1.56	8.05	mA
Source Positive Supply	VP3		19	20	21	V
	IP3	VP3=-20V		0.68	22.98	mA
Border Supply	-		-	-	-	V
Asymmetry Source	Vasm	VP1+VN1	-800		800	mV

Common Voltage	VCOM		-3.5	Adjusted	-0.3	V
	ICOM			8.73	11.82	mA
Maximum Power panel	Pmax				16388	mW
Typical power panel	Ptyp			878		mW
Standby power panel	Pstby				60.2	mW

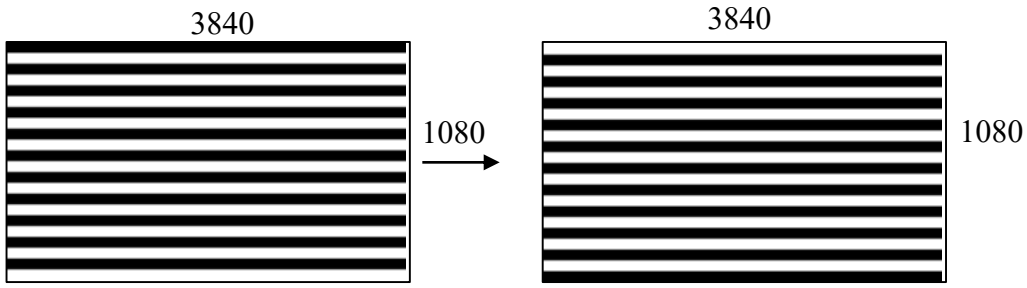
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents (Note 5)	IP1	VP1 = 15V	-		1500	mA
	IN1	VN1 = -15V	-		1540	mA
	IGH	VGH = 27V	-		416	mA
	IGL	VGL =-20V	-		1220	mA
	ICOM		-		4000	mA

Note:

1. The maximum power consumption is measured using 75Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)
2. The Typical average current for power consumption is measured using 75 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
3. The standby power is the consumed power when the panel controller is in standby mode.
4. The maximum power consumption is measured using 75Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines.
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-3).
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
5. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
6. Vcom is recommended to be set in the range of assigned value ± 0.1 V
7. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3024)
8. The maximum current is for reference only.

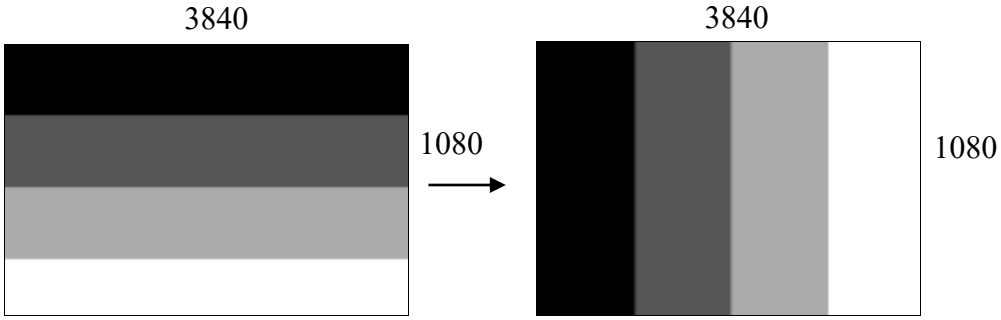
Note6-1

The maximum average current and Maximum Currents



Note6-2

The typical power consumption



Note6-3

The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
IDD	2.2uF x 14pcs / ±10%
IP1	2.2uF x 12pcs / ±10%
IP2	2.2uF x 12pcs / ±10%
IP3	2.2uF x 12pcs / ±10%
IN1	2.2uF x 12pcs / ±10%
IN2	2.2uF x 12pcs / ±10%
IN3	2.2uF x 12pcs / ±10%
IGH	2.2uF x 2pcs / ±10%
IGL	2.2uF x 3pcs / ±10%
ICOM	No Capacitor

6-3) Panel DC Characteristics for Device Battery-Life Estimation

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal Ground	VSS			0		V
Logic voltage Supply	VDD		2.7	3.3	3.6	V
	IDD	VDD=3.3V		30.88	36.84	mA
Gate Negative Supply	VGL		-21	-20	-19	V
	IGL	VGL=-20V		5.28	7.72	mA
Gate Positive Supply	VGH		26	27	28	V
	IGH	VGH=27V		2.41	2.49	mA
Source Negative Supply	VN1		-16	-15	-14	V
	IN1	VN1=15V		8.96	241.74	mA
Source Negative Supply	VN2		-13	-12	-11	V
	IN2	VN2=10V		0.43	0.89	mA
Source Negative Supply	VN3		-21	-20	-19	V
	IN3	VN3=20V		8.81	34.47	mA
Source Positive Supply	VP1		14	15	16	V
	IP1	VP1=-15V		5.51	239.79	mA
Source Positive Supply	VP2		11	12	13	V
	IP2	VP2=-10V		1.56	6.66	mA
Source Positive Supply	VP3		19	20	21	V
	IP3	VP3=-20V		0.68	12.98	mA
Border Supply	-		-	-	-	V
Asymmetry Source	Vasm	VP1+VN1	-800		800	mV
Common Voltage	VCOM		-3.5	Adjusted	-0.3	V
	ICOM			8.73	9.21	mA
Maximum Power panel	Pmax				8700	mW
Typical power panel	Ptyp			878		mW
Standby power panel	Pstby				60.2	mW

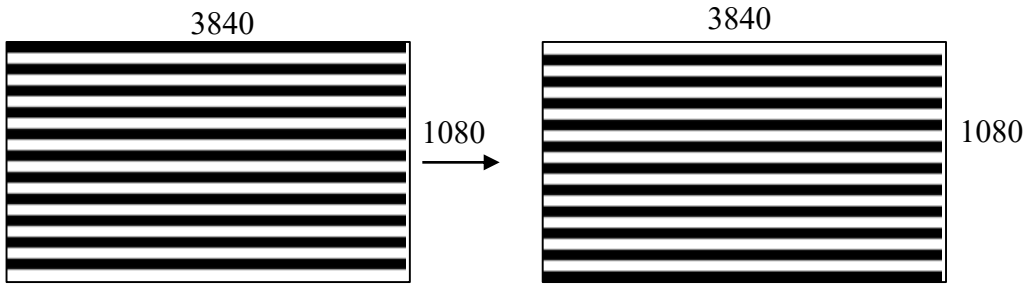
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents (Note 5)	IP1	VP1 = 15V	-		1500	mA
	IN1	VN1 = -15V	-		1540	mA
	IGH	VGH = 27V	-		416	mA
	IGL	VGL =-20V	-		1220	mA
	ICOM		-		4000	mA

Note:

1. The power consumption in this field is measured in whole updated time by 450ms (at 25 degree C) for device battery life estimation.
2. The maximum power consumption is measured using 75Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)
3. The Typical average current for power consumption is measured using 75 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
4. The standby power is the consumed power when the panel controller is in standby mode.
5. The maximum power consumption is measured using 75Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines.
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-3).
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
7. Vcom is recommended to be set in the range of assigned value ± 0.1 V
8. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3024)
9. The maximum current is for reference only.

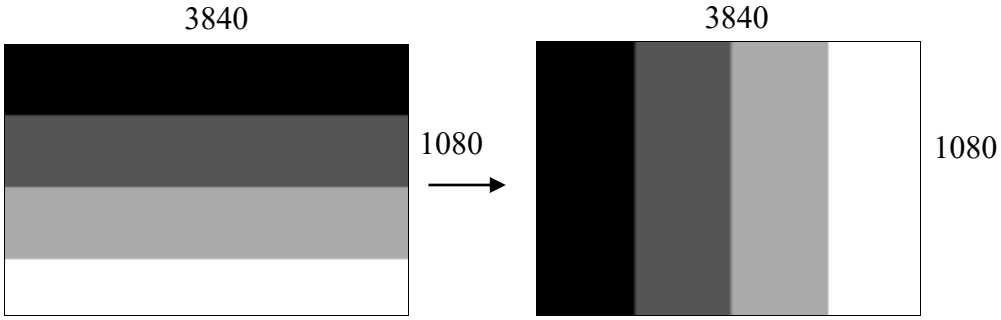
Note6-1

The maximum average current and Maximum Currents



Note6-2

The typical power consumption



Note6-3

The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
IDD	2.2uF x 14pcs / ±10%
IP1	2.2uF x 12pcs / ±10%
IP2	2.2uF x 12pcs / ±10%
IP3	2.2uF x 12pcs / ±10%
IN1	2.2uF x 12pcs / ±10%
IN2	2.2uF x 12pcs / ±10%
IN3	2.2uF x 12pcs / ±10%
IGH	2.2uF x 2pcs / ±10%
IGL	2.2uF x 3pcs / ±10%
ICOM	No Capacitor

6-4) Refresh Rate

The module ED280TT1 is applied at a maximum screen refresh rate of 75Hz.

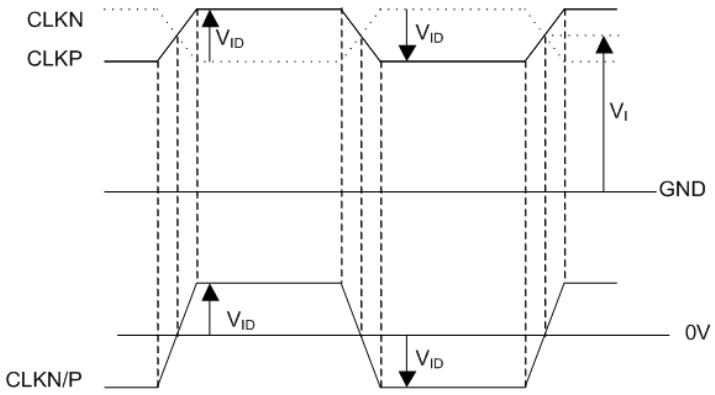
	Min	Max
Refresh Rate	-	75 Hz

6-5) Panel AC characteristics

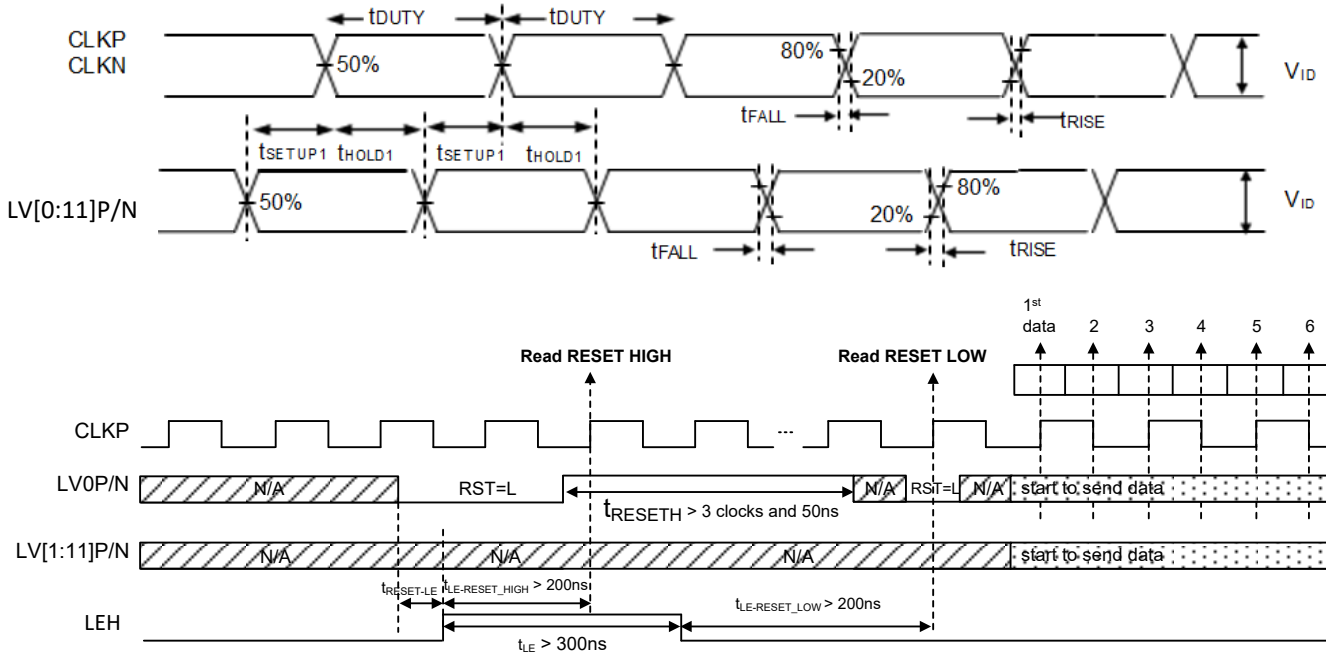
VDD=2.7V to 3.6V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit
mini-LVDS differential voltage	V_{ID}	300	-	-	mV
mini-LVDS common mode input voltage range	V_I	0.4	1.0	VDD-1.4	V
Source Clock frequency	F_{CLK}	-	-	150	MHz
Source Clock setup time	t_{SETUP1}	1.1	-	-	ns
Source Clock hold time	t_{HOLD1}	1.1	-	-	ns
Rise time	t_{RISE}	-	-	0.15	Unit interval
Fall time	t_{FALL}	-	-	0.15	Unit interval
LE rising to reset input time	$t_{LE\text{-}RESET\_HIGH}$	200	-	-	ns
LE falling to reset input time	$t_{LE\text{-}RESET\_LOW}$	200	-	-	ns
Reset high period	t_{RESETH}	3	-	-	CLK
Receiver off to LE timing	$t_{REC\text{-}OFF}$	40	-	-	CLK
LE width	t_{LE}	300	-	-	ns
Gate clock pulse high period	t_{CLKH}	500	-	-	ns
Gate clock pulse low period	t_{CLKL}	500	-	-	ns
Gate clock rise time	t_{IR_CLK}	-	-	100	ns
Gate clock fall time	t_{IF_CLK}	-	-	100	ns
Gate Start pulse setup time	t_{SU}	100	-	t_{CLKH}-100	ns
Gate Start pulse hold time	t_{HD}	100	-	t_{CLKL}-100	ns
Gate Start pulse rise time	t_{IR_STV}	-	-	100	ns
Gate Start pulse fall time	t_{IF_STV}	-	-	100	ns

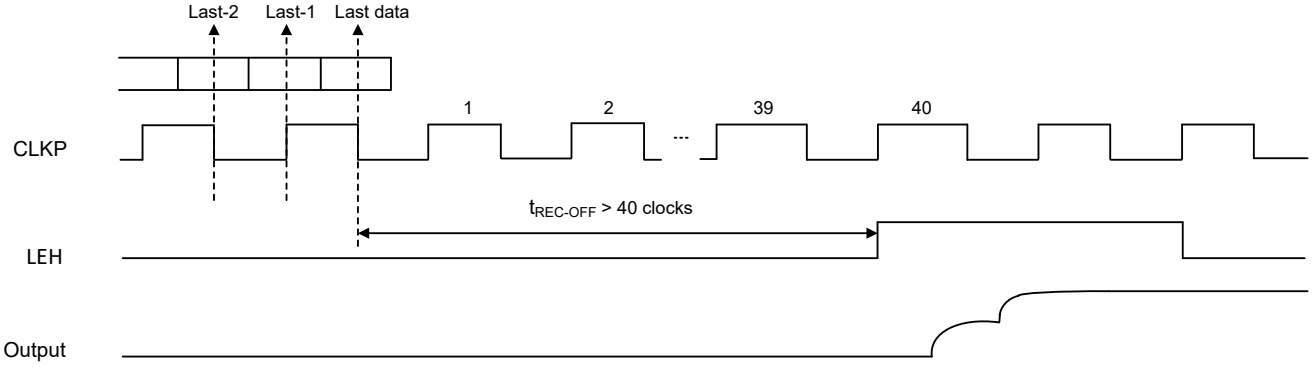
Mini-LVDS clock



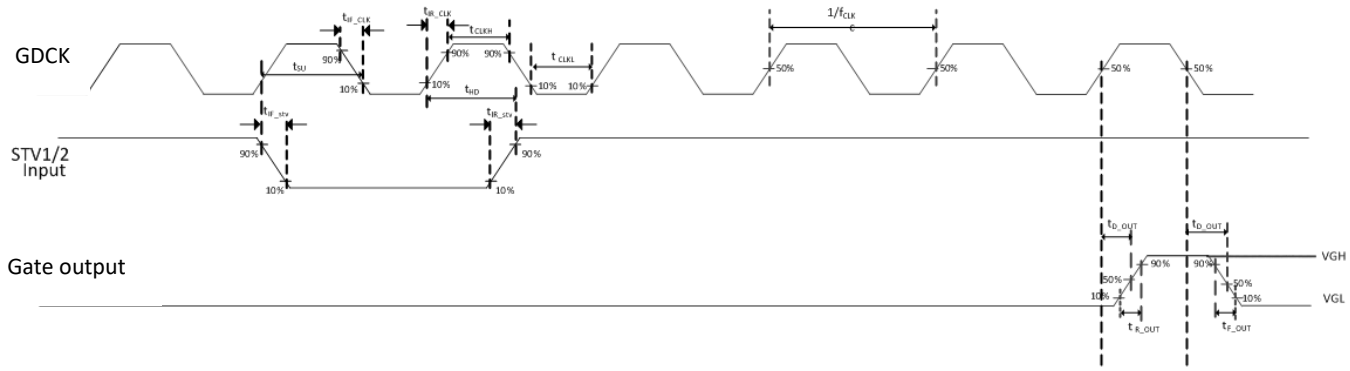
Mini-LVDS timing for receiving data



Mini-LVDS last data sampling to LE timing



GATE OUTPUT TIMING



Note：First gate line on timing
After 5CLK, Gate OUT1 is on.

6-6) Controllers Timing

The timing mode is depicted on Figure 6.1 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

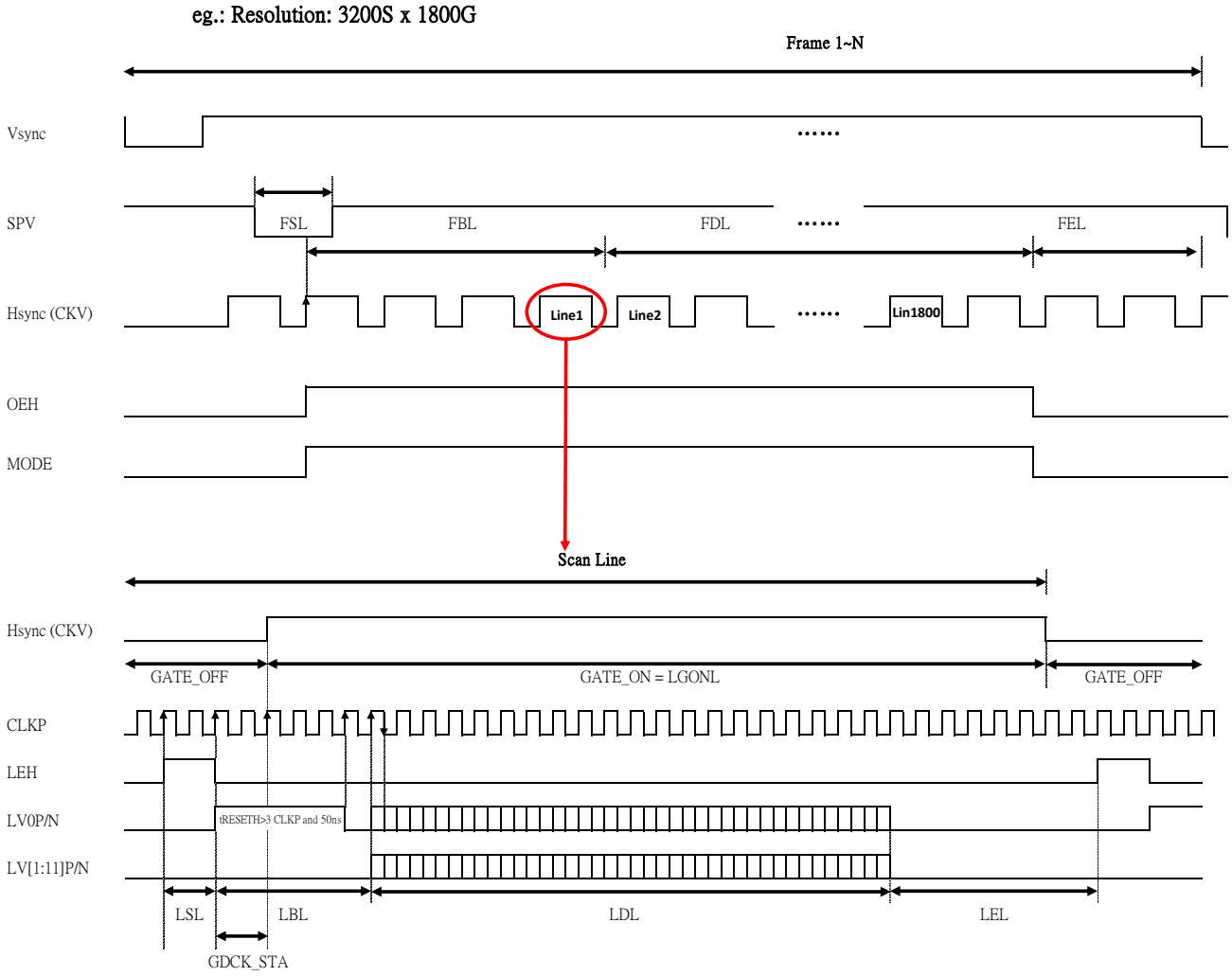


Figure 6.1 Timing in Mode 3

Note: LCK is an internal signal and it is shown for reference only.

Mode	3	Resolution				
SDCK [MHz]	48	3840 x 1080				
Pixels Per SDCK	8					
Line Parameters [SDCK]	LSL	LBL	LDL	LEL	GDCK _STA	LGONL
	15	15	480	79	1	466
Line Parameters [us]	0.31	0.31	10	1.65	0.02	9.71
Frame Parameters [lines]	FSL	FBL	FDL	FEL	-	FR [Hz]
	1	4	1080	1	-	75
Frame Parameters [us]	12.27	47.92	23090.4	11.38	-	-
					-	-

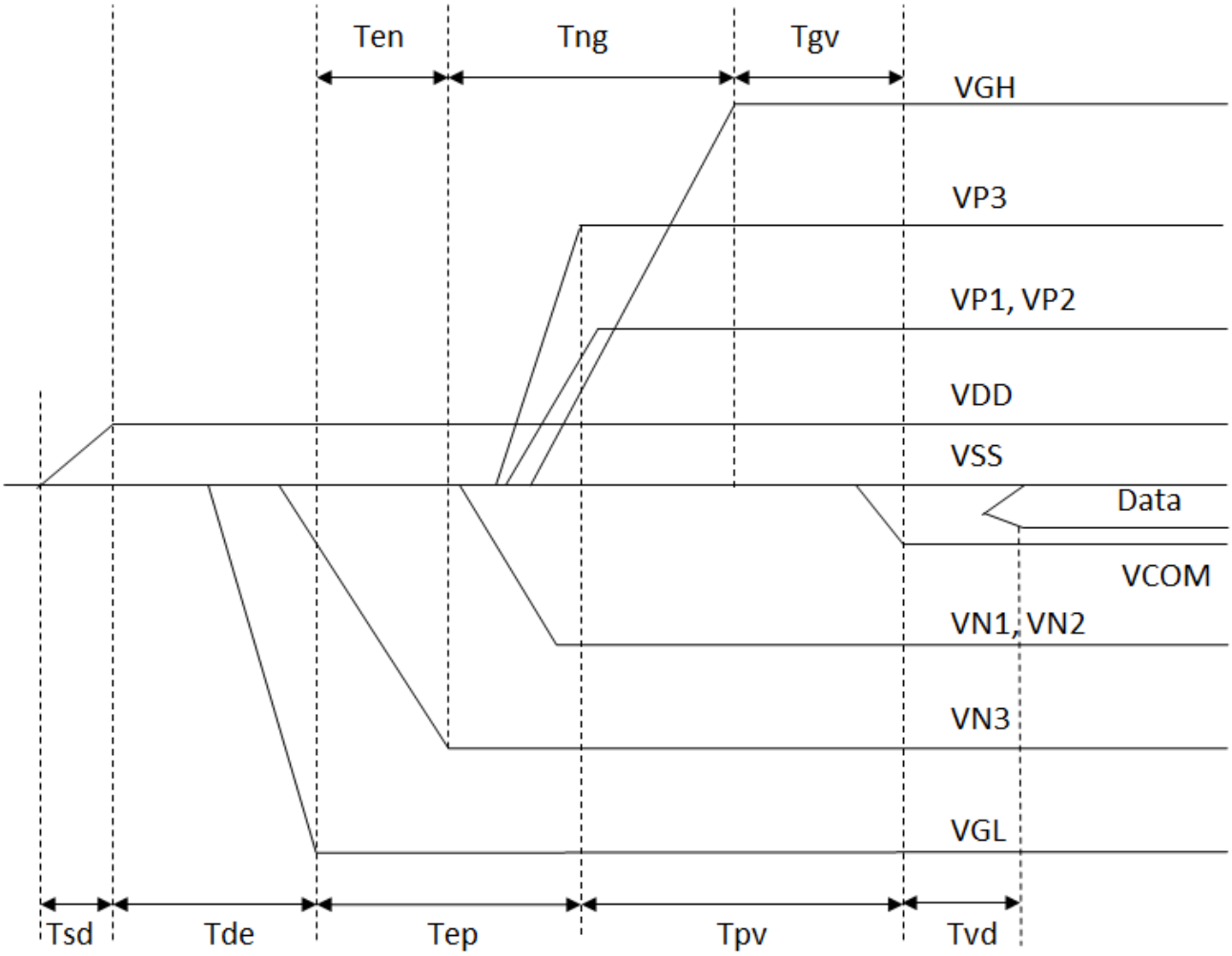
7. Power Sequence

Power Rails must be sequenced in the following order：

1. VSS → VDD → VN3 → VN1(VN2) → VP1(VP2) →VP3 → VCOM

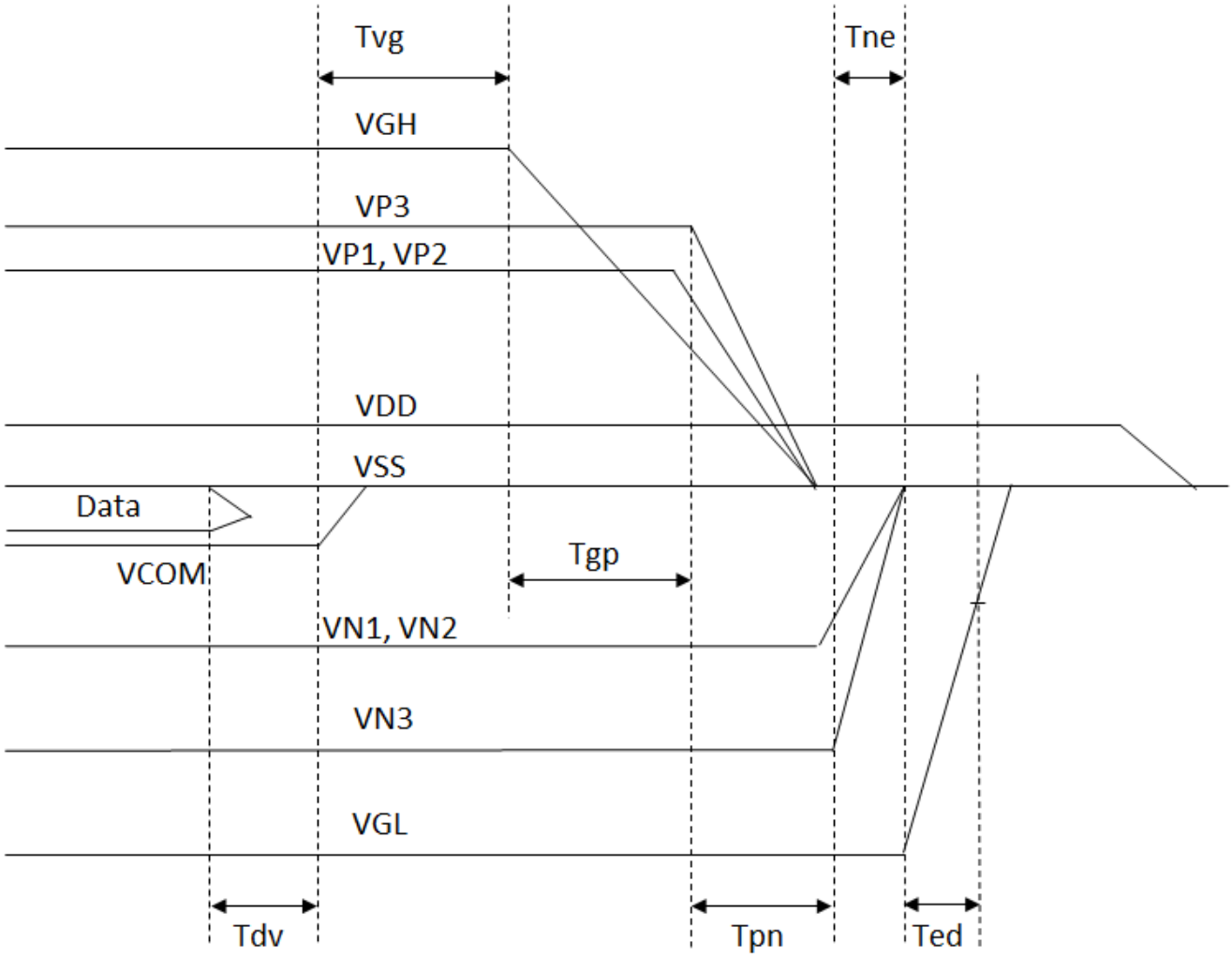
2. VSS → VDD → VGL → VGH (Gate driver)

POWER ON



	Min	Max	Remark
Tsd	30us	-	
Tde	100us	-	
Tep	1000us	-	
Tpv	100us	-	
Tvd	100us	-	
Ten	0us	-	
Tng	1000us	-	
Tgv	100us	-	

POWER OFF



	Min	Max	Remark
Tdv	100µs	-	-
Tvg	0µs	-	-
Tgp	0µs	-	-
Tpn	0µs	-	-
Tne	0µs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

8. Optical Characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25ºC

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	40	-	%	Note 8-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	12	-		

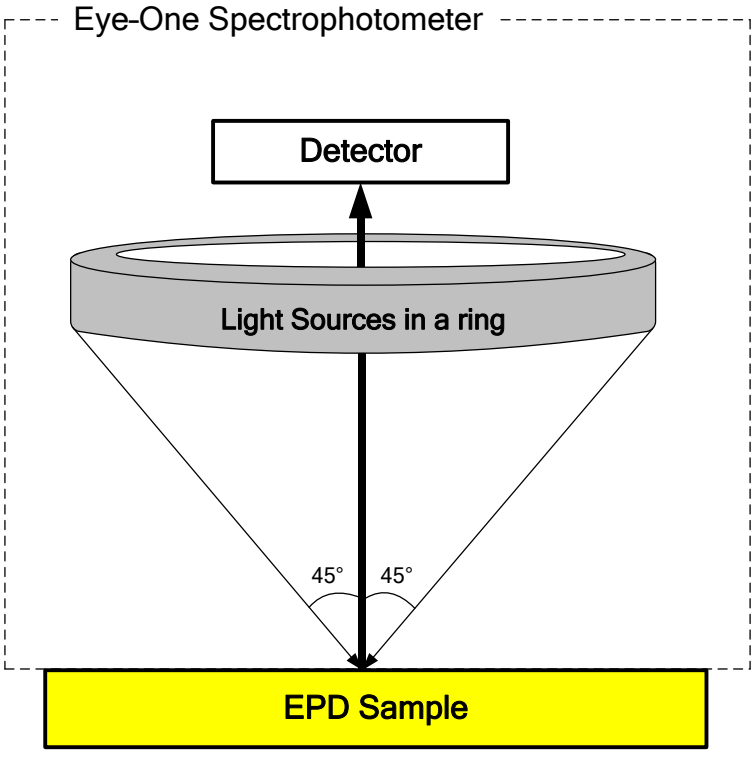
WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS

m:4、8、16　when 2、3、4 bits mode

Note 8-1: Luminance meter: Eye – One Pro Spectrophotometer

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl/Rd



8-3) Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor$_{white\ board}$ x (L_{center} / $L_{white\ board}$)

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
4) Acetic acid type and chlorine type materials for the cover case are not desirable because he former generates corrosive gas of attacking the PS at high temperature and the latter cause's circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.
Data sheet status
Product specification
This data sheet contains Preliminary product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other condition These are stress ratings only and operation of the device at these or at any other condition to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification

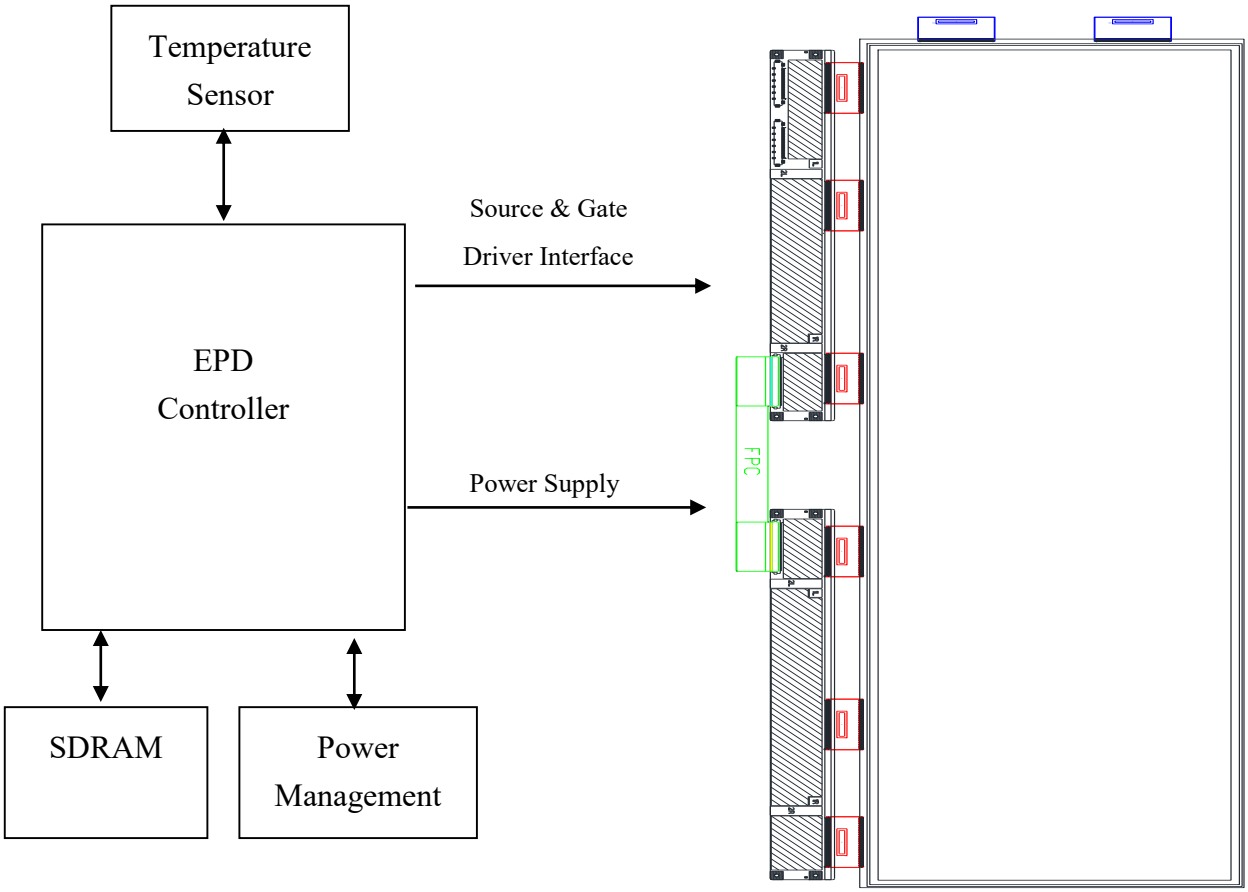
10 . Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +65°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = -15°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
	High-Temperature, High-Humidity Storage	T = +60°C, RH = 80% for 240 hrs	IEC 60 068-2-3CA	
6	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
7	Solar radiation test	765 W/m2,168hrs,40℃	IEC60 068-2-5Sa	
8	Package Vibration	Random Wave (1.5Grms) Frequency: 10~200Hz Direction: X,Y,Z Duration: 30mins each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 15.2 cm on concrete surface. Drop sequence: 6 flats	Full packed for shipment	
10	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	
11	Electrostatic Effect (non-operating)	(ESD gun) Air 15k, Contact 8k	IEC 62179, IEC 62180	

Actual EMC level to be measured on customer application
Note: The protective film must be removed before temperature test.

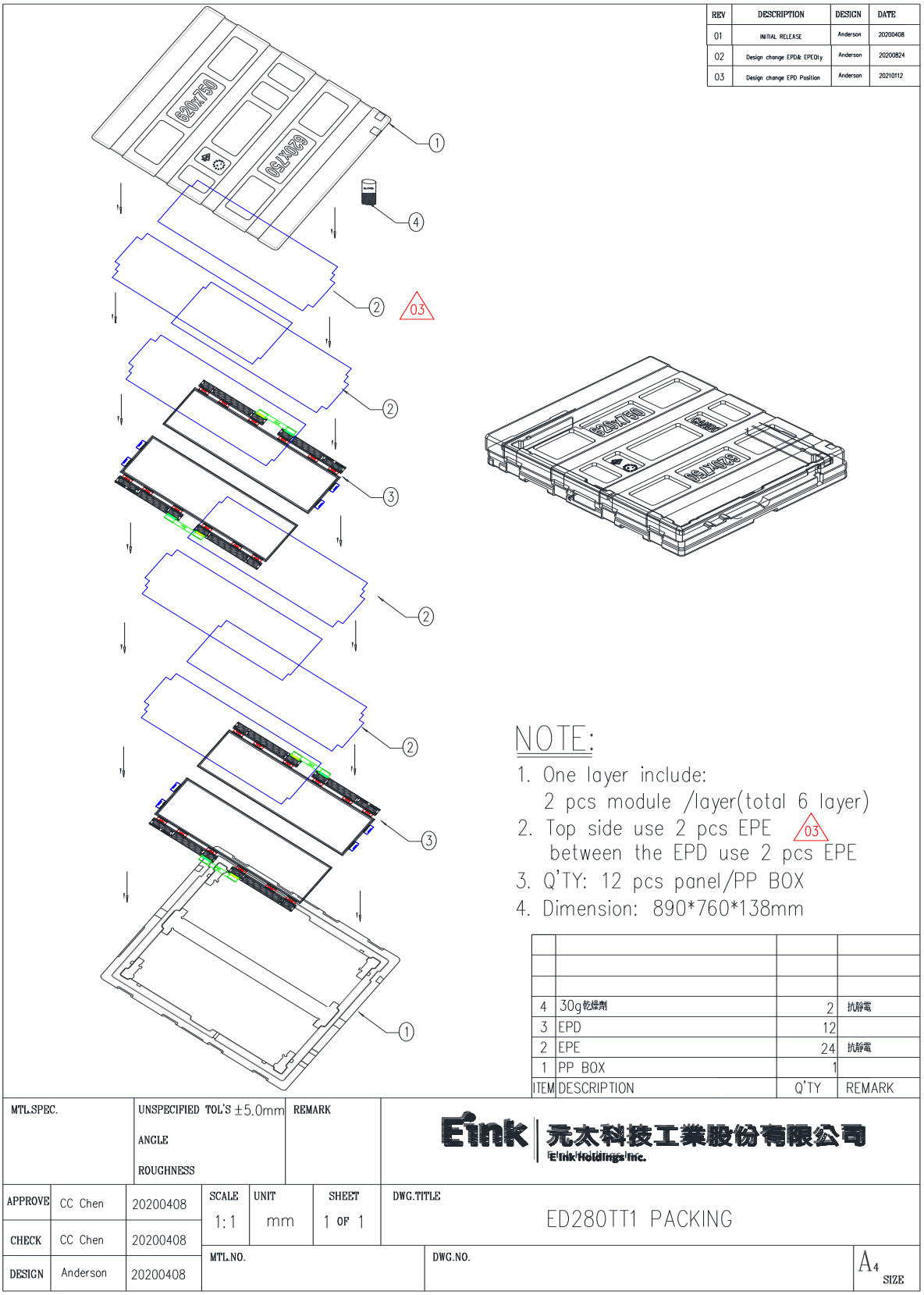
< Criteria >
In the standard conditions, there is not display function NG issue occurred. (Including: line defect, no image). All the cosmetic specification is judged before the reliability stress.

11. Block Diagram

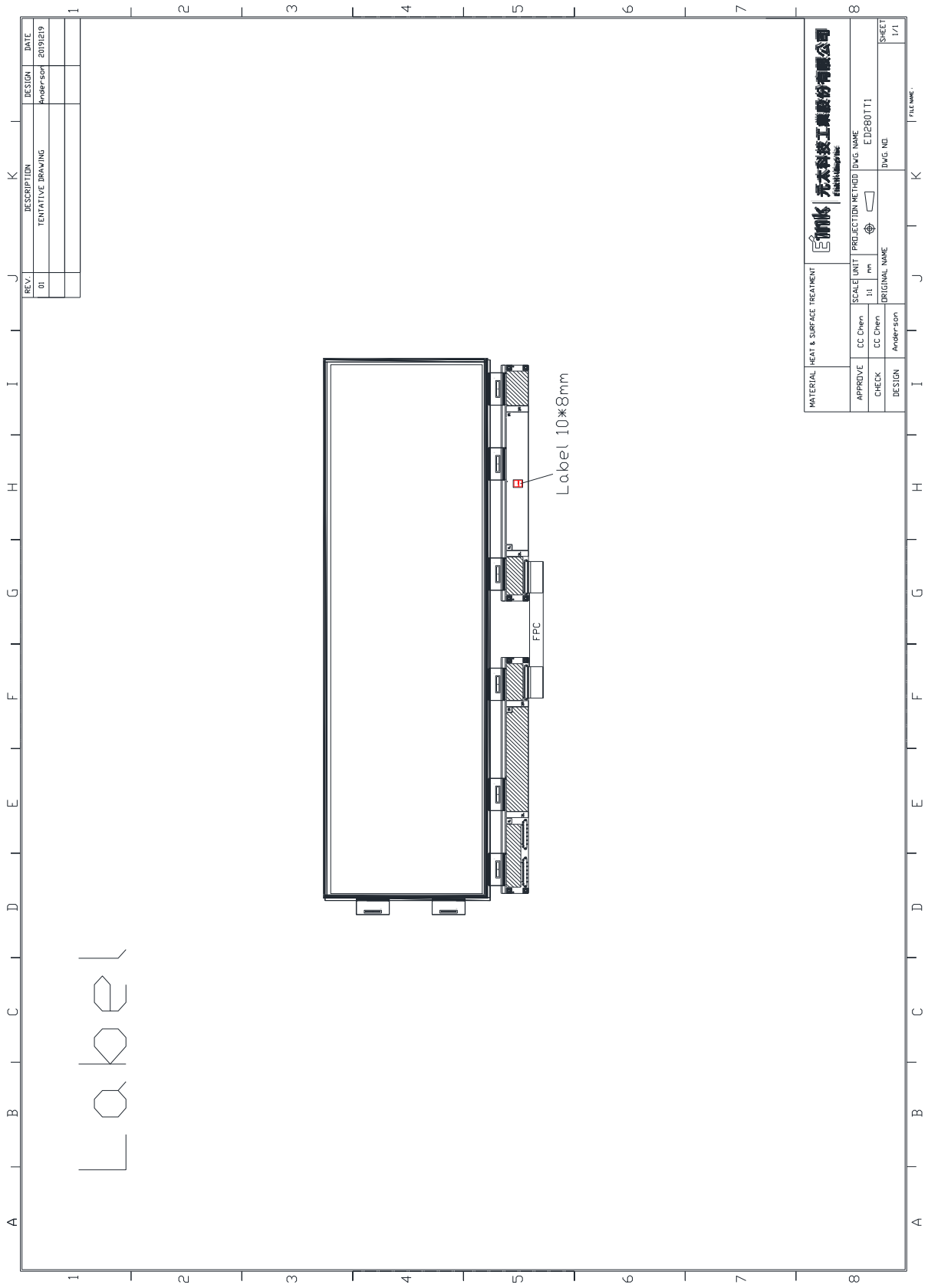


12. Packing

12-1) packing drawing

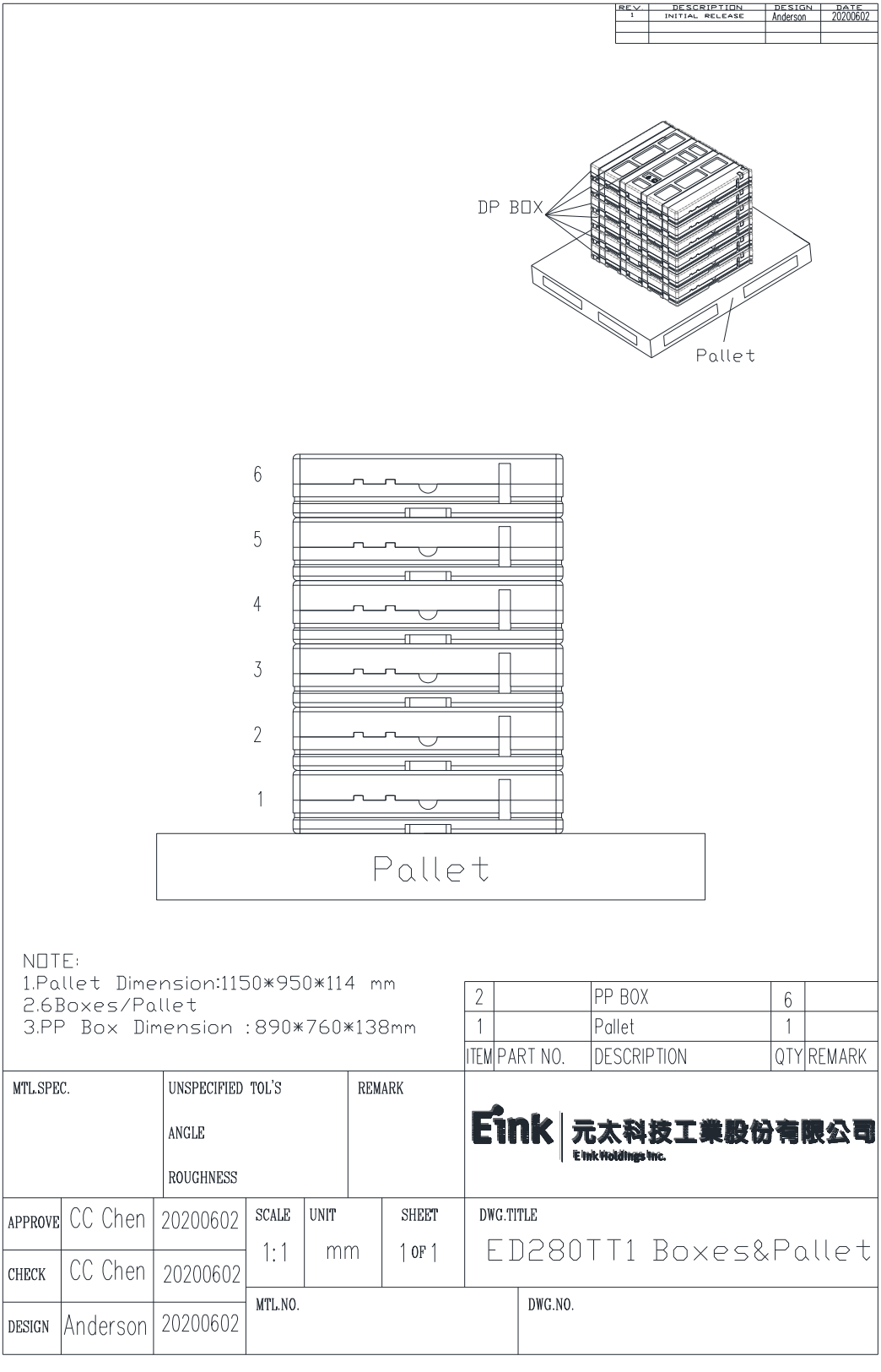


12-2) Label position



12-3) Pallet Stacking

Note: Stacking layer limitation: 6 layers.



13. Bar Code Definition

ET1	00	6	01	1	I	7	4	00361	A	T
1	2	3	4	2	5	6	2	7	2	8

1：EPD model code

2：Internal control codes

3：Internal control codes

4：Internal control codes

5：Year:

T:2018 / U:2019 / V:2020 / ... / Z: 2024

6：Month:

1:Jan. 2:Feb. ... 9:Sep. A:Oct. B:Nov. C:Dec.

7：Serial number

00000-99999

8：Internal control codes

14. Appendix:

For outdoor product please refer to details by followed documentations:

1. Outdoor Signage Design Recommendation
2. Signage Wide Temp. Support Requirement.

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