DATA MODUL

SPECIFICATION

ED028TC1

2.84”, 480x600, SPI

Version: 1.0
Date: 11.02.2019

Note: This specification is subject to change without prior notice

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Version: 1

TECHNICAL SPECIFICATION

MODEL NO: ED028TC1

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

Approved By kyle lee

Confirmed By kyle lee

Prepared By Justin Ji

Revision History

Rev.	Issued Date	Revised Contents
1	2019.02.11	Official issued.

TECHNICAL SPECIFICATION

CONTENTS

1. General Description

ED028TC1 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 2.84" active area with 480 x 600 pixels, the display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

2. Features

- High contrast reflective/ electrophoretic technology
- 480 x 600 dot resolution
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- All-in-one driver
- Commercial temperature range

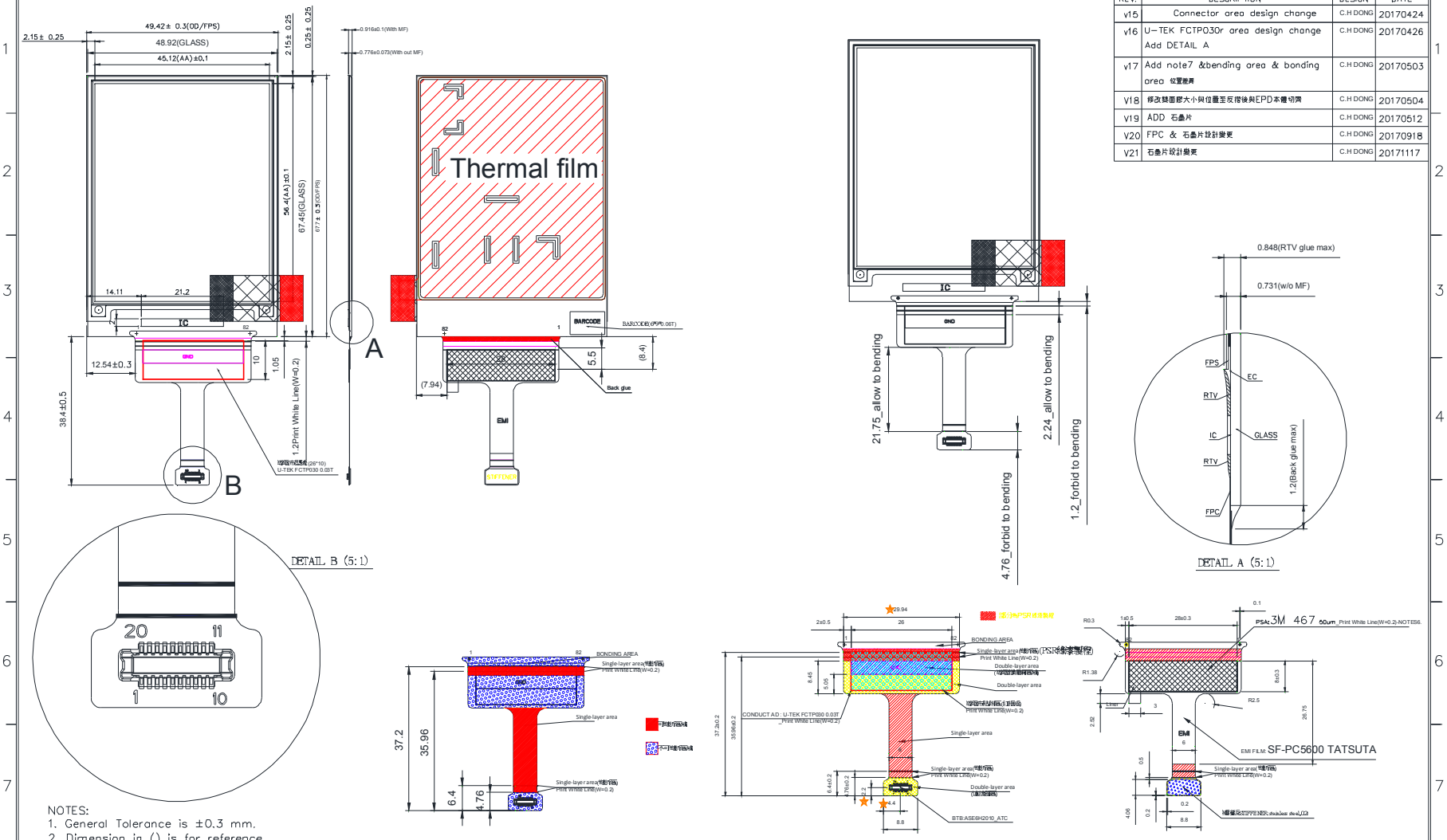
3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.84"	Inch	
Display Resolution	480(H) x 600(V)	Pixel	
Active Area	45.12 (H) × 56.4 (V)	mm	
Pixel Pitch	0.094 (H) × 0.094 (V)	mm	
Pixel Configuration	Square		
Outline Dimension	49.42 (W) × 67.7 (H) × 0.776 (D)	mm	
Module Weight	5.68	g	Note 3-1
Number of Gray	16 Gray Level (monochrome)		
Display operating mode	Reflective mode		

Note 3-1: No include protect film's masking film and thermal sheet's.

4. Mechanical Drawing of EPD Module

REV.	DESCRIPTION	DESIGN	DATE
v15	Connector area design change	C.H DONG	20170424
v16	U-TEK FCTP030r area design change Add DETAIL A	C.H DONG	20170426
v17	Add note7 &bending area & bonding area 位置差異	C.H DONG	20170503
V18	修改顯面積大小與位置至反摺後與EPD本體切齊	C.H DONG	20170504
V19	ADD 石墨片	C.H DONG	20170512
V20	FPC & 石墨片設計變更	C.H DONG	20170918
V21	石墨片設計變更	C.H DONG	20171117



NOTES:
1. General Tolerance is ±0.3 mm.
2. Dimension in () is for reference.
3. Barcode thickness: 0.06mm
4. If cover lens is needed, propose to design smaller visual area dimension than AA.
5. 4 corners of PS are weak, please handle these area with care
6. After FPC 1st time bent backward, please fix FPC on glass with PSA & don't have 2nd time FPC bent.
7. Able to pass 10 times for 90 & 180 bending on bending area. But please note don't to bend on bonding area over 1 time otherwise display will be abnormal.

MATERIAL	HEAT & SURFACE TREATMENT	E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.			
APPROVE	Patrick Lin	SCALE 1:1	UNIT mm	PROJECTION METHOD	DWG. NAME ED028TC1
CHECK	Patrick Lin	ORIGINAL NAME ED028TC1		DWG. NO. ED028TC1	SHEET 1/1
DESIGN	C.H DONG				

5. Input/Output Interface

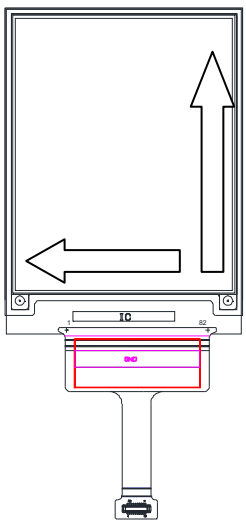
5-1) Connector type: ASE6H2010_ATC

5-2) Pin Assignment

Pin #	Signal	Description	Remark
1	BUSY_N	This pin indicates the driver status	
2	CSB	SPI chip select	
3	MOSI	SPI data input	
4	VCOM	VCOM output	
5	VSH	Positive source voltage	
6	GDR	This pin is N-MOS gate control	
7	VGL	Negative gate voltage	
8	VDDDO	Digital power output (1.8V)	
9	VDD	Digital voltage supply	
10	GND	Digital ground	
11	GND	Digital ground	
12	VDD	Digital voltage supply	
13	VDD	Digital voltage supply	
14	VSL	Negative source voltage	
15	FB	Keep open	Note 5.1
16	RESE	Current sense input for control loop	
17	VGH	Positive gate voltage	
18	MISO	SPI data output	
19	SCL	SPI clock input	
20	RST_N	Global reset pin	

Note 5.1: refer to Reference Circuit.

5-3) Panel Scan Direction



6. Electrical Characteristics

6-1) Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +6	V	--
Operating Temp. Range	TOTR	0 to 50	℃	--
Storage Temp. Range	TSTG	-25 to 70	℃	--

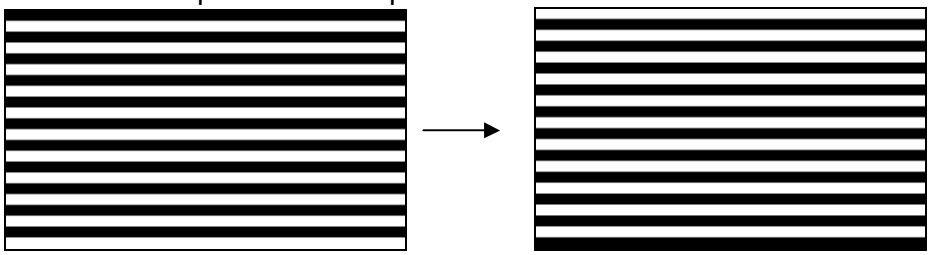
6-2) Panel DC Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	Vss		-	0	-	V
Logic voltage supply	Vdd		2.3	3.3	3.6	V
	Ivdd	Vdd=3.3V	-	17	245	mA
Common voltage Maximum Power panel	Vcom		-3.85	Adjusted	-0.52	V
Typical power panel	Ptyp		-	56	882	mW
Standby power panel	Pstby		-	-	0.2	mW

- The maximum power consumption is measured using 85 Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)
- The Typical power consumption is measured using 85 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink.

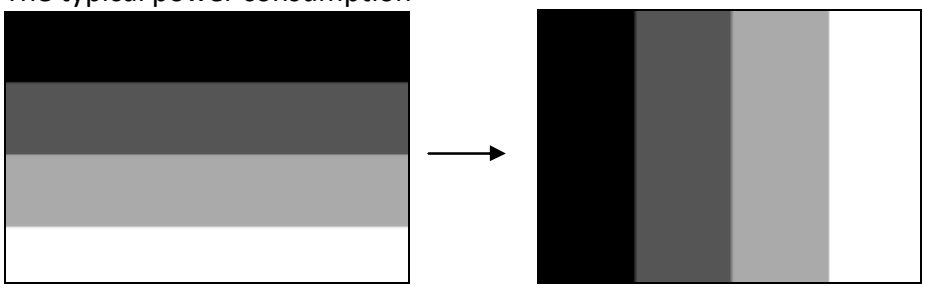
Note 6.1

The maximum power consumption



Note 6.2

The typical power consumption

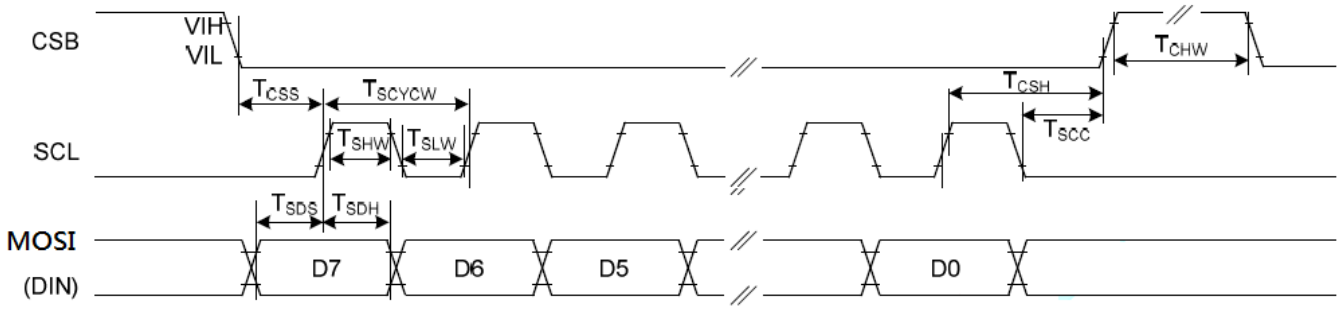


6-3) Panel AC characteristics

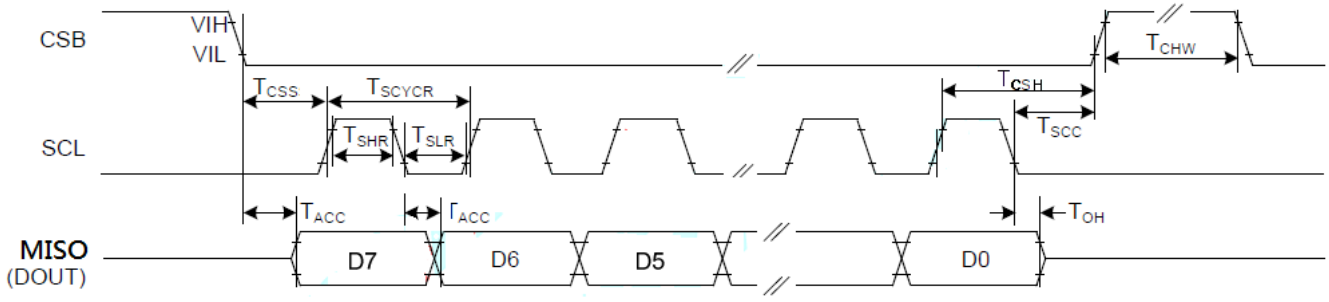
Symbol	Signal	Parameter	Min.	Typ.	Max.	Unit
Serial Communication						
t_{CSS}	CSB	Chip select setup time	20			ns
t_{CSH}		Chip select hold time	25			ns
t_{SCC}		SCL “L” to chip select “H”	10			ns
t_{CHW}		Chip select WIDTH	40			ns
t_{SCYCW}	SCL	Serial clock cycle (Write)	25/30/53 *Note 6.3			ns
T_{SHW}		SCL “H” pulse width (Write)	12			ns
t_{SLW}		SCL “L” pulse width (Write)	12			ns
t_{SCYCR}		Serial clock cycle (Read)	300			ns
T_{SHR}		SCL “H” pulse width (Read)	120			ns
t_{SLR}		SCL “L” pulse width (Read)	120			ns
t_{SDS}	MOSI	Data setup time	10			ns
t_{SDH}		Data hold time	10			ns
t_{ACC}	MISO	Access time	250			ns
t_{OH}		Output disable time	15			ns

Note 6.3: Command R10h and R12h take a long time to write to the SRAM. The following table is the tSCYCW between DM SPI and Nbpp.

DM	0(Normal mode)		1(Fast mode)	
SPIWM	0(1bit)	0(2bit)	0(1bit)	0(2bit)
1-bpp	53 ns	--	30 ns	53 ns
2-bpp	30 ns	53 ns	30 ns	30 ns
3-bpp	30 ns	30 ns	30 ns	30 ns
4-bpp	30 ns	30 ns	30 ns	30 ns



Serial Interface Characteristics (Write mode)



Serial Interface Characteristics (Read mode)

6-4) Refresh Rate

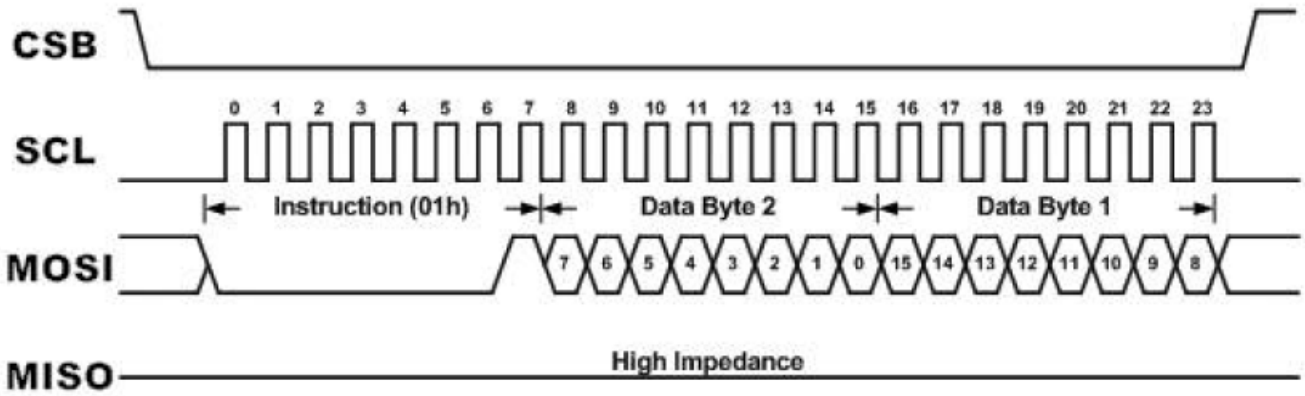
The module is applied at a maximum refresh rate of 85 Hz.

	Min	Max
Refresh Rate	-	85 Hz

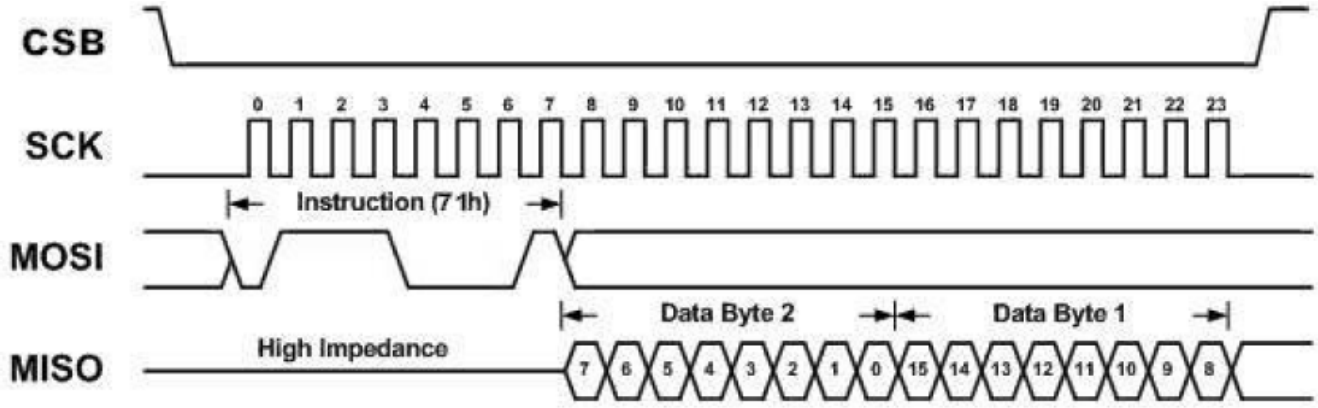
6-5) Controller Timing

SPI COMMAND

Standard SPI



Interface of standard SPI Write

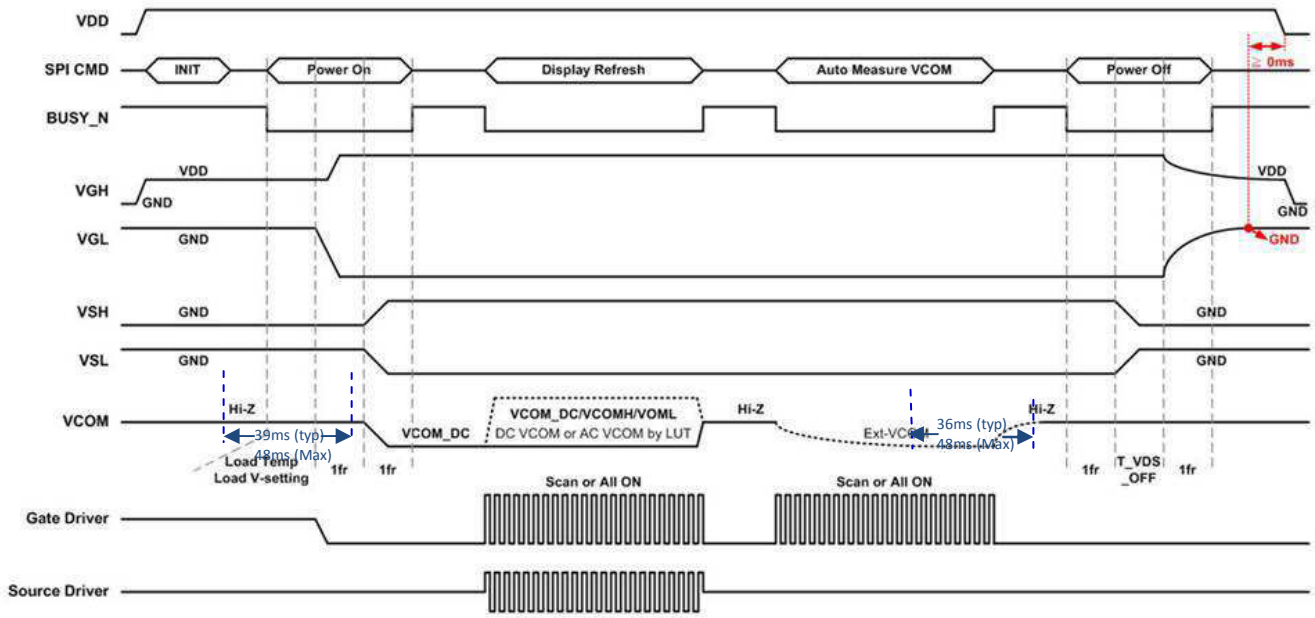


Interface of standard SPI Read

*CSB must be “L’’ between data and command in standard SPI mod

7. Power Sequence

7-1) POWER ON OFF

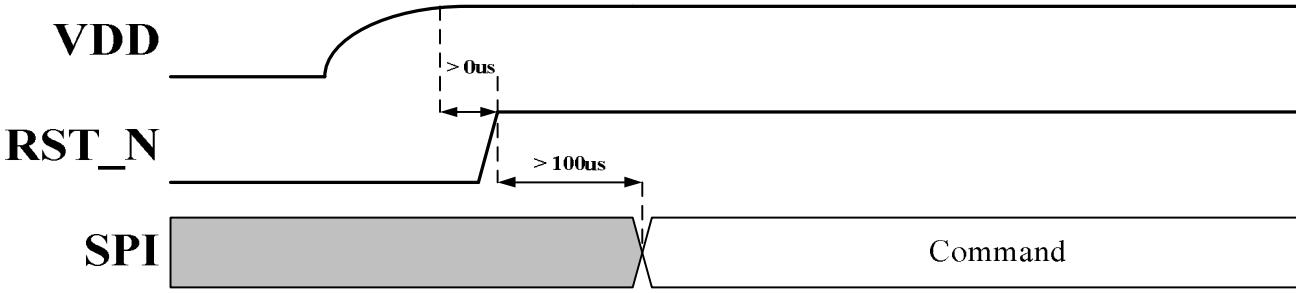


Note 7.1: VDD should be turned off after VGL have been turned off and returned to the ground state.
Note 7.2: R02 to VDD off time setting (reference only),

- T_VDS_OFF=0 , 100ms
- T_VDS_OFF=1 , 110ms
- T_VDS_OFF=2 , 120ms
- T_VDS_OFF=3 , 130ms

Note 7.3: When ED028TC1 with inner power charged-pump and under condition of frame rate 85Hz (around 12ms), total power-on period is 39ms (typ) / 48ms (Max), and total power-off period is 36ms (typ) / 48ms (Max). Theses data are measured by E Ink driving board, and may be changed by SPI command, outer circuit design, and passive components characteristic.
Note 7.4: During power-off sequence, keep VGH value greater than VSH, VGL value less than VSL, It means that VGH / VGL are highest voltage / lowest voltage. Then surely discharge VGH / VSH / VSL / VGL to GND before power-on.

7-2) Reset Sequence



8. Command Table

W/R: 0: Write Cycle 1: Read Cycle
C/D: 0: Command / 1: Data
D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	ED028TC1 Command	Registers	Defult (IC)
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0	00h		00h
		0	1	--	#	#	#	--	#	#	#	25h	RES0, LUT_SEL, DM, SHL, SPIWM, RST_N	05h
		0	1	--	--	--	--	--	--	--	--	00h		00h
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1	01h		01h
		0	1	--	--	--	--	--	--	#	#	03h	Vgate_EN, Vsource_EN	03h
		0	1	--	--	--	--	--	#	#	#	04h	VG_LVL[2:0]	02h
		0	1	--	#	#	#	#	#	#	#	00h	VSLV_LVL[6:0]	06h
		0	1	--	--	--	--	#	#	#	#	00h	VSL_LVL[1:0], VSH_LVL[1:0]	00h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0	02h		02h
4	Power OFF Sequence Setting(PFS)	0	0	0	0	0	0	0	0	1	1	03h		03h
		0	1	--	--	#	#	--	--	--	--	03h	T_VDS_OFF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0	04h		04h
6	Deep Sleep (DSLP)	0	0	0	0	0	0	0	1	1	0	06h		06h
		0	1	--	--	--	--	--	--	#	0	00h	DSLP	00h
7	Booster Soft Start (BTST)	0	0	0	0	0	1	0	0	0	0	07h		07h
		0	1	#	#	#	#	#	#	#	#	EFh	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	EFh	BT_PHB[7:0]	17h
		0	1	--	--	#	#	#	#	#	#	28h	BT_PHC[5:0]	17h
8	Data Start Transmission 1 (DTM1,current image data) ((M+2)-byte command)	0	0	0	0	0	1	0	0	0	0	10h		10h
		0	1	--	--	--	--	--	--	#	#	00h	CURR_BPP[1:0]	00h
		0	1	#	#	#	#	#	#	#	#	00h	Pixel1[3:0], Pixel2[3:0]	00h
		0	1	:	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	00h	Pixel(2M-1)[3:0], Pixel(2M)[3:0]	00h
9	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0	12h		12h
		0	1	--	#	#	#	#	#	--	--	08h	Waveform_mode[2:0], UPD_CPY_TO_PRE, DN_EN,	08h
		0	1	--	--	--	--	--	--	#	#	00h	X[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	00h		00h
		0	1	--	--	--	--	--	--	#	#	00h	Y[9:0]	00h

		0	1	#	#	#	#	#	#	#	#	00h		00h
		0	1	--	--	--	--	--	--	#	#	00h	W[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	00h		00h
		0	1	--	--	--	--	--	--	#	#	00h	L[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	00h		00h
10	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0	30h		30h
		0	1	--	--	0	0	--	--	--	0	0Eh		0Eh
11	Display Start transmission 2 (DTM2,previous image data) ((M+2)-byte command)	0	0	0	0	0	1	0	0	1	1	13h		13h
		0	1	--	--	--	--	--	--	#	#	00h	PRE_BPP[1:0]	00h
		0	1	#	#	#	#	#	#	#	#	00h	Pixel1[3:0], Pixel2[3:0]	00h
		0	1	:	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	00h	Pixel(2M-1)[3:0], Pixel(2M)[3:0]	00h
12	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0	40h		40h
		1	1	#	#	#	#	#	#	#	#	00h	D[10:3] / TS[8:1]	00h
		1	1	#	#	#	--	--	--	--	--	00h	D[2:0] / {TS[0], -, -}	00h
13	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1	41h		41h
		0	1	#	#	--	#	#	#	#	#	00h	TSE[1:0], TO[4:0]	00h
		0	1	#	#	#	#	#	#	#	#	1Ah	TEMP_VALUE[7:0]	1Ah
14	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0	50h		50h
		0	1	--	--	--	--	#	#	#	#	01h		01h
		0	1	#	#	#	#	#	#	#	#	22h		99h
15	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0	60h		60h
		0	1	#	#	#	#	#	#	#	#	3Fh	S2G [7:0]	08h
		0	1	#	#	#	#	#	#	#	#	09h	G2S [7:0]	08h
		0	1	#	#	#	#	#	#	#	#	2Dh	GHP [7:0]	08h
16	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1	61h		61h
		0	1	--	--	--	--	--	--	#	#	02h	HRES[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	60h		
		0	1	--	--	--	--	--	#	#	#	01h	VRES[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	E0h		
17	Auto Measurement Vcom (AMV)	0	0	1	0	0	0	0	0	0	0	80h		80h
		0	1	--	#	#	#	#	#	#	#	50h	CM_EN, AMVT[1:0], AMVX, AMVS, AMV, AMVE	50h
18	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1	81h		81h
		1	1	--	#	#	#	#	#	#	#	00h	VV[6:0]	00h
19	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0	82h		82h
		0	1	--	#	#	#	#	#	#	#	18h	VDCS[6:0]	18h

20	Data start Transmission Window (DTMW)	0	0	1	0	0	0	0	0	1	1	83h		83h
		0	1	--	--	--	--	--	--	#	#	00h	X[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	00h		
		0	1	--	--	--	--	--	--	#	#	00h	Y[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	00h		
		0	1	--	--	--	--	--	--	#	#	02h	W[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	58h		
		0	1	--	--	--	--	--	--	#	#	01h	L[9:0]	00h
		0	1	#	#	#	#	#	#	#	#	E0h		
21	GD Order Setting (GDOS)	0	0	1	1	1	0	0	0	0	0	E0h		E0h
		1	1	--	--	--	--	--	#	#	#	02h	GDOS[2:0]	00h
		0	1	1	1	1	1	1	1	1	1	FFh		FFh

8-1) Command description

W/R: 0: Write Cycle 1: Read Cycle

C/D: 0: Command / 1: Data

D7~D0: –: Don't Care #: Valid Data

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00h
	0	1	-	RES0	LUT_SEL	DM	-	SHL	SPIWM	RST_N	05h
	0	1	-	-	-	-	-	-	-	-	00h

RES0: Display Resolution setting (source x gate)

0b: 960x540 (Default)
1b: 800x600

LUT_SEL: LUT selection

0: Using LUT from external Flash.
1: Using LUT from register.

DM: Dither mode or not

0: Normal mode, (Default)
Internal storage will always be in 4bpp, if host writes image format other than 4bpp, the driver IC will still store the image in 4bpp.
1: Fast mode,
Internal storage will always be in 2bpp. If the host transfers image format in 3/4bpp, users can choose to dither it to 2bpp or not. If the host transfers 1 bpp, the driver IC will store the data in 2 bpp automatically.

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn → Sn-1 → Sn-2 → Sn-3 → … → S0

1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1 → Sn

SPIWM: SPI pixel Write Mode

0: SPI 1-bit wirte mode. (Default)

1: SPI 2-bit write mode. (Default) Can NOT be used in the DM=0 and 0-bpp mode.

RST_N: Soft Reset

0: The controller is reset. All registers will be set to their default value.
1: No effect (Default). Normal operation.

When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

Notes:

When RST_N becomes low, the driver will be reset and all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will stay as previous condition, 0V or floating.

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01h
	0	1	-	-	-	-	-	-	VGate_EN	Vsource_EN	03h
	0	1	-	-	-	-	-	VG_LVL[2:0]			02h
	0	1	-	VSLV_LVL[6:0]							06h
	0	1	-	-	-	-	VSL_LVL[1:0]		VSH_LVL[1:0]		00h

VSource_EN: VSource power selection
0: External source power from VSH and VSL pins
1: Inetrnal DC/DC function for generating source power. (Default)

VGate_EN: VGate power selection
0: External gate power from VGH/VGL pins
1: Internal DC/DC function for generating VGH/VGL (Default)

VG_LVL[2:0]: VGH / VGL Voltage Level selection.

VG_LVL	VG_LVL Voltage Level
000	VGH=17V, VGL= -17V
001	VGH=18V, VGL= -18V
010	**VGH=19V, VGL= -19V (Default)**
011	VGH=20V, VGL= -20V
100	VGH=21V, VGL= -21V

VSLV_LVL[6:0]: Internal VSLV_LVL power selection. (**Default value: 3.0V**)

VSLV_LVL	Voltage	VSLV_LVL	Voltage	VSLV_LVL	Voltage	VSLV_LVL	Voltage
000 0000	2.4 V	000 1100	3.6 V	011 1000	8.0 V	111 0100	14.0 V
000 0001	2.5 V	000 1101	3.7 V	:	:	:	:

000 0010	2.6 V	000 1110	3.8 V	100 0010	9.0 V	111 1110	15.0 V
000 0011	2.7 V	000 1111	3.9 V	:	:	111 1111	15.0 V
000 0100	2.8 V	001 0000	4.0 V	100 1100	10.0 V		
000 0101	2.9 V	:	:	:	:		
000 0110	**3.0 V**	001 1010	5.0 V	101 0110	11.0 V		
000 0111	3.1 V	:	:	:	:		
000 1000	3.2 V	010 0100	6.0 V	110 0000	12.0 V		
000 1001	3.3 V	:	:	:	:		
000 1010	3.4 V	010 1110	7.0 V	110 1010	13.0 V		
000 1011	3.5 V	:	:	:	:		

VSL_LVL[1:0], VSH_LVL[1:0]: VSL_LVL, VSH_LVL power selction for source voltage adjustment.

VSL_LVL, VSH_LVL	VSL, VSH Voltage Level
00	**VSH=15V, VSL= -15V (Default)**
01	VSH=14V, VSL= -14V
10	VSH=13V, VSL= -13V
11	VSH=12V, VSL= -12V

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	02h

After the Power OFF command, driver will power off following the power off sequence, and BUSY_N signal will become “0”.

The Power OFF command will turn OFF DCDC, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD OFF.

SD output and VCOM will remain as its previous condition: 0V or floating.

(4) POWER OFF SEQUENCE SETTING(PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	03h
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00h

T_VDS_OFF[1:0]: Source to Gate power OFF interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	04h

After the Power ON command, the driver will be powered ON following the Power ON Sequence. After the Power ON command and when all power sequence are ready, the BUSY_N signal will become “1”.

(6) DEEP SLEEP (DSLP) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	06h
	0	1	-	-	-	-	-	-	DSLP	**0**	00h

After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset.

DSLP: 1: to enter deep sleep mode.

(7) BOOSTER SOFT START (BTST) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Warm start Booster	0	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	07h
	0	1	BT_PHA[7:0]								17h
	0	1	BT_PHB[7:0]								17h
	0	1	-	-	BT_PHC[5:0]						17h

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 010b: strength 3 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS 111b: 6.58uS

(8) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	10h
	0	1	-	-	-	-	-	-	Cur_BPP[1:0]		00h
	0	1	Pixel1[3:0]				Pixel2[3:0]				00h
	0	1	:				:				00h
	0	1	Pixel(2M-1)[3:0]				Pixel(2M)[3:0]				00h

The register is indicates that user start to transmit data. Then write to current image SRAM. While complete data transmission, user must send command 11H. Then chip will start to send data/VCOM for panel.

Cur_BPP[1:0]: bits per pixel

00b: 1bpp
Byte 3~2M:

D7	D6	D5	D4	D3	D2	D1	D0
Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8

01b: 2bpp
Byte 3~2M:

D7	D6	D5	D4	D3	D2	D1	D0
Pixel 1 [1:0]		Pixel 2 [1:0]		Pixel 3 [1:0]		Pixel4 [1:0]	

10b: 3bpp
Byte 3~2M:

D7	D6	D5	D4	D3	D2	D1	D0
-	Pixel 1 [2:0]			-	Pixel 2 [2:0]		

11b: 4bpp
Byte 3~2M:

D7	D6	D5	D4	D3	D2	D1	D0
Pixel 1 [3:0]				Pixel 2 [3:0]			

(9) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display (10-byte command)	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	12h
	0	1	-	Waveform_mode[2:0]			UPD_CPY_TO_PRE	DN_EN	-	-	08h
	0	1	-	-	-	-	-	-	X[9:8]		00h
	0	1	X[7:0]								00h
	0	1	-	-	-	-	-	-	Y[9:8]		00h
	0	1	Y[7:0]								00h
	0	1	-	-	-	-	-	-	W[9:8]		00h
	0	1	W[7:0]								00h
	0	1	-	-	-	-	-	-	L[9:8]		00h
	0	1	L[7:0]								00h

This command will make the driver refresh display (data/VCOM) according to SRAM data and LUT.

After this command, BUSY_N signal will become “0”.

Waveform_mode[2:0]: Waveform mode selection

001b: mode 1

UPD_CPY_TO_PRE:

0: current image buffer did not copy to previous image buffer after update
1: current image buffer was copied to previous image buffer after update

DN_EN:

0: Data follow VCOM function disable.
1: If the pixel from “New data” SRAM equals to “Old data” SRAM on display area, this pixel output would follow VCOM LUT.

X[9:0], Y[9:0], W[9:0], L[9:0]: define the window when updating the image to panel.

(X,Y) is the origin of the window, while W and L indicate Width and Length (height) of the window, respectively.

This command only active when BUSY_N = “1”.

(10) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30h
	0	1	-	-	0	0	-			0	0Eh

The command decides internal OSC clock frequency.

(11) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	13h
	0	1	--	--	--	--	--	--	Pre_BPP[1:0]		00h
	0	1	Pixel1[3:0]				Pixel2[3:0]				00h
	0	1	:				:				00h
	0	1	Pixel(2M-1)[3:0]				Pixel(2M)[3:0]				00h

The register is indicates that user start to transmit data. Then write to previous image SRAM. While complete data transmission, user must send command 11H. Then chip will start to send data/VCOM for panel.

Pre_BPP[1:0]: bits per pixel

00b: 1bpp

Byte 3~2M:	D7	D6	D5	D4	D3	D2	D1	D0
	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8

01b: 2bpp

Byte 3~2M:	D7	D6	D5	D4	D3	D2	D1	D0
	Pixel 1 [1:0]		Pixel 2 [1:0]		Pixel 3 [1:0]		Pixel4 [1:0]	

10b: 3bpp

Byte 3~2M:	D7	D6	D5	D4	D3	D2	D1	D0
	--	Pixel 1 [2:0]			--	Pixel 2 [2:0]		

11b: 4bpp

Byte 3~2M:	D7	D6	D5	D4	D3	D2	D1	D0
	Pixel 1 [3:0]				Pixel 2 [3:0]			

(12) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40h
	1	1	D10/TS8	D9 / TS7	D8 / TS6	D7 / TS5	D6 / TS4	D5 / TS3	D4 / TS2	D3 / TS1	00h
	1	1	D2 / TS0	D1	D0	-	-	-	-	-	00h

This command represents temperature value. The first byte indicates integer degree-C and second byte indicates a decimal fraction.

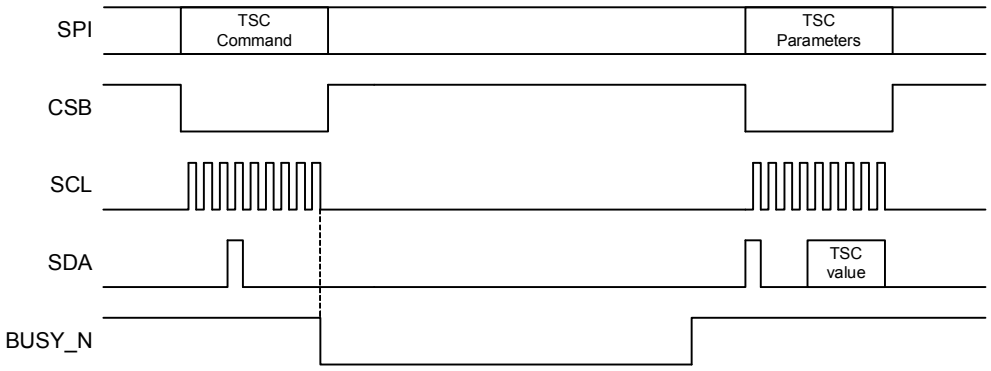
TS[8:0] is available when TSE (Bits D7~D6 of command R41h) set to 00b.
D[10:0] is available when TSE (Bits D7~D6 of command R41h) set to 10b.

TS[8:0]: internal temperature sensor value

TS[8:0]	Temperature (^{o}C)
1 1011 0000	-40
:	:
1 100 1110	-25
:	:
1 1111 1110	-1
1 1111 1111	-0.5
0 0000 0000	0
0 0000 0001	0.5
0 0000 0010	1
0 0000 0011	1.5
:	:
0 0110 0100	50
:	:
0 1010 1110	87
0 1010 1111	87.5

D[10:0]: external LM75 temperature sensor value

BUSY_N become low after TSC command. When BUSYN become high, Parameter can be read.



(13) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41h
	0	1	TSE[1:0]		-	TO[4:0]					00h
	0	1	TEMP_VALUE[7:0]								1ah

This command indicates the driver IC temperature sensor enable and calibration function.

TSE[1:0]: Internal temperature sensor switch

00: Enable (default)

10: Disable; using external sensor. 01b, 11b: Using TEMP_VALUE[7:0] (unit: 1 °C)

TO[4:0]: Temperature offset. If set TO[4:0] value, read TS[8:0] will added TO[4:0], TO[4:0] use 2's complement.

TEMP_VALUE[7:0]: Host-forced temperature value.

(14) Vcom and Data Interval Setting (CDI) (R50h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between Vcom and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	-	-	-	-	-	-	-	-	01h
	0	1	-	-	-	-	-	-	-	-	99h

This command indicates the interval of VCOM and data output.

(15) TCON Setting (TCON) (R60h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	60h
	0	1	-	-	-	-	-	-	-	-	08h
	0	1	-	-	-	-	-	-	-	-	08h
	0	1	-	-	-	-	-	-	-	-	08h

This command defines non-overlap period of Gate and Source.

(16) Resolution Setting (TRES) (R61h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61h
	0	0	-	-	-	-	-	-	VRES[9:8]		00h
	0	1	HRES[7:0]								00h
	0	1	-	-	-	-	-	-	VRES[9:8]		00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[9:0]: Horizontal Display Resolution. (Default: 000h)

VRES[9:0]: Vertical Display Resolution. (Default: 000h)

The source/gate driver output will always start from S0/G0 for all of the resolutions. For example, if Panel size is 640x480, HRES[9:0] set to 0x280, VRES[9:0] set to 1E0.

Horizontal Resolution should be multiple of 16. Minimum Resolution is 16x16.

(17) Auto Measure Vcom (AMV) (R80h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	80h
	0	1	-	VCM_EN	AMVT[1:0]		AMVX	AMVS	AMV	AMVE	50h

This command reads the IC status.

VCM_EN: Vcom Output enable

0: VCOM floating

1: VCOM output (default)

AMVT[1:0]: the sensing time of VCOM detection

00b: 3s **01b: 5s (default)**

10b: 8s 11b: 10s

AMVX: **0: Measure VCOM w/o XON function (gate scanning turn on) (default)**

1: Measure VCOM w/o XON function (gate all turn on)

AMVS: **0: Setting source output = 0V. (default)**

1: Setting source output = 3V(or VSLV)

AMV: **0: Get VCOM value by R81H (default)**

1: Get VCOM value in analog SIGNAL

AMVE: **0: Auto measure VCOM disable (default)**

1: Auto measure VCOM enable

(18) Read Vcom Value (VV) (R81h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	81h
	1	1	-	VV[6:0]							00h

This command gets the Vcom value.

VV[6:0]: Vcom Value Output

VV[6:0]	Vcom value
000 0000	(Reserved)
000 0001	(Reserved)
000 0010	-0.10 V
000 0011	-0.15 V
000 0100	-0.20 V
:	:
101 0000	-4.00 V
(others)	Reserved

(19) VCM_DC Setting (VDCS) (R82h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCM_DC	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	82h
	0	1	-	VDCS[6:0]							18h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS[6:0]	Vcom value
000 0000	(Reserved)
000 0001	(Reserved)
000 0010	-0.10 V
000 0011	-0.15 V
000 0100	-0.20 V
:	:
001 0100	-1.00 V
:	:
001 1110	-1.50 V
:	:

101 0000	-4.00 V
(others)	Reserved

(20) Data Start Transmission Window (DTMW) (R83h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sets window (X, Y, W, L)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	83h
	0	1	-	-	-	-	-	-	X[9:8]		00h
	0	1	X[7:0]								00h
	0	1	-	-	-	-	-	-	Y[9:8]		00h
	0	1	Y[7:0]								00h
	0	1	-	-	-	-	-	-	W[9:8]		00h
	0	1	W[7:0]								00h
	0	1	-	-	-	-	-	-	L[9:8]		00h
	0	1	L[7:0]								00h

This command defines the window before user start to transmit data.

(X, Y) is the origin of the window, while indicates its width, and L the height. X and W should be 4n format where n is integer.

X and W should be multiple by 4 when DM=0 (R00h).

X and W should be multiple by 8 when DM=1 (R00h).

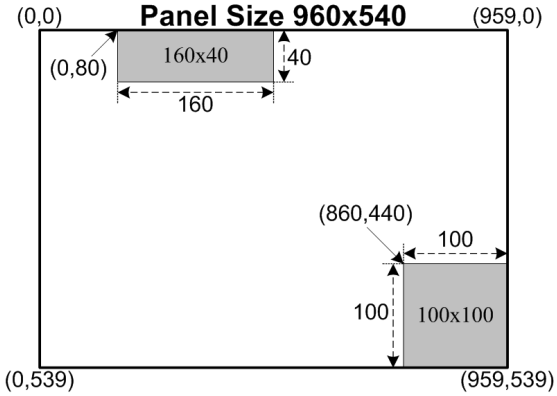
Minimum window size is 4x1(DM=0) or 8x1(DM=1).

Example: If Panel size is 960x540, then Top-left point is (X,Y)=(0,0) Top-Right point is (X,Y)=(959,0)

Bottom-Left point is (X,Y)=(0,539), Bottom-Right point is (X,Y)=(959,539)

If window size 160x40, top-left point is (100,0), then (X, Y, W, L)=(100, 0, 160, 40)

If window size 100x100, top-left point is (860, 440), then (X, Y, W, L)=(860, 440, 100, 100)

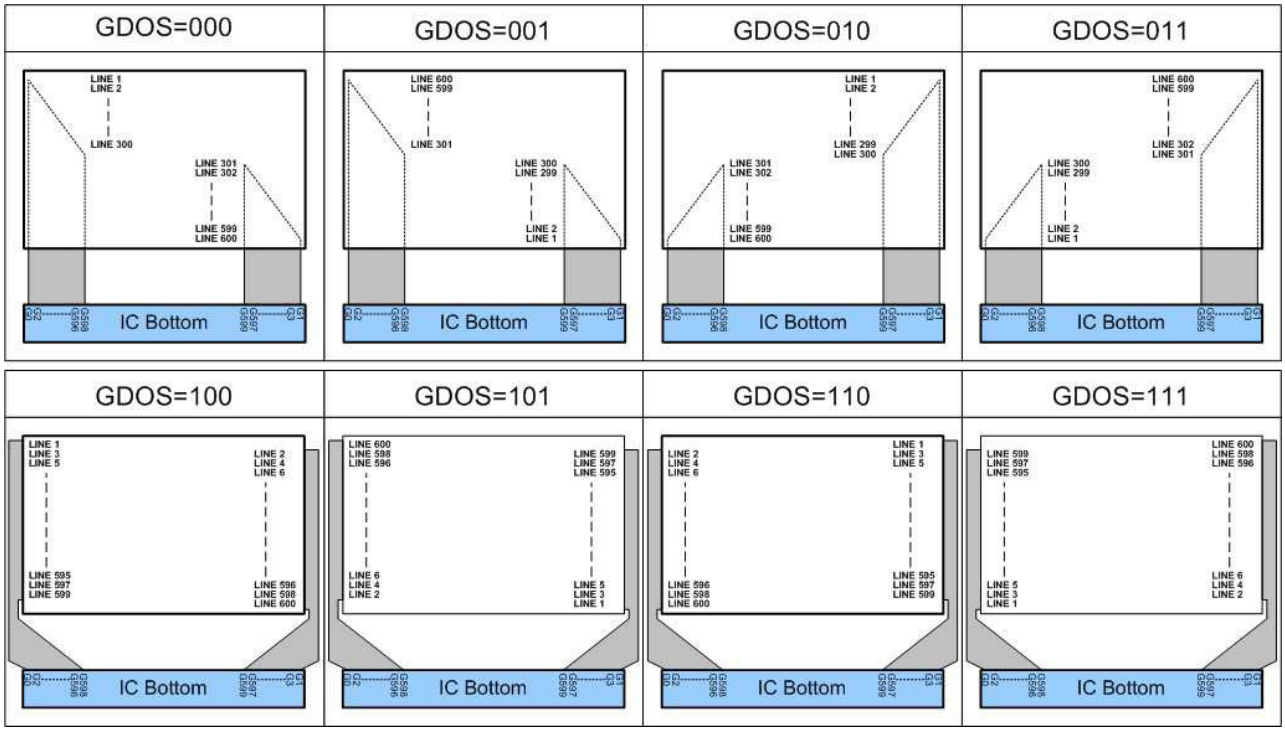


(21) GD Order Setting (GDOS) (RE0h)

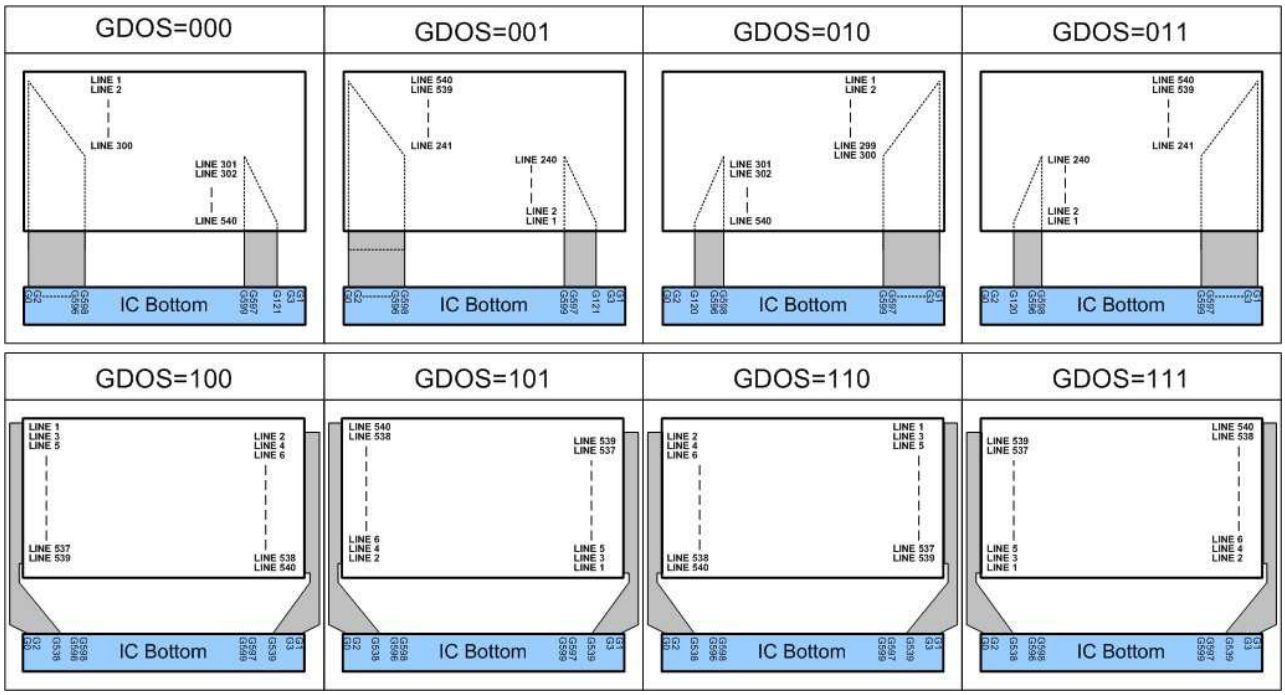
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set GD scan order	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	E0h
	1	1	-	-	-	-	0	GDOS[2:0]			00h
	1	1	1	1	1	1	1	1	1	1	FFh

GDOS: Gate Driver Order Setting

GDOS[2:0]			GD Scan Order **(GATE number = 600)**
0	0	0	G0→G2→G4….G594→G596→G598→G599→G597→G595….G5→G3→G1
0	0	1	G1→G3→G5….G595→G597→G599→G598→G596→G594….G4→G2→G0
0	1	0	G1→G3→G5….G595→G597→G599→G598→G596→G594….G4→G2→G0
0	1	1	G0→G2→G4….G594→G596→G598→G599→G597→G595….G5→G3→G1
1	0	0	G0→G1→G2….G597→G598→G599
1	0	1	G599→G598→G597….G2→G1→G0
1	1	0	G1→G0→G3→G2….G597→G596→G599→G598
1	1	1	G598→G599→G596→G597….G2→G3→G0→G1



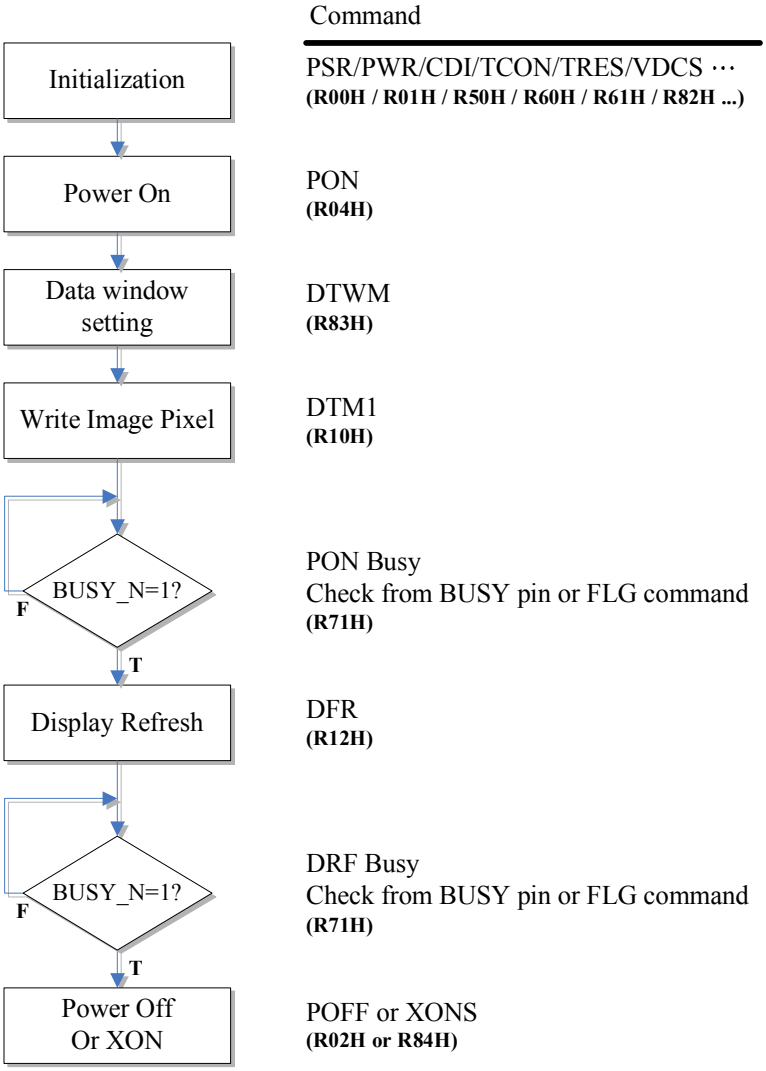
GDOS[2:0]			GD Scan Order **(GATE number = 540)**
0	0	0	G0→G2→G4….G594→G596→G598→G599→G597→G595….G125→G123→G121
0	0	1	G121→G123→G125….G595→G597→G599→G598→G596→G594….G4→G2→G0
0	1	0	G1→G3→G5….G595→G597→G599→G598→G596→G594….G124→G122→G120
0	1	1	G120→G122→G124….G594→G596→G598→G599→G597→G595….G5→G3→G1
1	0	0	G0→G1→G2….G537→G538→G539
1	0	1	G539→G538→G537….G2→G1→G0
1	1	0	G1→G0→G3→G2….G537→G536→G539→G538
1	1	1	G538→G539→G536→G537….G2→G3→G0→G1



The pins to be connected are fixed and pins to be unconnected may become NC in above layout illustration.

The layout illustrations above are just examples, and the layout method can be adjusted according to actual requirement.

8-2) Normal display mode



9. Optical characteristics

9-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	33	42	-	%	Note 9-1
Gn	N_{th} Grey Level	-		DS+(WS-DS)×n /(m-1)		L*	-
CR	Contrast Ratio	-	10	16	-		-

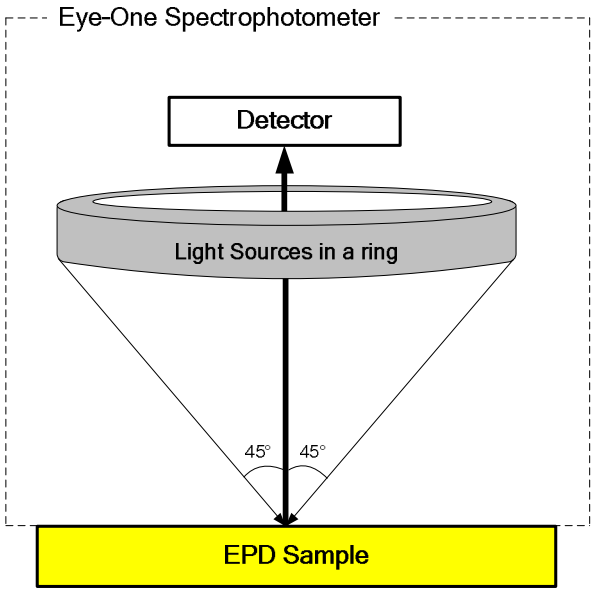
WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS

m:4、8、16 when 2、3、4 bits mode

Note 9.1: Luminance meter: Eye – One Pro Spectrophotometer.

9-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl / Rd



9-3) Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{center} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board.

10. HANDLING, SAFETY AND ENVIRONMENTAL REQUIREMENTS AND REMARK

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. When the display is broken, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.
REMARK
All the specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any post-assembly operation.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains preliminary product specifications.
Limiting values	
1.Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. 2. The LED maximum driving current is 25mA	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

11. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-1	
3	High-Temperature Storage	T = +70°C, RH=40% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-78	
6	High Temperature, High- Humidity Storage	T = +60℃, RH=80% for 240hrs Test in white pattern	IEC 60 068-2-78	
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ Test in white pattern	IEC60 068-2-5Sa	
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	
10	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3 edges, 6 faces One drop for each.	Full packed for shipment	
11	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	JEDEC EIAJ JESD22-A115-C	

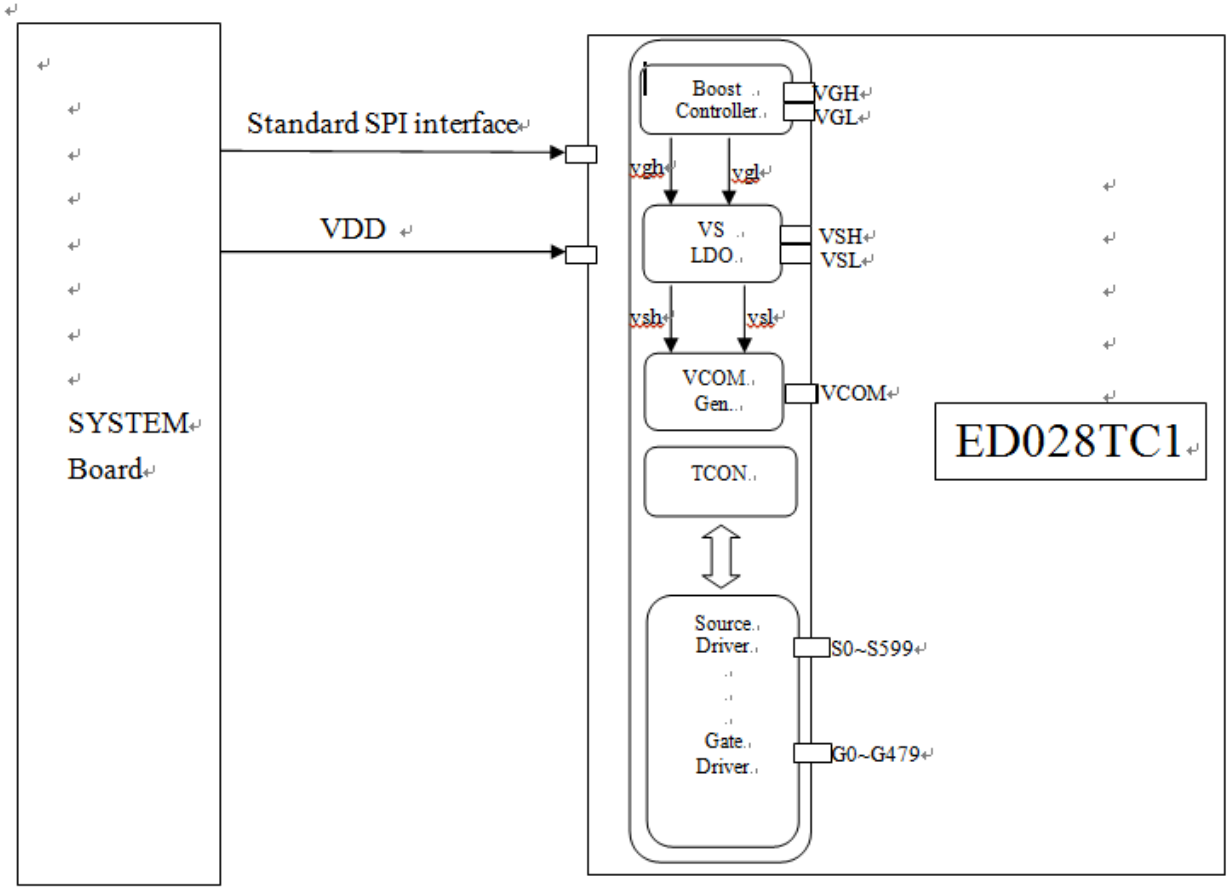
Actual EMC level to be measured on customer application

Note 11.1: The protective film must be removed before temperature test.

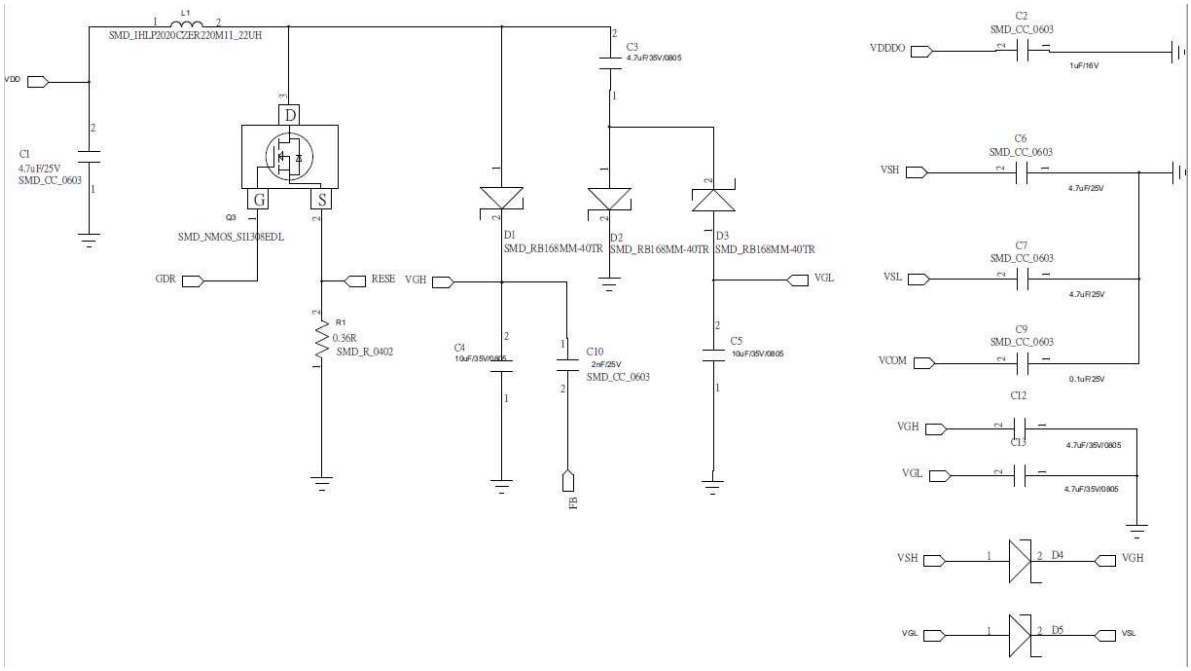
< Criteria >

In the standard conditions, there is not display function NG issue occurred. (include: line defect ,no image). All the cosmetic specification is judged before the reliability stress.

12. Block Diagram

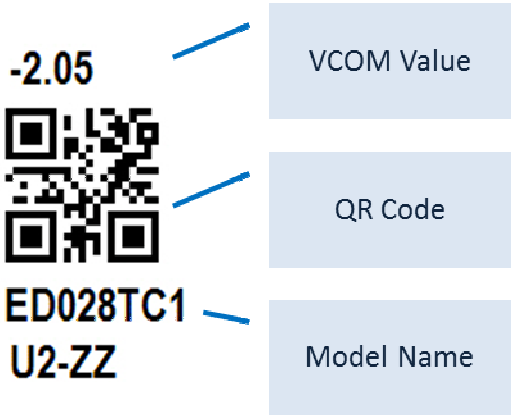


13. Reference Circuit



Note 13.1 The capacitor value of VGH/VGL must be equal or more than the one of VSH/VSL. During power-off sequence, keep VGH value greater than VSH, VGL value less than VSL. It means that VGH / VGL are highest voltage / lowest voltage. Then surely discharge VGH / VSH / VSL / VGL to GND before power-on.

14. Module Barcode Definition

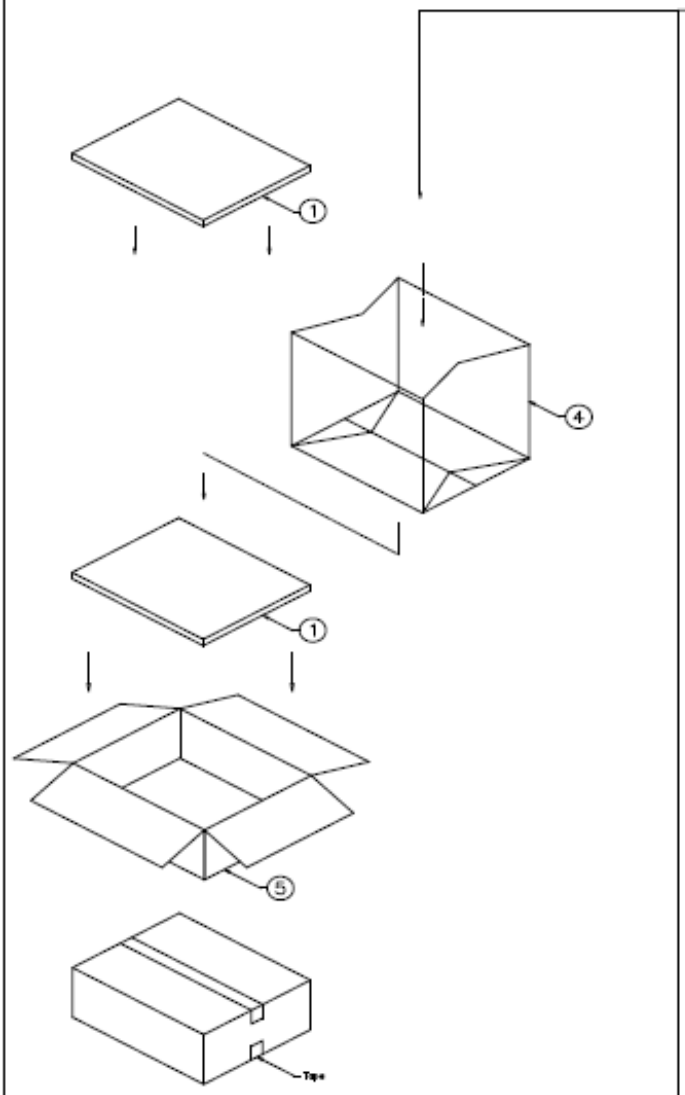


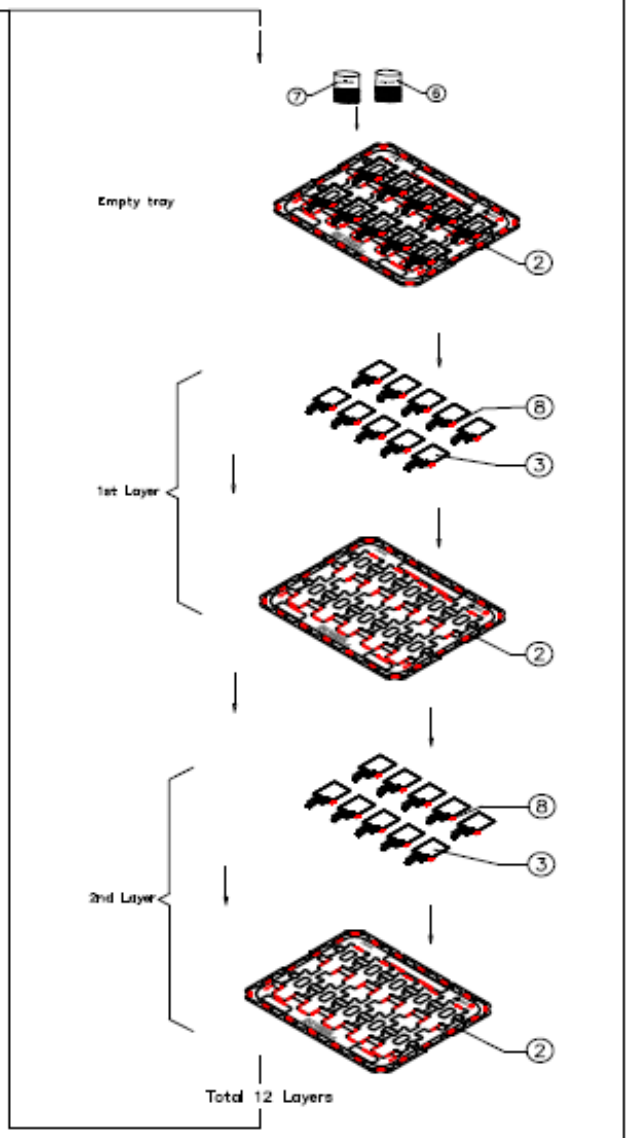
Total 25 digits in barcode scan information. Definition is below,

Digit 1~3	Module No
Digit 4~5	System code
Digit 6~8	FPL Version Code
Digit 9	System code
Digit 10	Year Code
Digit 11	Month Code
Digit 12~19	System code
Digit 20	Blank
Digit 21~25	Vcom Value

15. Packing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	CH Dong	2017/06/01





NOTE:
1. One layer include:
   10 pcs module & 1 piece of tray.
2. Q'TY: 120 pcs panel/carton.
3. Dimension: 445*365*170mm
4. Make sure tray stacked with 0° rotation.
   We can check this by lateral side view.

ITEM	DESCRIPTION	Q'TY	REMARK
8	Peeling tape	120	
7	30g 73*95mm	2	
6	(25L)	3	
5	CARTON INTERNAL	1	
4	450*380*580mm	1	
3	ED028TC1	120	
2	TRAY	13	
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ±5.0mm ANGLE ROUGHNESS	REMARK

E Ink 元太科技工業股份有限公司

			SCALE	UNIT	SHEET	DWG.TITLE
APPROVE	Patrick Lin	2017/06/15	1:1	mm	1 OF 1	ED028TC1 PACKING
CHECK	Patrick Lin	2017/06/15	MTL.NO.		DWG.NO.	A4 SIZE
DESIGN	CH DONG	2017/06/01				

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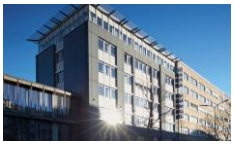
ALL TECHNOLOGIES. ALL COMPETENCIES. ONE SPECIALIST.



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