



SPECIFICATION



DEPG0154BNS800F25

1.54", 152×152

Version: 2.0

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Note: This specification is subject to change without prior notice

www.data-modul.com

Specification for 1.54 inch EPD Model NO. :

DEPG0154BNS800F25

DKE's Confirmation:

| Prepared by | Checked by | Approved by |
|-------------|------------|-------------|
| | | |

Customer approval:

| Customer | Approved by | Date |
|----------|-------------|------|
| | | |

Revision History

| Version | Content | Date | Producer |
|----------------|----------------|-------------|-----------------|
| 2.0 | New release | 2020/11/12 | |
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1. Over View

DEPG0154BNS800F25 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 1.54inch active area contains 152×152 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆ 152×152 pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I²C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor

3. Mechanical Specification

| Parameter | Specifications | Unit | Remark |
|---------------------|---------------------------|-------|---------|
| Screen Size | 1.54 | Inch | |
| Display Resolution | 152(H)×152(V) | Pixel | DPI:140 |
| Active Area | 27.512×27.512 | mm | |
| Pixel Pitch | 0.181×0.181 | mm | |
| Pixel Configuration | Square | | |
| Outline Dimension | 31.8(H)×37.3 (V) ×1.0 (D) | mm | |
| Weight | 2.18±0.5 | g | |

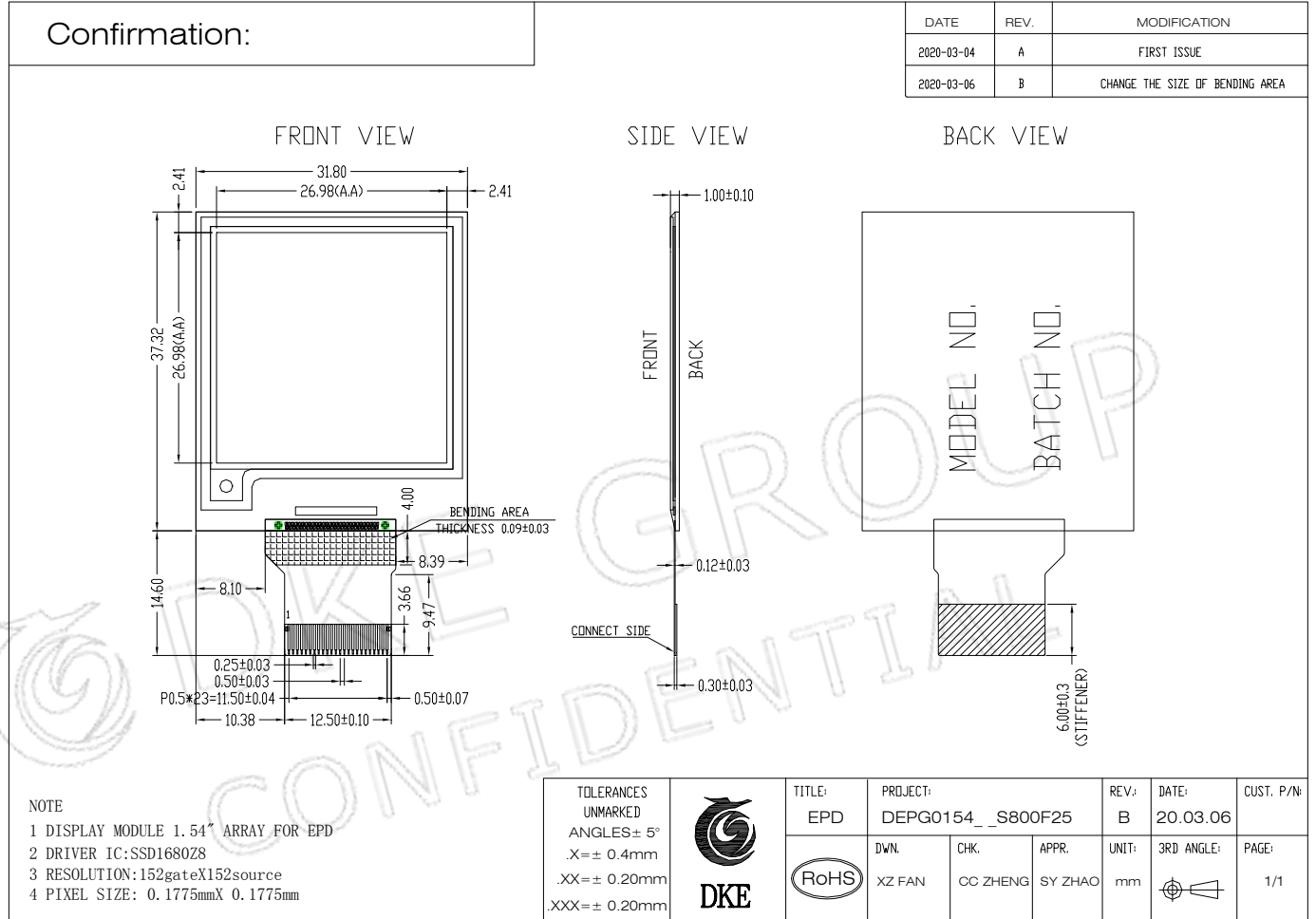
| Symbol | Parameter | Conditions | Min | Typ. | Max | Units | Notes |
|--------|----------------------|----------------------------------|------|--------|-----|-------|-------|
| KS | Black State L* value | | - | 18 | 20 | | 3-1 |
| | Black Ghosting ΔL | | - | 1 | - | | 3-1 |
| WS | White State L* value | | 66 | 67 | | | 3-1 |
| | White Ghosting ΔL | | - | 1 | - | | 3-1 |
| R | White Reflectivity | White | 30 | 34 | - | % | 3-1 |
| CR | Contrast Ratio | Indoor | 15:1 | 20:1 | - | | 3-1 |
| | | | | | | | 3-2 |
| GN | 2Grey Level | - | - | - | - | | |
| Life | | Temp:23±3°C Humidity:55±10%RH | | 5years | | | 3-3 |

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

4. Mechanical Drawing of EPD Module



5. Input/output Pin Assignment

| No. | Name | I/O | Description | Remark |
|-----|-------|-----|--|-----------|
| 1 | NC | | Do not connect with other NC pins | Keep Open |
| 2 | GDR | O | N-Channel MOSFET Gate Drive Control | |
| 3 | RESE | I | Current Sense Input for the Control Loop | |
| 4 | NC | NC | Do not connect with other NC pins | Keep Open |
| 5 | VSH2 | C | Positive Source driving voltage(Red) | |
| 6 | TSCL | O | I2C Interface to digital temperature sensor Clock pin | |
| 7 | TSDA | I/O | I2C Interface to digital temperature sensor Data pin | |
| 8 | BS1 | I | Bus Interface selection pin | Note 5-5 |
| 9 | BUSY | O | Busy state output pin | Note 5-4 |
| 10 | RES# | I | Reset signal input. Active Low. | Note 5-3 |
| 11 | D/C# | I | Data /Command control pin | Note 5-2 |
| 12 | CS# | I | Chip select input pin | Note 5-1 |
| 13 | SCL | I | Serial Clock pin (SPI) | |
| 14 | SDA | I/O | Serial Data pin (SPI) | |
| 15 | VDDIO | P | Power Supply for interface logic pins It should be connected with VCI | |
| 16 | VCI | P | Power Supply for the chip | |
| 17 | VSS | P | Ground | |
| 18 | VDD | C | Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS | |
| 19 | VPP | P | FOR TEST | Keep Open |
| 20 | VSH1 | C | Positive Source driving voltage | |
| 21 | VGH | C | Power Supply pin for Positive Gate driving voltage and VSH1 | |
| 22 | VSL | C | Negative Source driving voltage | |
| 23 | VGL | C | Power Supply pin for Negative Gate driving voltage VCOM and VSL | |
| 24 | VCOM | C | VCOM driving voltage | |

I = Input Pin, O =Output Pin, /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

| BS1 State | MCU Interface |
|-----------|--|
| L | 4-lines serial peripheral interface(SPI) - 8 bits SPI |
| H | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

6. Electrical Characteristics

6.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit |
|--------------------------|--------|------------------|------|
| Logic supply voltage | VCI | -0.5 to +6.0 | V |
| Logic Input voltage | VIN | -0.5 to VCI +0.5 | V |
| Logic Output voltage | VOUT | -0.5 to VCI +0.5 | V |
| Operating Temp range | TOPR | 0 to +50 | °C. |
| Storage Temp range | TSTG | -25 to+70 | °C. |
| Optimal Storage Temp | TSTGo | 23±3 | °C. |
| Optimal Storage Humidity | HSTGo | 55±10 | RH |

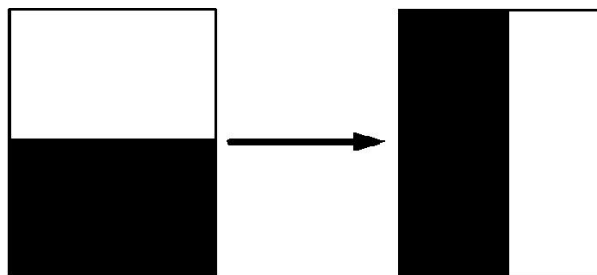
Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR = 25°C.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---------------------------|-----------------------|---|-----------------|---------------------|-------|---------------------|------|
| Single ground | V _{SS} | - | | - | 0 | - | V |
| Logic supply voltage | V _{CI} | - | V _{CI} | 2.2 | 3.0 | 3.7 | V |
| Core logic voltage | V _{DD} | | V _{DD} | 1.7 | 1.8 | 1.9 | V |
| High level input voltage | V _{IH} | - | - | 0.8 V _{CI} | - | - | V |
| Low level input voltage | V _{IL} | - | - | - | - | 0.2 V _{CI} | V |
| High level output voltage | V _{OH} | I _{OH} = -100uA | - | 0.9 V _{CI} | - | - | V |
| Low level output voltage | V _{OL} | I _{OL} = 100uA | - | - | - | 0.1 V _{CI} | V |
| Typical power | P _{TYP} | V _{CI} = 3.0V | - | - | 7.5 | - | mW |
| Deep sleep mode | P _{STPY} | V _{CI} = 3.0V | - | - | 0.003 | - | mW |
| Typical operating current | I _{opr_VCI} | V _{CI} = 3.0V | - | - | 2.5 | - | mA |
| Image update time | - | 25 °C | - | - | 4 | - | sec |
| Typical peak current | I _{opr_VCI} | 2.2~3.7v | | | 30 | 40 | mA |
| Sleep mode current | I _{slp_VCI} | DC/DC off No clock No input load Ram data retain | - | - | 20 | | uA |
| Deep sleep mode current | I _{dslp_VCI} | DC/DC off No clock No input load Ram data not retain | - | - | 1 | 5 | uA |

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical characteristics are only guaranteed under the controller & waveform provided by DKE.

4. Electrical measurement: Tektronix oscilloscope - MDO3024,

Tektronix current probe - TCP0030A.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|--------------------------------|-----------------|-----------|----------------------------------|-------|------|-------|------|
| VCOM output voltage | VCOM | - | VCOM | - | TBD | - | V |
| Positive Source output voltage | V _{SH} | - | S ₀ ~S ₁₅₁ | +14.5 | +15 | +15.5 | V |
| Negative Source output voltage | V _{SL} | - | S ₀ ~S ₁₅₁ | -15.5 | -15 | -14.5 | V |
| Positive gate output voltage | V _{gh} | - | G ₀ ~G ₁₅₁ | +21 | +22 | +23 | V |
| Negative gate output voltage | V _{gl} | - | G ₀ ~G ₁₅₁ | -21 | -20 | -19 | V |

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

| Pin Name | Data/Command Interface | | Control Signal | | |
|------------------|------------------------|-----|----------------|------|------|
| | SDA | SCL | CS# | D/C# | RES# |
| Bus interface | SDA | SCL | CS# | D/C# | RES# |
| BS1=L 4-wire SPI | SDA | SCL | CS# | D/C# | RES# |
| BS1=H 3-wire SPI | SDA | SCL | CS# | L | RES# |

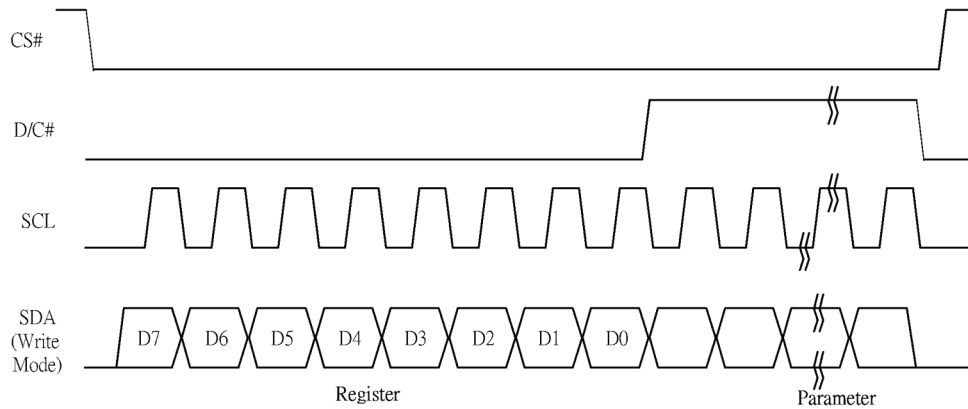
6.4.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

| Function | CS# | D/C# | SCL |
|---------------|-----|------|-----|
| Write command | L | L | ↑ |
| Write data | L | H | ↑ |

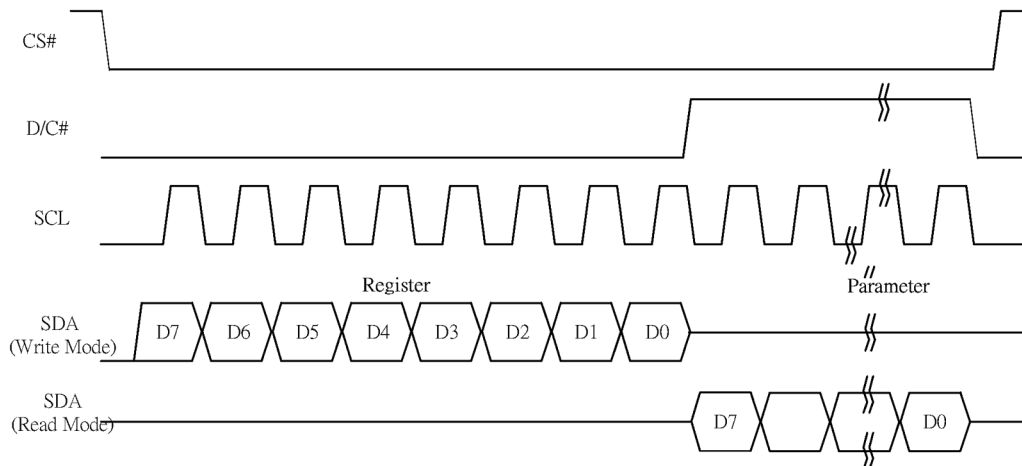
Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

Figure 6-1: Write procedure in 4-wire SPI mode


In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-2: Read procedure in 4-wire SPI mode


6.4.3 MCU Serial Interface (3-wire SPI)

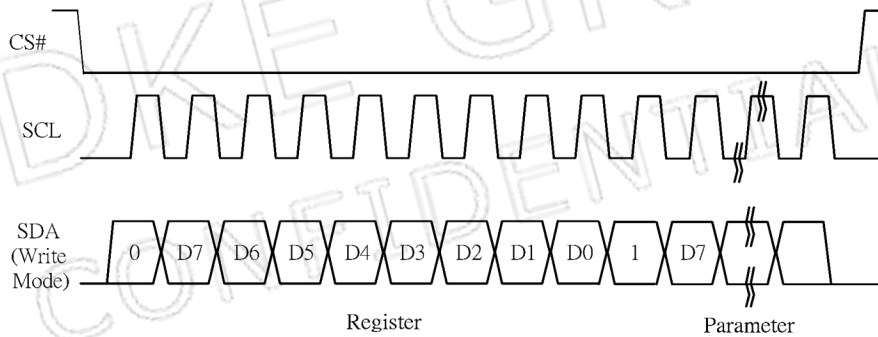
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

| Function | CS# | D/C# | SCL |
|---------------|-----|------|-----|
| Write command | L | Tie | ↑ |
| Write data | L | Tie | ↑ |

Note: ↑ stands for rising edge of signal

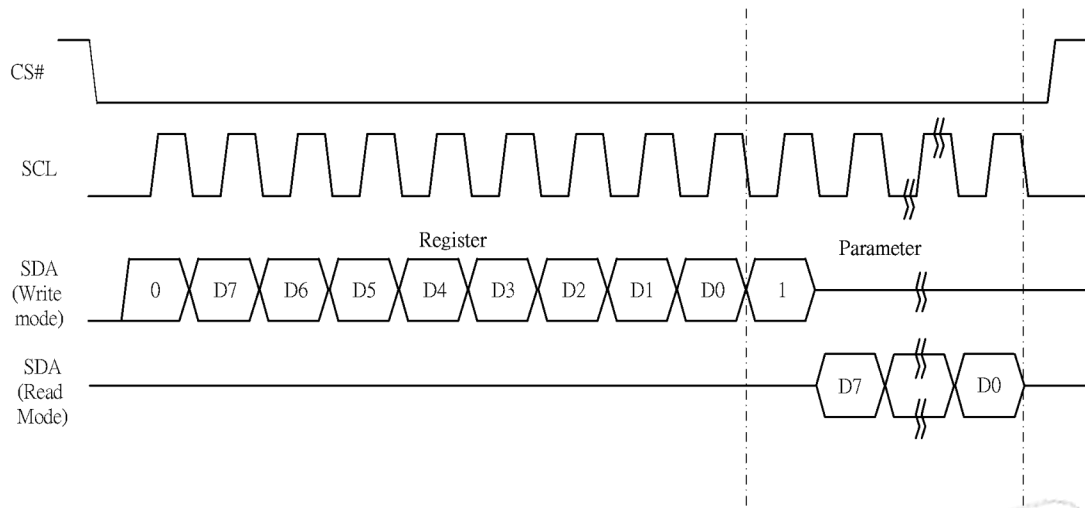
Figure 6-3: Write procedure in 3-wire SPI mode



In the Read mode:

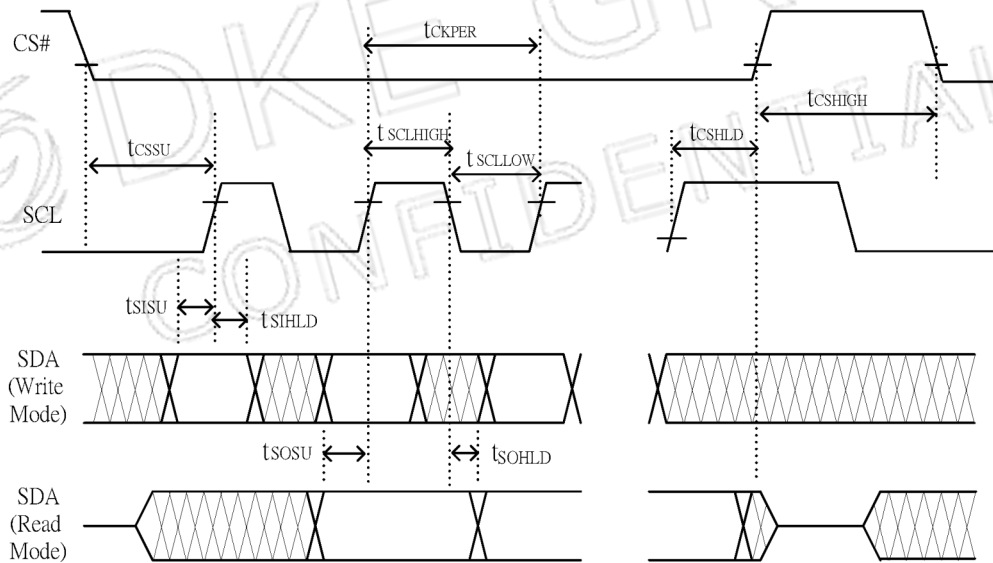
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, T_{OPR} =25°C.



Changed Diagram

Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20pF)

Write mode

| Symbol | Parameter | Min | Typ. | Max | Unit |
|----------|--|-----|------|-----|------|
| fSCL | SCL frequency (Write Mode) | | | 20 | MHz |
| tCSSU | Time CS# has to be low before the first rising edge of SCLK | 60 | | | ns |
| tCSHLD | Time CS# has to remain low after the last falling edge of SCLK | 65 | | | ns |
| tCSHIGH | Time CS# has to remain high between two transfers | 100 | | | ns |
| tSCLHIGH | Part of the clock period where SCL has to remain high | 25 | | | ns |
| tSCLLOW | Part of the clock period where SCL has to remain low | 25 | | | ns |
| tSISU | Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL | 10 | | | ns |
| tSIHLD | Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL | 40 | | | ns |

Read mode

| Symbol | Parameter | Min | Typ. | Max | Unit |
|----------|--|-----|------|-----|------|
| fSCL | SCL frequency (Read Mode) | | | 2.5 | MHz |
| tCSSU | Time CS# has to be low before the first rising edge of SCLK | 100 | | | ns |
| tCSHLD | Time CS# has to remain low after the last falling edge of SCLK | 50 | | | ns |
| tCSHIGH | Time CS# has to remain high between two transfers | 250 | | | ns |
| tSCLHIGH | Part of the clock period where SCL has to remain high | 180 | | | ns |
| tSCLLOW | Part of the clock period where SCL has to remain low | 180 | | | ns |
| tSOSU | Time SO(SDA Read Mode) will be stable before the next rising edge of SCL | | 50 | | ns |
| tSOHLD | Time SO (SDA Read Mode) will remain stable after the failing edge of SCL | | 0 | | ns |

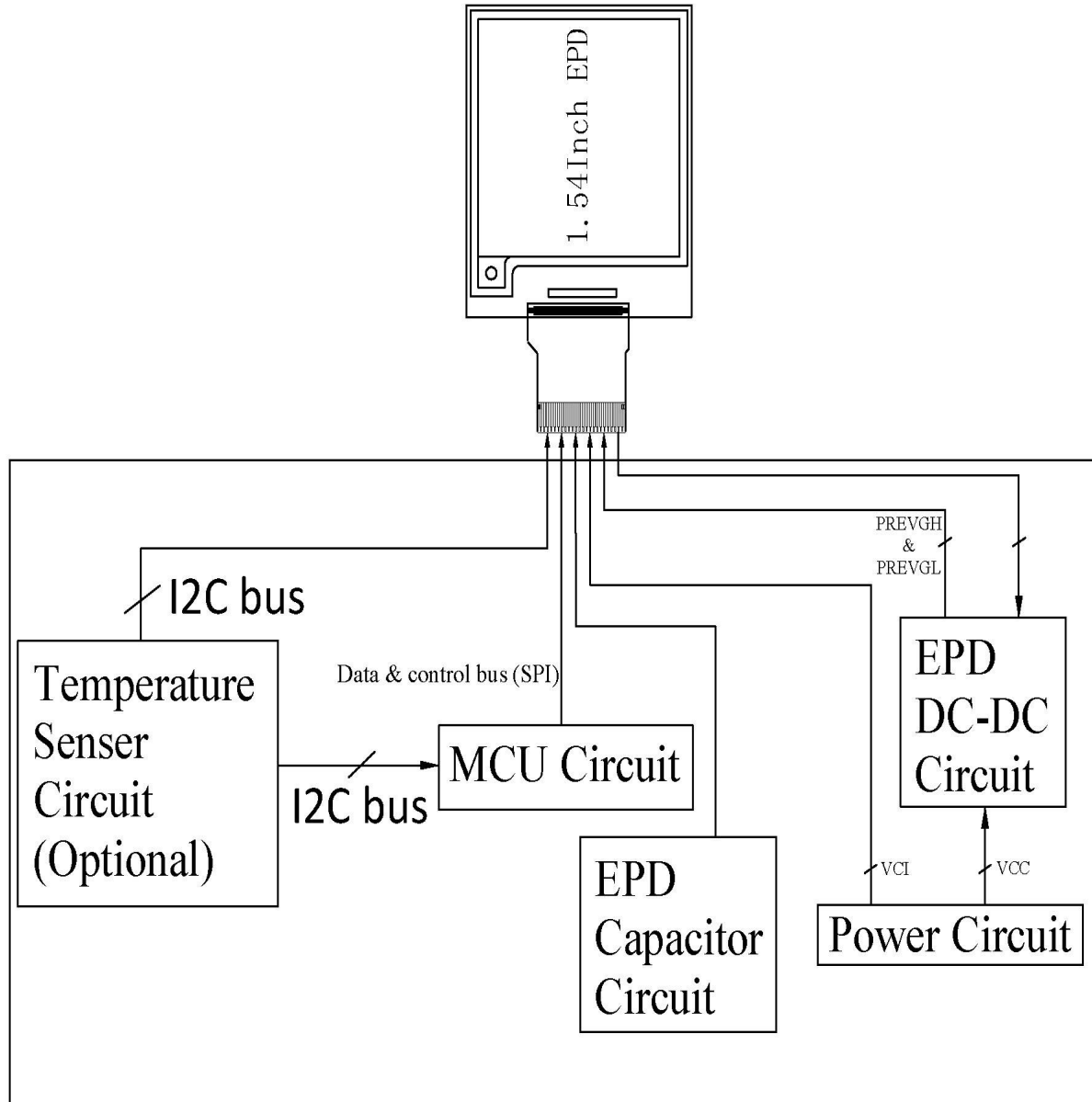
7. Command Table

| R/W# | D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Command | Description |
|------|------|-----|----|----|----|----|----|----|----|----|----------------------------|---|
| 0 | 0 | 01 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Driver Output control | Gate setting Set A[8:0]=0097h Set B[8:0]=00h |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A8 | | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | B2 | B1 | B0 | | |
| 0 | 0 | 10 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Deep Sleep mode | Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A0 | | |
| 0 | 1 | | 1 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 1 | | 1 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 1 | | 1 | C6 | C5 | C4 | C3 | C2 | C1 | C0 | | |
| 0 | 1 | | 0 | 0 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 0 | 0 | 12 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | SWRESET | It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command. |
| 0 | 0 | 18 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | Temperature Sensor Control | Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 0 | 20 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Master Activation | Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images. |

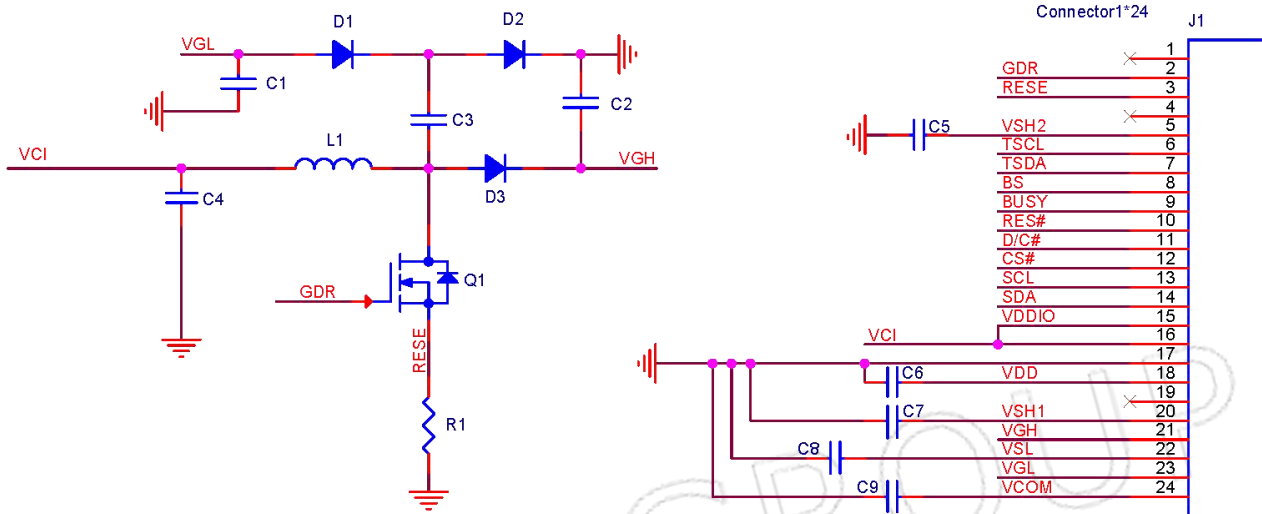
| | | | | | | | | | | | | |
|---|---|----|----|----|----|----|----|----|----|----|--------------------------|---|
| 0 | 0 | 22 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | Display Update Control 2 | Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR) Operating sequence Parameter (in Hex) Enable clock signal 80 Disable clock signal 01 Enable clock signal Enable Analog C0 Disable Analog Disable clock signal 03 Enable clock signal Load LUT with DISPLAY Mode 1 Disable clock signal C7 Enable clock signal Enable Analog Display with DISPLAY Mode 2 Disable Analog Disable OSC F7 Enable clock signal Enable Analog Load temperature value DISPLAY with DISPLAY Mode 2 Disable Analog Disable OSC FF |
| 0 | 1 | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| 0 | 0 | 2F | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | Status Bit Read | Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively |

| | | | | | | | | | | | | | |
|---|---|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------|--|--|
| 0 | 0 | 3C | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | | | Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HiZ. A [7:6] :Select VBD option A[7:6] Select VBD as 00 GS Transition, Defined in A[2] and A[1:0] 01 Fix Level, Defined in A[5:4] 10 VCOM 11[POR] HiZ A [5:4] Fix Level Setting for VBD A[5:4] VBD level 00 VSS 01 VSH1 10 VSL 11 VSH2 A[2] GS Transition control A[2] GS Transition control 0 Follow LUT (Output VCOM @ Yellow) 1 Follow LUT A [1:0] GS Transition setting for VBD A[1:0] VBD Transition 00 LUT0 01 LUT1 10 LUT2 11 LUT3 |
| 0 | 1 | | A ₇ | A ₆ | A ₅ | A ₄ | 0 | 0 | A ₁ | A ₀ | | | |
| 0 | 0 | 44 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Set RAM | Specify the start/end positions of the window | |
| 0 | 1 | | 0 | 0 | 0 | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | X - | address | |
| 0 | 1 | | 0 | 0 | 0 | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | Start / | End | |
| | | | | | | | | | | | position | | |
| 0 | 0 | 45 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Set Ram | Specify the start/end positions of the window | |
| 0 | 1 | | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | Y- | address | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A ₈ | Start / | End | |
| 0 | 1 | | B ₇ | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ | position | | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | B ₈ | | | |
| 0 | 0 | 4E | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | Set RAM | Make initial settings for the RAM X address in | |
| 0 | 1 | | 0 | 0 | 0 | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | X | address | |
| | | | | | | | | | | | counter | | |
| 0 | 0 | 4F | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Set RAM | Make initial settings for the RAM Y address in | |
| 0 | 1 | | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | Y | address | |
| 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A ₈ | counter | | |

8. Block Diagram



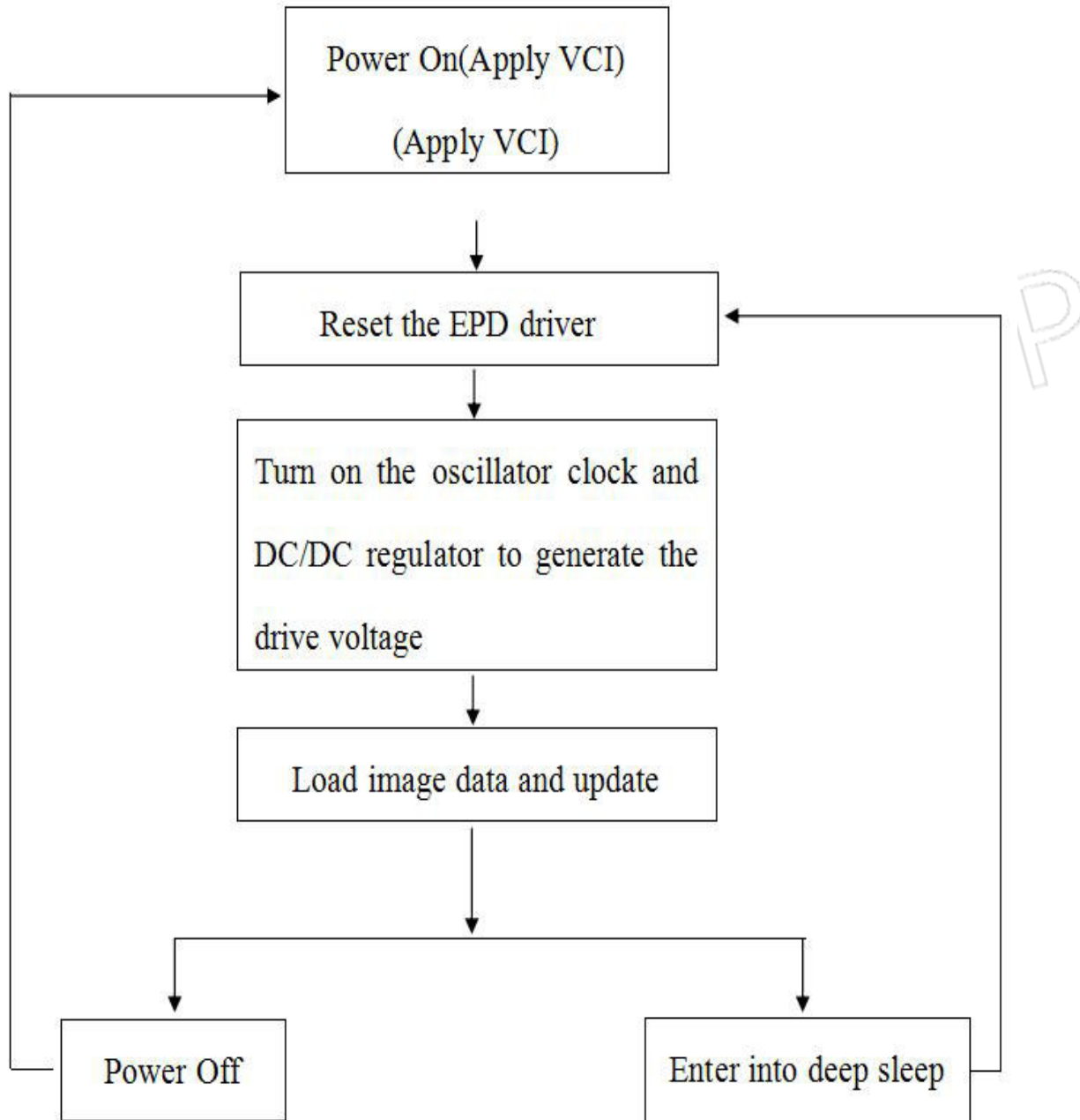
9. Typical Application Circuit with SPI Interface



| Part Name | Value | Reference Part | Requirements for spare part |
|----------------------|------------|--|--|
| C4 C6 | 1uF | X5R/X7R; Voltage Rating:6v or 25v | |
| C1 C2 C9 C5 C7 C8 | 1uF | 0402/0603/0805; X5R/X7R; Voltage Rating:25v | |
| C3 | 0.47uF/1uF | 0603/0805; X7R; Voltage Rating:25v NOTE: Effective capacitance >0.25uF @18v DC bias | |
| R1 | 2.2Ohm | 0402/0603/0805; 1% variation, ≥0.05W | |
| D1 D2 D3 | Diode | MBR0530 | 1)Reverse DC Voltage ≥30V 2)Io ≥500mA 3)Forward voltage ≤430mV |
| Q1 | NMOS | Si1304BDL/NX3008NBK | 1)Drain-Source breakdown voltage ≥30v 2)Vgs(th)=0.9v(Typ), 1.3v(Max) 3)rds on ≤2.1Ω @ Vgs=2.5v |
| L1 | 47UH | CDRH2D18/LDNP-470NC | 1) Io=500mA(max) |

10 Typical Operating Sequence

10.1 OTP Operation Flow



10.2 OTP Operation Reference Program Code

| ACTION | VALUE/DATA | COMMENT |
|--------------------------|------------|----------------------------|
| POWER ON | | |
| delay | 10ms | |
| PIN CONFIG | | |
| RES# | low | Hardware reset |
| delay | 200us | |
| RES# | high | |
| delay | 200us | |
| Read busy pin | | Wait for busy low |
| Command 0x12 | | Software reset |
| Read busy pin | | Wait for busy low |
| SET VOLTAGE AND LOAD LUT | | |
| LOAD IMAGE AND UPDATE | | |
| Command 0x24 | 2888bytes | Load image (152/8*152)(BW) |
| Command 0x20 | | |
| Read busy pin | | Wait for busy low |
| Command 0x10 | Data 0X01 | Enter deep sleep mode |
| POWER OFF | | |


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11. Reliability Test

| NO | Test items | Test condition |
|----|---|--|
| 1 | Low-Temperature Storage | T = -25°C, 240 h Test in white pattern |
| 2 | High-Temperature Storage | T=+70°C, RH=40%, 240h Test in white pattern |
| 3 | High-Temperature Operation | T=+50°C, RH=30%, 240h |
| 4 | High-Temperature, High-Humidity Operation | T=40°C, RH=90%, 240h |
| 5 | High Temperature, High Humidity Storage | T=60°C, RH=80%, 240h Test in white pattern |
| 6 | Temperature Cycle | 1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern |
| 7 | ESD Gun | Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area) |

Note: 1. Stay white pattern for storage and non-operation test.

2. Operation is black→white pattern, the interval is 150s.

°C--25°C for 1hour after test finished, The function ,appearance and display performance is ok.

12. Quality Assurance

12.1 Environment

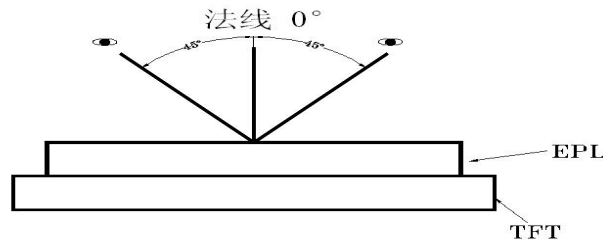
Temperature: 23±3°C

Humidity: 55±10%RH

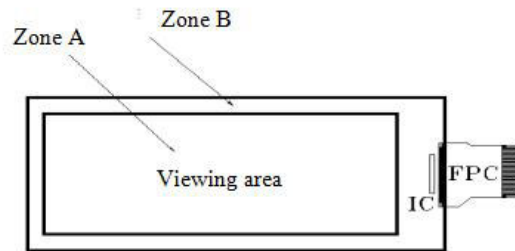
12.2 Illuminance

Brightness: 1200~1500LUX; distance: 20-30CM; Angle: Relate 45° surround.

12.3 Inspect method

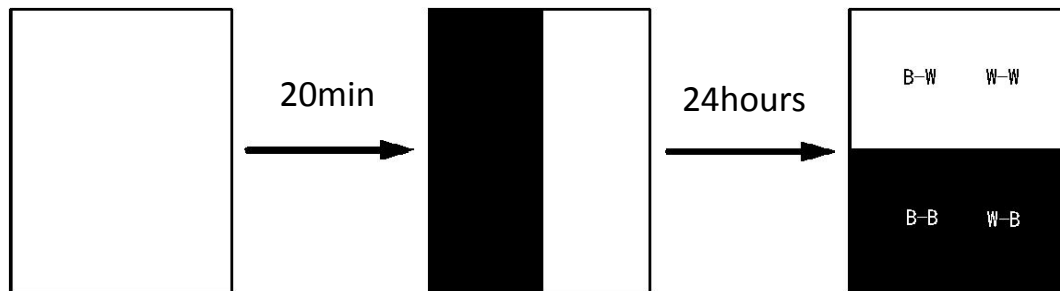


12.4 Display area



12.5 Ghosting test method

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by DKE.



1) Measurement Instruments: X-rite i1Pro

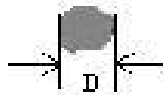
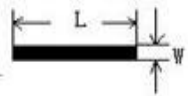
2) Ghosting formula:

W ghosting: $\Delta L = \text{Max} (\Delta L(W-W, B-W)) - \text{Min} (\Delta L(W-W, B-W))$

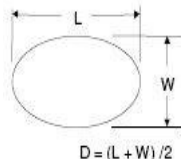
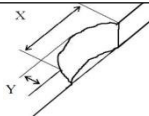
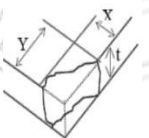
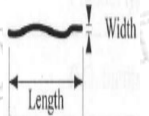



K ghosting: $\Delta L = \text{Max} (\Delta L(W-B, B-B)) - \text{Min} (\Delta L(W-B, B-B))$

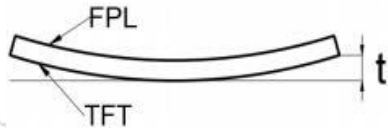
12.6 Inspection standard

12.6.1 Electric inspection standard

| NO. | Item | Standard | Defect level | Method | Scope |
|-----|--|--|--------------|----------------------------|------------------|
| 1 | Display | Display complete Display uniform | MA | | |
| 2 | Black/White spots |  $D \leq 0.25\text{mm}$, Allowed $0.25\text{mm} < D \leq 0.4\text{mm}$. $N \leq 4$ allowable $D > 0.4\text{mm}$ is not allowed | | Visual inspection | |
| 3 | Show B/W lines |  $L \leq 0.4\text{mm}, W \leq 0.1\text{mm}$ negligible $0.4\text{mm} < L \leq 1.0\text{mm}$ $0.1\text{mm} < W \leq 0.4\text{mm}$ $N \leq 4$ allowable $L > 1.0\text{mm}, W > 0.4\text{mm}$ is not allowed | MI | Visual/ Inspection card | Zone A |
| 4 | Ghost image | Allowed in switching process | MI | Visual inspection | |
| 5 | Flash spots/ Larger FPL size | Flash spots in switching, Allowed FPL size larger than viewing area, Allowed | MI | Visual/ Inspection card | Zone A Zone B |
| 6 | Display wrong/Missing | All appointed displays are showed correct | MA | Visual inspection | Zone A |
| 7 | Short circuit/ Circuit break/ Display abnormal | Not Allow | | | |

12.6.2 Appearance inspection standard

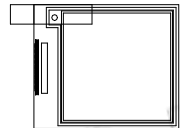
| NO. | Item | Standard | Defect level | Method | Scope |
|-----|---|--|--------------|---------------------|--------------------|
| 1 | B/W spots /Bubble/ Foreign bodies/ Dents |  <p>$D \leq 0.25\text{mm}$ negligible $0.25\text{mm} < D \leq 0.4\text{mm}$ $N \leq 4$ allowable $D > 0.4\text{mm}$ is not allowed</p> | MI | Visual inspection | Zone A |
| 2 | Glass crack | Not Allow | MA | Visual / Microscope | Zone A Zone B |
| 3 | Dirty | Allowed if can be removed | MI | | Zone A Zone B |
| 4 | Chips/Scratch/ Edge crown |  <p>$X \leq 3\text{mm}, Y \leq 0.5\text{mm}$ And without affecting the electrode is permissible</p>  <p>$2\text{mm} \leq X$ or $2\text{mm} \leq Y$ Not Allow</p>  <p>$W \leq 0.1\text{mm}, L \leq 5\text{mm}$, No harm to the electrodes and $N \leq 2$ allow</p> | MI | Visual / Microscope | Zone A Zone B |
| 5 | TFT Cracks |  <p>Not Allow</p> | MA | Visual / Microscope | Zone A Zone B |
| 6 | Dirty/ foreign body | Allowed if can be removed/ allow | MI | Visual / Microscope | Zone A / Zone B |
| 7 | FPC broken/ Goldfingers oxidation/ scratch |   <p>Not Allow</p> | MA | Visual / Microscope | Zone B |

| | | | | | |
|----|--|---|----|---------------------|------------------|
| 8 | TFT edge bulge /TFT chromatic aberration | TFT edge bulge: $X \leq 3\text{mm}$, $Y \leq 0.3\text{mm}$ Allowed TFT chromatic aberration :Allowed | MI | Visual / Microscope | Zone A Zone B |
| 9 | PCB damaged/ Poor welding/ Curl | PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl $\leq 1\%$ | MI | Visual / Ruler | Zone B |
| 10 | Edge glue height/ Edge glue bubble | Edge Adhesives H \leq PS surface (Including protect film) Edge adhesives seep in $\leq 1/2$ Margin width Length excluding Edge adhesives bubble: bubble Width $\leq 1/2$ Margin width; Length $\leq 0.5\text{mm}$ 。 n ≤ 5 | | | |
| 11 | Protect film | Surface scratch but not effect protect function, Allowed | | | |
| 12 | Silicon glue | Thickness \leq PS surface (With protect film): Full cover the IC; Shape: The width on the FPC $\leq 0.5\text{mm}$ (Front) The width on the FPC $\leq 1.0\text{mm}$ (Back) smooth surface, No obvious raised. | MI | Visual Inspection | |
| 13 | Warp degree (TFT substrate) |  $t \leq 1.0\text{mm}$ | MI | Ruler | |
| 14 | Color difference in COM area (Silver point area) | Allowed | | Visual Inspection | |

13.Packaging

| | | | | | | | |
|----------------------------------|--|--|--|--|--|----------|--|
| <h3>EPD PACKING INSTRUCTION</h3> | | | | | | DATE | |
| DKE-QS. D-010 | | | | | | DESIGN | |
| | | | | | | CHECKED | |
| | | | | | | APPROVED | |

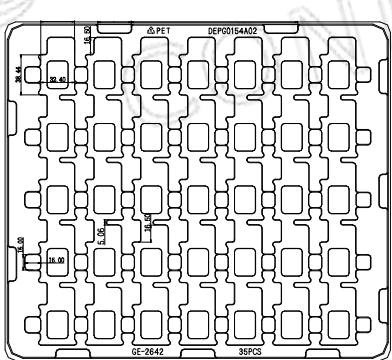
| | | | | | | | |
|----------|---------------|----------|-------|------------|---------|---------------|-----------|
| P/N | Customer Code | Ref. P/N | Type | PKG Method | Marking | Surface Marks | Pull Tape |
| DEPG0154 | | | GLASS | Blister | BACK | None | YES |

| Packing Materials List | | | | | 35PCS/LAYER, 20LAYER/CTN, TOTAL 700PCS/CTN. | |
|------------------------|--------------------------|-----------|------|-------|--|--|
| List | Model | Materials | Q'ty | Unit | Pull tape:  | |
| Carton | 7# 417*362*229 mm | corrugate | 1 | Piece | | |
| Inner Carton | 7#(INNER) 400*343 *95 mm | corrugate | 2 | Piece | | |
| Blister | DEPG0154A02 PET1.0 | PET | 22 | Piece | | |
| Thin foam | 298.4*273.92*T1.8*2.0mm | EPE | 20 | Piece | | |
| Antistatic vacuum bag | 450*590*0.075 | | 2 | Piece | | |
| Foam board | DKE2251-10 | EPE | 5 | Piece | | |
| PULL TAPE | 16*5*T0.05 | | 700 | Piece | | |

Detail:

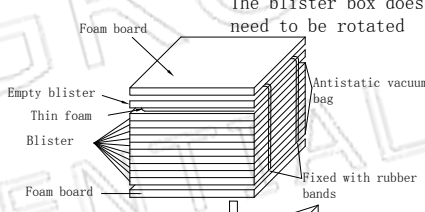
Blister box:

Note: there are 20 layers of products, divided into 2 inner boxes, and an empty blister box is placed on the top of each inner box, so the number of blister boxes is 22



QUANTITY: 35PCS

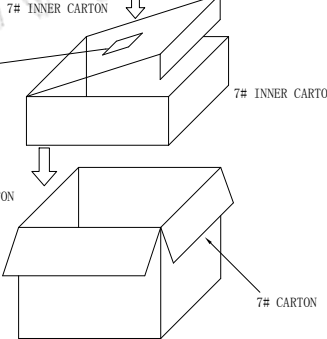
The blister box does not need to be rotated



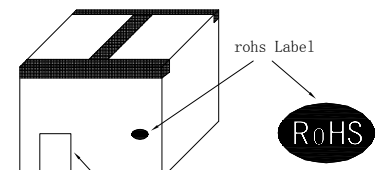
INNER BOX LABEL

| | |
|---------------|--|
| 型号 (MODEL) | |
| 数量 (QUANTITY) | |
| 批号 (LOT#) | |

PUT TWO 7# INNER CARTON INTO 7# CARTON



Packing belt



Shipping marks according to customer's requirements

| Epaper Identification | |
|-----------------------|----------------|
| QC: | PASS |
| Model No. | _____ |
| Quantity | _____ pcs |
| Date: | _____ |
| Carton No. | _____ of _____ |

14. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

| Data sheet status | |
|---|--|
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
| Product Environmental certification | |
| ROHS | |
| REMARK | |
| All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation. | |
| Transport environment | |
| When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range | |



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