



## SPECIFICATION

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**DKE** 东方科脉

DEPG0350BNS850F3

3.52", 384x184, B/W

Version: 2.0

Date: 01.06.2022

Note: This specification is subject to change without prior notice

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## Specification for 3.5 inch EPD

**Model NO. : DEPG0350BNS850F3**

### **DKE's Confirmation:**

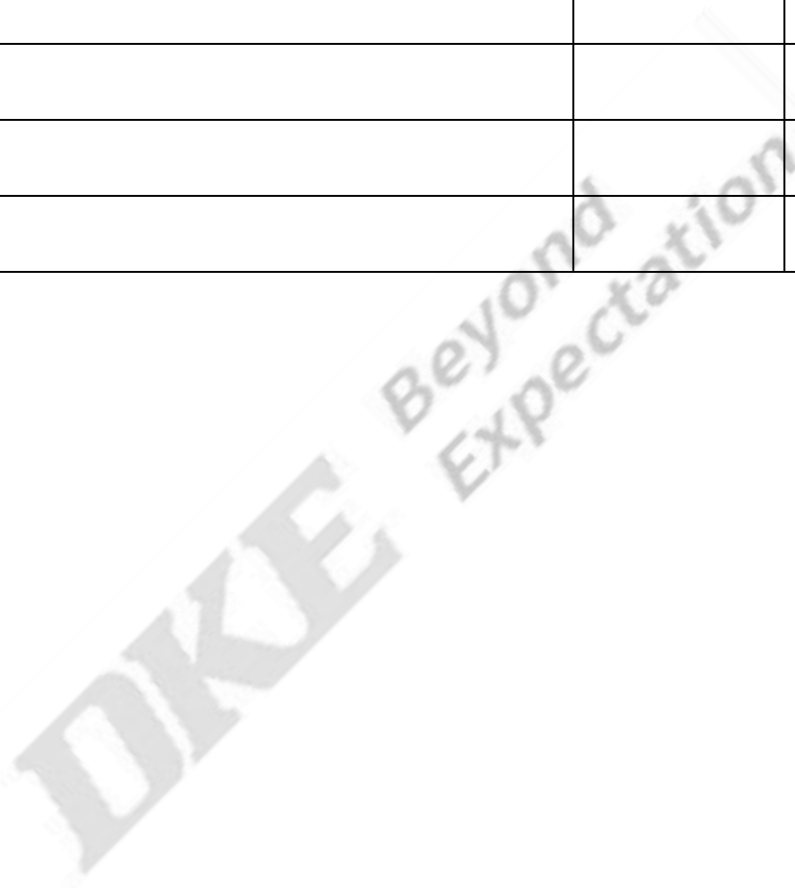
<b>Prepared by</b>	<b>Checked by</b>	<b>Approved by</b>

### **Customer approval:**

<b>Customer</b>	<b>Approved by</b>	<b>Date</b>

Revision History

<b>Version</b>	<b>Content</b>	<b>Date</b>	<b>Producer</b>
2.0	New release	2022/6/1	



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## 1. Over View

DEPG0350BNS850F0 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white and black full display capabilities. The 3.52inch active area contains 384×184 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

## 2. Features

- ◆ 384 × 184 pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator for generating VCOM, Gate and Source driving voltage
- ◆ I<sup>2</sup>C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor

### 3.Mechanical and Optical Specification

Parameter	Specifications	Unit	Remark
Screen Size	3.5	Inch	
Display Resolution	384(V)×184(H)	Pixel	DPI:120
Active Area	38.18×79.68	mm	
Pixel Pitch	0.207×0.207	mm	
Pixel Configuration	Rectangle		
Outline Dimension	45.03(H)×91.75 (V) ×0.90(D)	mm	
Weight	7.0±0.3	g	

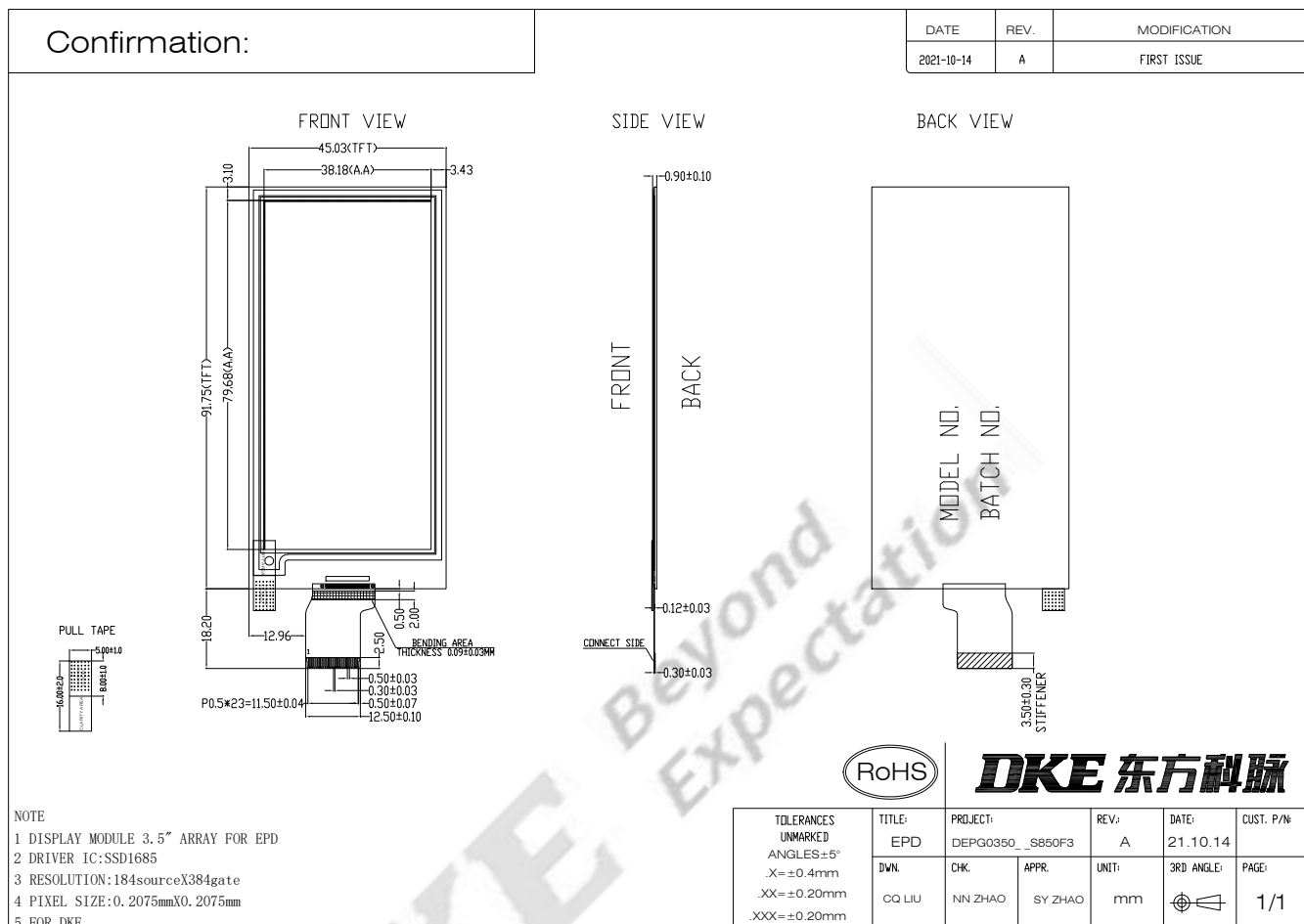
Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
KS	Black State L* value		-	18	20		3-1
	Black Ghosting $\Delta L$		-	1	-		3-1
WS	White State L* value		66	67	-		3-1
	White Ghosting $\Delta L$		-	1	-		3-1
R	White Reflectivity	White	30	34	-	%	3-1
CR	Contrast Ratio	Indoor	15:1	20:1	-		3-1
							3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3°C Humidity:55±10%RH		5years			3-3

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

4.Mechanical Drawing of EPD Module



## 5.Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage 2	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	Note 5-6
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	Note 5-6
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

**I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin**



**Note 5-1:** This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

**Note 5-2:** This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

**Note 5-3:** This pin (RES#) is reset signal input. The Reset is active low.

**Note 5-4:** This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor

**Note 5-5:** Bus interface selection pin

**Note 5-6:** This pin connect to the VSS if there is no external temperature sensor.

<b>BS1 State</b>	<b>MCU Interface</b>
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating

<b>Parameter</b>	<b>Symbol</b>	<b>Rating</b>	<b>Unit</b>
Logic supply voltage	VCI	-0.5 to +6.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	°C.
Storage Temp range	TSTG	-25 to+70	°C.
Optimal Storage Temp	TSTGo	23±3	°C.
Optimal Storage Humidity	HSTGo	55±10	RH

**Note:**

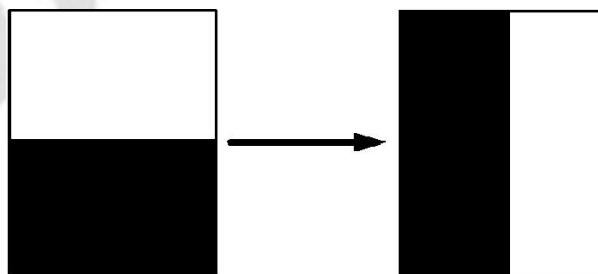
1. Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

## 6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR = 25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V <sub>SS</sub>	-		-	0	-	V
Logic supply voltage	V <sub>CI</sub>	-	V <sub>CI</sub>	2.2	3.0	3.7	V
Core logic voltage	V <sub>DD</sub>		V <sub>DD</sub>	1.7	1.8	1.9	V
High level input voltage	V <sub>IH</sub>	-	-	0.8 V <sub>CI</sub>	-	-	V
Low level input voltage	V <sub>IL</sub>	-	-	-	-	0.2 V <sub>CI</sub>	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100uA	-	0.9 V <sub>CI</sub>	-	-	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100uA	-	-	-	0.1 V <sub>CI</sub>	V
Typical power	P <sub>TYP</sub>	V <sub>CI</sub> = 3.0V	-	-	15	-	mW
Deep sleep mode	P <sub>STPY</sub>	V <sub>CI</sub> = 3.0V	-	-	0.003	-	mW
Typical operating current	I <sub>opr_VCI</sub>	V <sub>CI</sub> = 3.0V	-	-	5	-	mA
Image update time	-	25 °C	-	-	4	-	sec
Typical peak current	I <sub>opr_VCI</sub>	2.2~3.7v			40	50	mA
Minimum Power Consumption Spec	-	0°C	-	-	-	80	mAs
	-	10°C	-	-	-	60	mAs
	-	25°C	-	-	-	42	mAs
Sleep mode current	I <sub>slp_VCI</sub>	DC/DC off No clock No input load Ram data retain	-	-	20	-	uA
Deep sleep mode current	I <sub>dslp_VCI</sub>	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical characteristics are only guaranteed under the controller & waveform provided by DKE.
4. Electrical measurement: Tektronix oscilloscope - MDO3024,

Tektronix current probe - TCP0030A.

### 6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	TBD	-	V
Positive Source output voltage	V <sub>SH</sub>	-	S <sub>0</sub> ~S <sub>199</sub>	+14.5	+15	+15.5	V
Negative Source output voltage	V <sub>SL</sub>	-	S <sub>0</sub> ~S <sub>199</sub>	-15.5	-15	-14.5	V
Positive gate output voltage	V <sub>gh</sub>	-	G <sub>0</sub> ~G <sub>299</sub>	+19	+20	+21	V
Negative gate output voltage	V <sub>gl</sub>	-	G <sub>0</sub> ~G <sub>299</sub>	-21	-20	-19	V

Notes:VGH,VGL,VSH,VSL drop voltage<2V.

### 6.4 Panel AC Characteristics

#### 6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface			Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#	
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#	
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#	

#### 6.4.2 MCU Serial Interface (4-wire SPI)

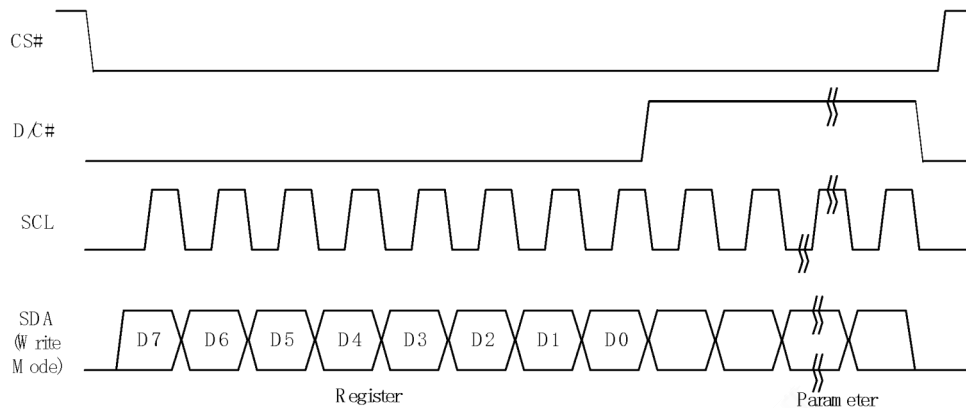
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

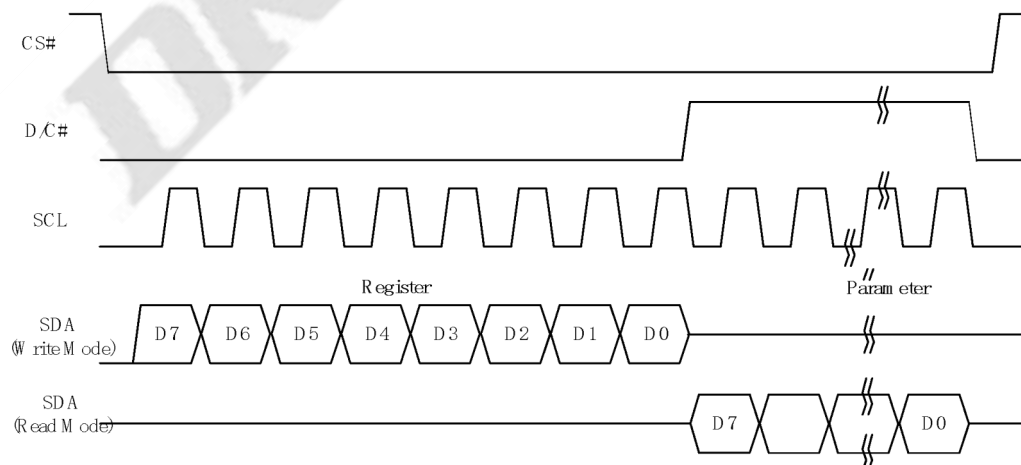
Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

**Figure 6-2: Read procedure in 4-wire SPI mode**



### 6.4.3 MCU Serial Interface (3-wire SPI)

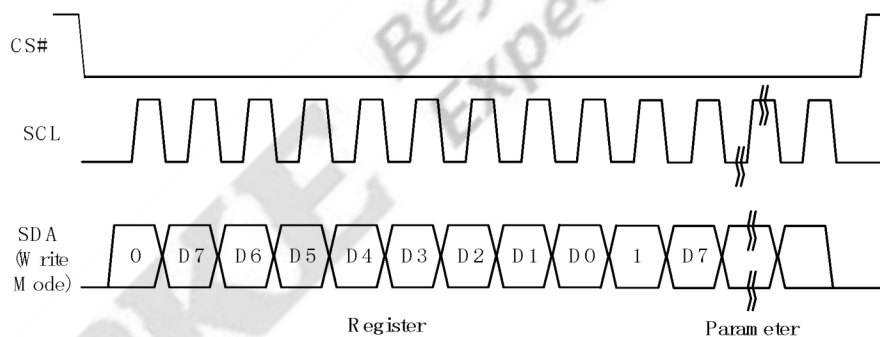
The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

**Note:** ↑ stands for rising edge of signal

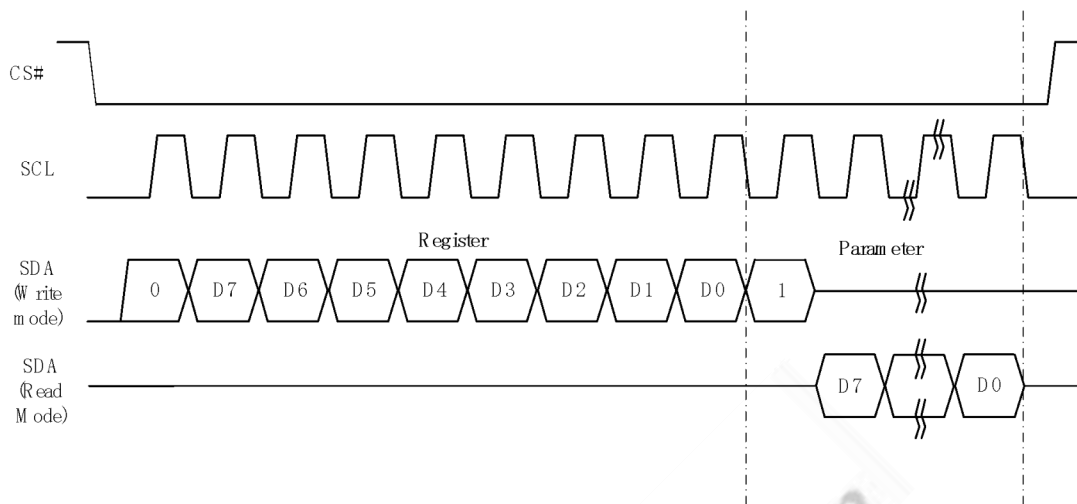
**Figure 6-3: Write procedure in 3-wire SPI mode**



In the Read mode:

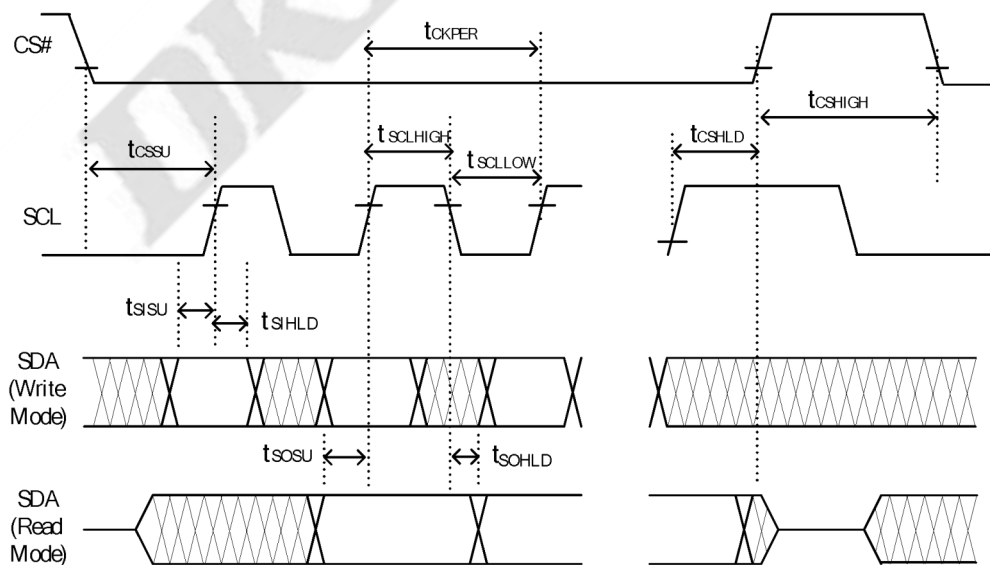
1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

Figure 6-4: Read procedure in 3-wire SPI mode



### 6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, T<sub>OPR</sub> =25°C.



Changed Diagram

**Serial Interface Timing Characteristics**

(VCI - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20pF)

**Write mode**

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	60			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

**Read mode**

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH H	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

**7.Command Table**

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 012Bh [POR], 300 MUX MUX Gate lines setting as (A[8:0] + 1). B [2:0] = 0000 [POR]. Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0, G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ... B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...G382, G299 (left and right gate interlaced) SM=1, G0, G2, G4 ...G382, G1, G3, ...G299 B[0]: TB TB = 0 [POR], scan from G0 to G299 TB = 1, scan from G299 to G0.
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	Set Gate Driving voltage A[4:0]=17h[POR],VGH at 20V[POR] VGH setting from 10V to 20V
0	1		0	0	0	A4	A3	A2	A1	A0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage control	Set Source Driving voltage A[7:0]= 41h[POR],VSH1 at 15V B[7:0]=A Ch[POR],VSH2 at 5.4V C[7:0]= 32h[POR], VSL at -15V
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		



0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting. A[7:0] -> Soft start setting for Phase1 = 8Bh [POR] B[7:0] -> Soft start setting for Phase2 = 9Ch [POR] C[7:0] -> Soft start setting for Phase3 = 96h [POR] D[7:0] -> Duration setting = 0Fh [POR] Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:																																														
0	1		1	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																																																
0	1		1	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>																																																
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<table border="1"> <thead> <tr> <th>Bit[6:4]</th><th>Driving Strength Selection</th></tr> </thead> <tbody> <tr><td>000</td><td>1(Weakest)</td></tr> <tr><td>001</td><td>2</td></tr> <tr><td>010</td><td>3</td></tr> <tr><td>011</td><td>4</td></tr> <tr><td>100</td><td>5</td></tr> <tr><td>101</td><td>6</td></tr> <tr><td>110</td><td>7</td></tr> <tr><td>111</td><td>8(Strongest)</td></tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Bit[3:0]</th><th>Min Off Time Setting of GDR [ Time unit ]</th></tr> </thead> <tbody> <tr><td>0000</td><td rowspan="2">NA</td></tr> <tr><td>~0011</td></tr> <tr><td>0100</td><td>2.6</td></tr> <tr><td>0101</td><td>3.2</td></tr> <tr><td>0110</td><td>3.9</td></tr> <tr><td>0111</td><td>4.6</td></tr> <tr><td>1000</td><td>5.4</td></tr> <tr><td>1001</td><td>6.3</td></tr> <tr><td>1010</td><td>7.3</td></tr> <tr><td>1011</td><td>8.4</td></tr> <tr><td>1100</td><td>9.8</td></tr> <tr><td>1101</td><td>11.5</td></tr> <tr><td>1110</td><td>13.8</td></tr> <tr><td>1111</td><td>16.5</td></tr> </tbody> </table> D[5:0]: duration setting of phase D[5:4]: duration setting of phase 3 D[3:2]: duration setting of phase 2 D[1:0]: duration setting of phase 1												Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)	Bit[3:0]	Min Off Time Setting of GDR [ Time unit ]	0000	NA	~0011	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5
Bit[6:4]	Driving Strength Selection																																																									
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01	20ms																																																									
10	30ms																																																									
11	40ms																																																									

0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	A <sub>1</sub>	A <sub>0</sub>		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR] A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor
			A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] = 7Fh [POR]
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		

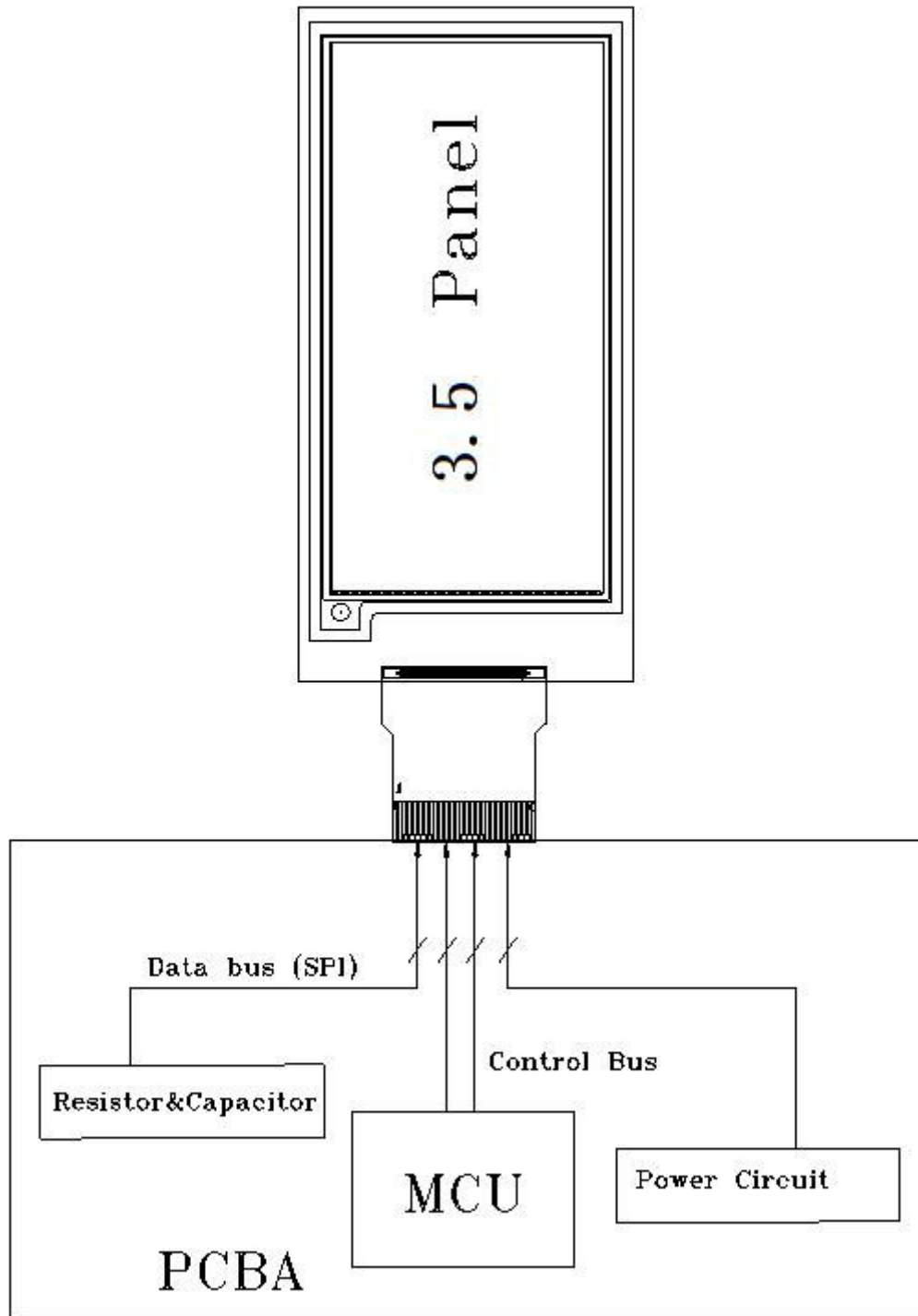
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.		
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR] A[7:4] Red RAM option		
0	1		A7	A6	A5	A4	A3	A2	A1	A0			0000	Normal
0	1		B7	B6	0	0	0	0	0	0			0100	Bypass RAM content as 0
													1000	Inverse RAM content
												A[3:0] BW RAM option		
												0000	Normal	
												0100	Bypass RAM content as 0	
												1000	Inverse RAM content	
												B[7:6] Resolution select		
												00	Display resolution is 200x384	
												01	Display resolution is 184x384	
												10	Display resolution is 168x384	
												11	Display resolution is 216x384	

0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR)																																																																													
	1		A7	A6	A5	A4	A3	A2	A1	A0			<table border="1"> <thead> <tr> <th>Operating sequence</th> <th>Parameter (in Hex)</th> </tr> </thead> <tbody> <tr> <td>Enable clock signal</td> <td>80</td> </tr> <tr> <td>Disable clock signal</td> <td>01</td> </tr> <tr> <td>Enable clock signal</td> <td>C0</td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Disable Analog</td> <td>03</td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>91</td> </tr> <tr> <td>Load LUT with DISPLAY Mode 1</td> <td></td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>99</td> </tr> <tr> <td>Load LUT with DISPLAY Mode 2</td> <td></td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>B1</td> </tr> <tr> <td>Load temperature value Load LUT with DISPLAY Mode 1</td> <td></td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>B9</td> </tr> <tr> <td>Load temperature value Load LUT with DISPLAY Mode 2</td> <td></td> </tr> <tr> <td>Disable clock signal</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>C7</td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Display with DISPLAY Mode 1</td> <td></td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>CF</td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Display with DISPLAY Mode 2</td> <td></td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>F7</td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Load temperature value DISPLAY with DISPLAY Mode 1</td> <td></td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> <tr> <td>Enable clock signal</td> <td>FF</td> </tr> <tr> <td>Enable Analog</td> <td></td> </tr> <tr> <td>Load temperature value DISPLAY with DISPLAY Mode 2</td> <td></td> </tr> <tr> <td>Disable Analog</td> <td></td> </tr> <tr> <td>Disable OSC</td> <td></td> </tr> </tbody> </table>	Operating sequence	Parameter (in Hex)	Enable clock signal	80	Disable clock signal	01	Enable clock signal	C0	Enable Analog		Disable Analog	03	Disable clock signal		Enable clock signal	91	Load LUT with DISPLAY Mode 1		Disable clock signal		Enable clock signal	99	Load LUT with DISPLAY Mode 2		Disable clock signal		Enable clock signal	B1	Load temperature value Load LUT with DISPLAY Mode 1		Disable clock signal		Enable clock signal	B9	Load temperature value Load LUT with DISPLAY Mode 2		Disable clock signal		Enable clock signal	C7	Enable Analog		Display with DISPLAY Mode 1		Disable Analog		Disable OSC		Enable clock signal	CF	Enable Analog		Display with DISPLAY Mode 2		Disable Analog		Disable OSC		Enable clock signal	F7	Enable Analog		Load temperature value DISPLAY with DISPLAY Mode 1		Disable Analog		Disable OSC		Enable clock signal	FF	Enable Analog		Load temperature value DISPLAY with DISPLAY Mode 2		Disable Analog	
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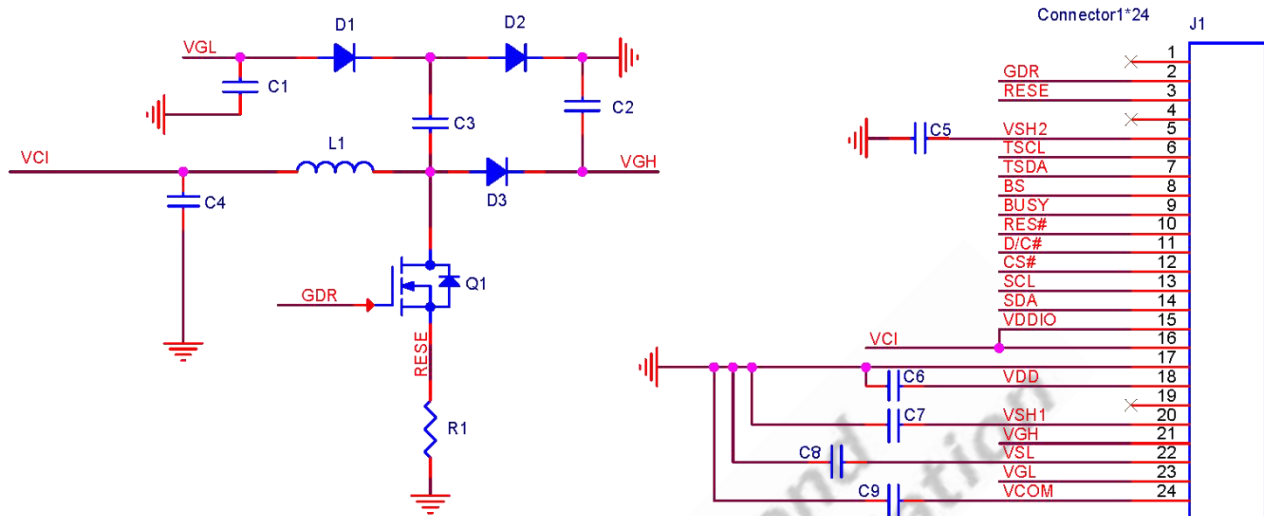
0	0	24	0	0	1	0	0	1	0	0	Write RAM (Black White) / RAM	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=4Bh
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.
1	1		0	0	A5	A4	0	0	A1	A0		

0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [227 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING																														
0	1		A7	A6	A5	A4	A3	A2	A1	A0																																
0	1		B7	B6	B5	B4	B3	B2	B1	B0																																
0	1		:	:	:	:	:	:	:	:																																
0	1		:	:	:	:	:	:	:	:																																
0	1		:	:	:	:	:	:	:	:																																
0	1		:	:	:	:	:	:	:	:																																
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option <table border="1" data-bbox="993 548 1373 814"> <thead> <tr> <th>A[7:6]</th><th>Select VBD as</th></tr> </thead> <tbody> <tr> <td>00</td><td>GS Transition, Defined in A[2] and A[1:0]</td></tr> <tr> <td>01</td><td>Fix Level Define A [5:4]</td></tr> <tr> <td>10</td><td>VCOM</td></tr> <tr> <td>11[POR]</td><td>HIZ</td></tr> </tbody> </table> A [5:4] Fix Level Setting for VBD <table border="1" data-bbox="993 846 1373 1010"> <thead> <tr> <th>A[5:4]</th><th>VBD level</th></tr> </thead> <tbody> <tr> <td>00</td><td>VSS</td></tr> <tr> <td>01</td><td>VSH1</td></tr> <tr> <td>10</td><td>VSL</td></tr> <tr> <td>11</td><td>VSH2</td></tr> </tbody> </table> A [1:0] GS Transition setting for VBD VBD Level Selection: 00b: VCOM ; 01b: VSH1; 10b: VSL; 11b: VSH2 <table border="1" data-bbox="993 1142 1448 1306"> <thead> <tr> <th>A[1:0]</th><th>VBD Transition</th></tr> </thead> <tbody> <tr> <td>00</td><td>LUT0</td></tr> <tr> <td>01</td><td>LUT1</td></tr> <tr> <td>10</td><td>LUT2</td></tr> <tr> <td>11</td><td>LUT3</td></tr> </tbody> </table>	A[7:6]	Select VBD as	00	GS Transition, Defined in A[2] and A[1:0]	01	Fix Level Define A [5:4]	10	VCOM	11[POR]	HIZ	A[5:4]	VBD level	00	VSS	01	VSH1	10	VSL	11	VSH2	A[1:0]	VBD Transition	00	LUT0	01	LUT1	10	LUT2	11	LUT3
A[7:6]	Select VBD as																																									
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00	LUT0																																									
01	LUT1																																									
10	LUT2																																									
11	LUT3																																									
0	1		A7	A6	A5	A4	0	0	A1	A0																																
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM A[5:0]: XSA[5:0], X Start, POR = 00h B[5:0]: XEA[5:0], X End, POR = 18h																														
0	1		0	0	A5	A4	A3	A2	A1	A0																																
0	1		0	0	B5	B4	B3	B2	B1	B0																																
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y-address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], Y Start, POR = 012Bh B[8:0]: YEA[8:0], Y End, POR = 0000h																														
0	1		A7	A6	A5	A4	A3	A2	A1	A0																																
0	1		0	0	0	0	0	0	0	A8																																
0	1		B7	B6	B5	B4	B3	B2	B1	B0																																
0	1		0	0	0	0	0	0	0	B8																																
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h																														
0	1		0	0	0	A4	A3	A2	A1	A0																																
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD[8:0], POR is 012Bh																														
0	1		A7	A6	A5	A4	A3	A2	A1	A0																																
0	1		0	0	0	0	0	0	0	A8																																

## 8. Block Diagram



## 9. Typical Application Circuit with SPI Interface

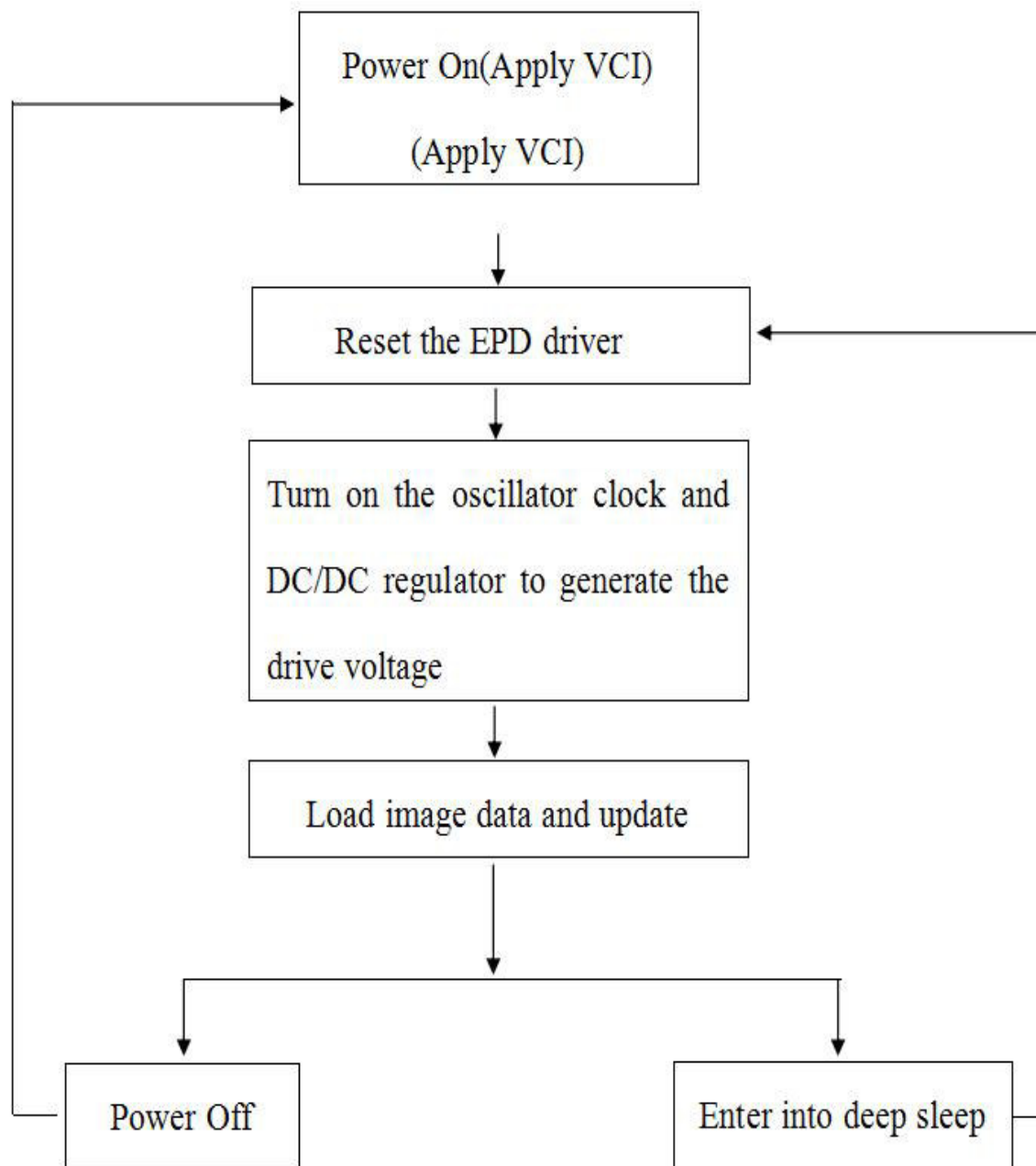


Part Name	Value	Reference Part	Requirements for spare part
C4 C6	1uF	X5R/X7R; Voltage Rating: 6v or 25v	
C1 C2 C3 C5 C7 C8	1uF	0402/0603/0805; X5R/X7R; Voltage Rating: 25v	
C9	0.47uF/1uF	0603/0805; X7R; Voltage Rating: 25v NOTE: Effective capacitance >0.25uF @18v DC bias	
R1	2.2Ohm	0402,0603,0805; 1% variation, $\geq 0.05W$	
D1 D2 D3	Diode	MBR0530	1) Reverse DC Voltage $\geq 30V$ 2) $I_o \geq 500mA$ 3) Forward voltage $\leq 430mV$
Q1	NMOS	Si1304BDL/NX3008NBK	1) Drain-Source breakdown voltage $\geq 30v$ 2) $V_{gs(th)} = 0.9v(Typ), 1.3v(Max)$ 3) $R_{ds\ on} \leq 2.1\Omega @ V_{gs} = 2.5v$
L1	47UH	CDRH2D18/LDNP-470NC	1) $I_o = 500mA(max)$



## 10. Typical Operating Sequence

### 10.1 LUT from OTP Operation Flow



**10.2 OTP Operation Reference Program Code**

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RES#	low	Hardware reset
delay	200us	
RES#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
SET VOLTAGE AND LOAD LUT		
LOAD IMAGE AND UPDATE		
Command 0x24	7500bytes	Load image (200/8*300)(BW)
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

## 11. Reliability Test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T = +70°C, RH=40% ,240h Test in white pattern
3	High-Temperature Operation	T = +50°C, RH = 30% ,240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=+40°C, RH=90%,240h
6	High Temperature, High Humidity Storage	T=+60°C, RH=80%,240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles Test in white pattern
8	ESD Gun	Air+/-4KV;Contact+/-2KV Contact+/-2KV(HBM C:100pF;R:1.5k ohm) Contact+/-200V(MM C:200pF;R:0 ohm) (Naked EPD display,including IC and FPC area)
9	UV exposure Resistance	762W/m <sup>2</sup> for 168 hrs,40°C Test in white pattern

**Note:** 1. Stay white pattern for storage and non-operation test.  
2. Operation is black→white pattern, the interval is 150s.

## 12. Quality Assurance

### 12.1 Environment

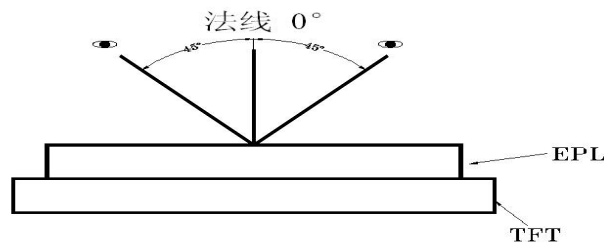
Temperature: 23±3°C

Humidity: 55±10%RH

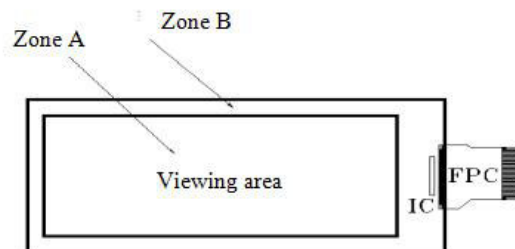
### 12.2 Illuminance

Brightness: 1200~1500LUX; distance: 20-30CM; Angle: Relate 45° surround.

### 12.3 Inspect method

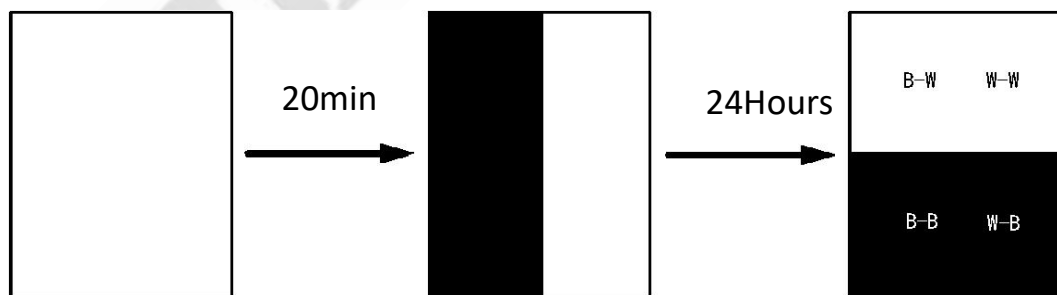


### 12.4 Display area



### 12.5 Ghosting test method

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by DKE.



1) Measurement Instruments: X-rite i1Pro

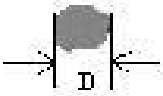
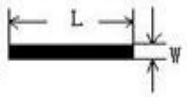
2) Ghosting formula:

W ghosting:  $\Delta L = \text{Max} (\Delta L(W-W, B-W)) - \text{Min} (\Delta L(W-W, B-W))$

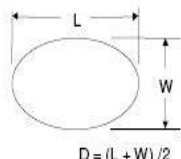
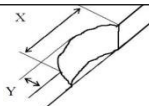
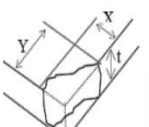
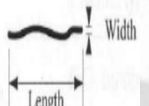


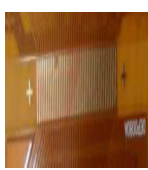
K ghosting:  $\Delta L = \text{Max} (\Delta L(W-B, B-B)) - \text{Min} (\Delta L(W-B, B-B))$

## 12.6 Inspection standard

### 12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	
2	Black/White spots	 $D \leq 0.25\text{mm}$ , Allowed $0.25\text{mm} < D \leq 0.4\text{mm}$ . $N \leq 4$ allowable $D > 0.4\text{mm}$ is not allowed	MI		
3	Show B/W lines	 $L \leq 0.4\text{mm}, W \leq 0.1\text{mm}$ negligible $0.4\text{mm} < L \leq 1.0\text{mm}$ $0.1\text{mm} < W \leq 0.4\text{mm}$ $N \leq 4$ allowable $L > 1.0\text{mm}, W > 0.4\text{mm}$ is not allowed		Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Shortcircuit/ Circuit break/ Display abnormal	Not Allow			

12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 <p><math>D = (L + W) / 2</math></p> <p><math>D \leq 0.25\text{mm}</math> negligible  <math>0.25\text{mm} &lt; D \leq 0.4\text{mm}</math> <math>N \leq 4</math> allowable  <math>D &gt; 0.4\text{mm}</math> is not allowed</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 <p><math>X \leq 3\text{mm}, Y \leq 0.5\text{mm}</math> And without affecting the electrode is permissible</p>  <p><math>2\text{mm} \leq X</math> or <math>2\text{mm} \leq Y</math> Not Allow</p>  <p><math>W \leq 0.1\text{mm}, L \leq 5\text{mm}</math>, No harm to the electrodes and <math>N \leq 2</math> allow</p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 <p>Not Allow</p>	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ Goldfingers oxidation/ scratch	  <p>Not Allow</p>	MA	Visual / Microscope	Zone B

8	B/W Line	 <p> <math>L \leq 1.0\text{mm}, W \leq 0.15\text{mm}</math> negligible  <math>1.0\text{mm} &lt; L \leq 4.0\text{mm}</math>  <math>0.15\text{mm} &lt; W \leq 0.5\text{mm}</math>  <math>N \leq 4</math> allowable  <math>L &gt; 4.0\text{mm}, W &gt; 0.5\text{mm}</math> is not allowed         </p>	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	<p>TFT edge bulge:  <math>X \leq 3\text{mm}, Y \leq 0.3\text{mm}</math> Allowed            TFT chromatic aberration :Allowed</p>	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	<p> <math>D \leq 0.25\text{mm}</math>, allow  <math>0.25\text{mm} &lt; D \leq 0.4\text{mm}, n \leq 4</math> allow  <math>D &gt; 0.4\text{mm}</math> is not allowed            (<math>n \leq 8</math> items are allowed within 5 mm in diameter)         </p>	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	<p>PCB (Circuit area) damaged Not Allow            PCB Poor welding Not Allow            PCB Curl <math>\leq 1\%</math></p>			
12	Edge glue height/ Edge glue bubble	<p>Edge Adhesives <math>H \leq</math> PS surface (Including protect film) Edge adhesives seep in <math>\leq 1/2</math> Margin width            Length excluding            Edge adhesives bubble: bubble Width  <math>\leq 1/2</math> Margin width; Length <math>\leq 0.5\text{mm}</math>. <math>n \leq 5</math></p>	MI	Visual / Ruler	Zone B
13	Protect film	Surface scratch but not effect protect function, Allowed		Visual Inspection	
14	Silicon glue	<p>Thickness <math>\leq</math> PS surface (With protect film): Full cover the IC;            Shape:            The width on the FPC <math>\leq 0.5\text{mm}</math> (Front)            The width on the FPC <math>\leq 1.0\text{mm}</math> (Back)            smooth surface, No obvious raised.</p>	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 <p> <math>t \leq 1.0\text{mm}</math> </p>	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	


**13.Packaging**

<b>EPD PACKING INSTRUCTION</b>					DATE	
DKE-QS. D-010					DESIGN	
					CHECKED	
					APPROVED	

P/N	Customer Code	Ref. P/N	Type	PKG Method	Marking	Surface Marks	Pull Tape
DEPG0350			GLASS	Blister	BACK	None	YES

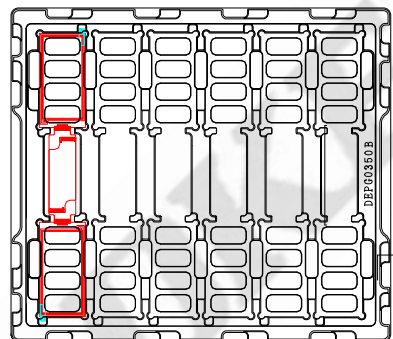
Packing Materials List					12PCS/LAYER, 20LAYER/CTN, TOTAL 240PCS/CTN.	
List	Model	Materials	Q'ty	Unit	Pull tape: 	
Carton	7# 417*362*229 mm	corrugate	1	Piece		
Inner Carton	7# (INNER) 400*343 *95 mm	corrugate	2	Piece		
Blister	DEPG0350B	PET	22	Piece		
Thin foam	272.41*311.43*T1.5~1.8	EPE	20	Piece		
Antistatic vacuum bag	450*590*0.075		2	Piece		
Foam board	DKE2251-10	EPE	3	Piece		
PULL TAPE	16*5*T0.05		240	Piece		

**Detail:**

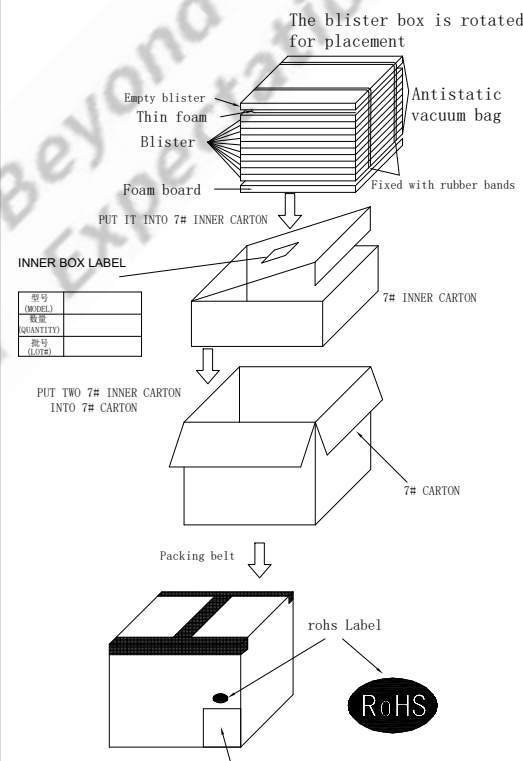
**Blister box:**

Note: there are 20 layers of products, divided into 2 inner boxes, and an empty blister box is placed on the top of each inner box, so the number of blister boxes is 22



QUANTITY: 12PCS

The blister box is rotated for placement



INNER BOX LABEL

型号 (MODEL)	
数量 (QUANTITY)	
批号 (LOT#)	

Shipping marks according to customer's requirements

Epaper Identification	
QC:	PASS
Model No.	_____
Quantity	_____ pcs
Date:	_____
Carton No.	_____ of _____



## 14. Handling, Safety, and Environment Requirements

### Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

### Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

<b>Data sheet status</b>	
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
<b>Product Environmental certification</b>	
ROHS	
<b>REMARK</b>	
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.	
<b>Transport environment</b>	
When the humidity of transportation environment is between 45%RH~70%RH, the product can be stored for 30 days, and the product can be stored for 10 days if it is lower or higher than this range	



ALL TECHNOLOGIES. ALL COMPETENCIES. ONE SPECIALIST.



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