

# Specification

## **G104XCE-LM1**

10,4" - 1024 x 768 – LVDS

Spec Revision: 2.2

Revision Date: 13.09.2023

Note: This specification is subject to change without prior notice

Doc. Number :

- ☐ Tentative Specification  
☐ Preliminary Specification  
☒ Approval Specification

**MODEL NO.: G104XCE**  
**SUFFIX: LM1**

**Customer: Common**

**APPROVED BY**

**SIGNATURE**

Name / Title

Note

Product Version

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
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## REVISION HISTORY

[illegible]


## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

G104XCE- LM1 is a 10.4" IAV TFT Liquid Crystal Display module with LED backlight unit and 30-pin-and-1ch LVDS interface. This product supports 1024 x 768 XGA format and can display true 16.7M colors. The PSWG is to establish a set of displays with standard mechanical dimensions and select electrical interface requirements for an industry standard 10.4" XGA LCD panel and the LED driving device for Backlight is built in PCBA.

### 1.2 FEATURES

- Excellent brightness (350 nits)
- Ultra high contrast ratio (1000:1)
- Fast response time ( $T_R + T_F = 25$  ms)
- XGA (1024 x 768 pixels) resolution
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- PSWG (Panel Standardization Working Group)
- Ultra wide viewing angle: 176(H)/ 176(V) (CR>10) AAS technology
- 180 degree rotation display option
- Wide operation temperature

### 1.3 APPLICATION

- TFT LCD monitor
- Slim design display for portable applications

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	210.432 (H) x 157.824 (V) (10.4" diagonal)	mm	(1)
Bezel Opening Area	215.4 (H) x 161.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1024 x R.G.B. x 768	pixel	-
Pixel Pitch (Sub Pixel)	0.0685 (H) x 0.2055 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262K/16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti Glare	-	-
Total power consumption	Total 6.4W(Typ) @cell 1.9W (Typ), BL 4.5W (Typ)	W	typ

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

### 1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	238.1	238.6	239.1	mm	(1)
	Vertical (V)	175.3	175.8	176.3	mm	
	Depth (D)	6.97	7.47	7.97	mm	-
Weight			318	334	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

## 2. ABSOLUTE MAXIMUM RATINGS

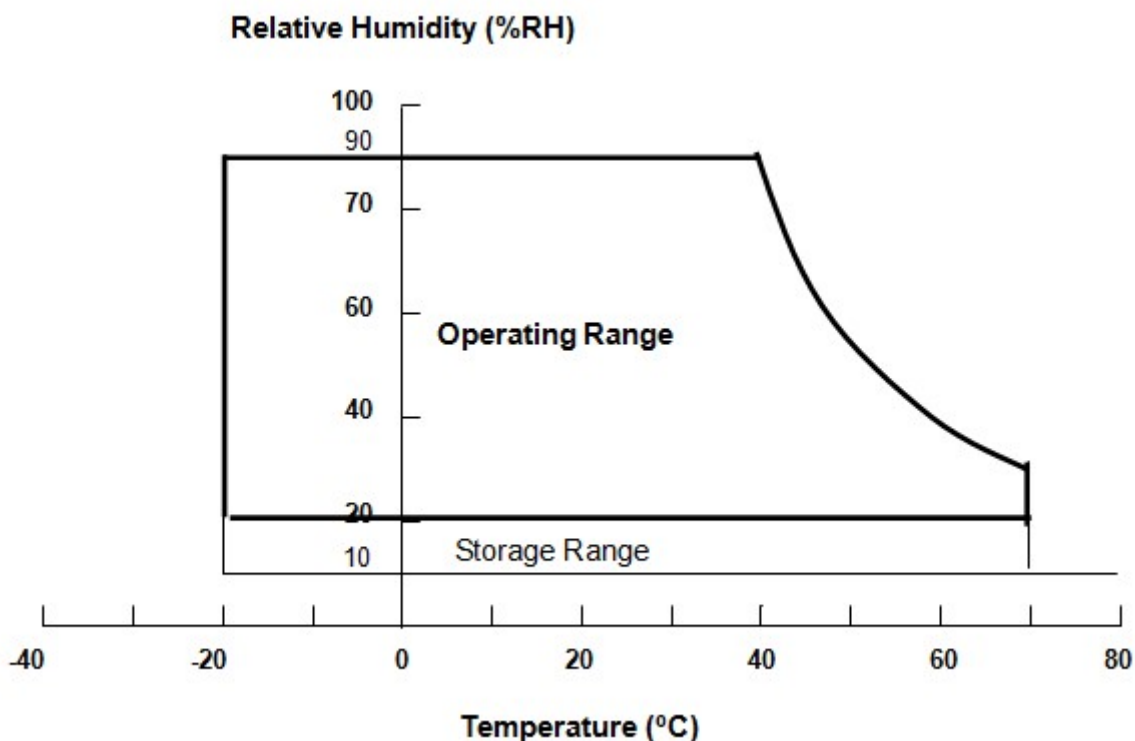
### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Operating Ambient Temperature	T <sub>OP</sub>	-20	+70	°C	(1)(2)
Storage Temperature	T <sub>ST</sub>	-20	+70	°C	

Note (1)

- (a) 90 %RH Max.
- (b) Wet-bulb temperature should be 39 °C Max.
- (c) No condensation.

Note (2) Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 70°C . ( Panel sureface temperature )





## 2.2 ELECTRICAL ABSOLUTE RATINGS

### 2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V <sub>CC</sub>	-0.3	4.0	V	(1)
Logic Input Voltage	V <sub>IN</sub>	-0.3	4.0	V	

### 2.2.2 LED CONVERTER

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Converter Voltage	V <sub>i</sub>	-0.3	18	V	(1), (2)
Enable Voltage	EN	-0.3	5.5	V	
Backlight Adjust	ADJ	-0.3	5.5	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED light bar (Refer to 3.2 for further information).

## 3. ELECTRICAL CHARACTERISTICS

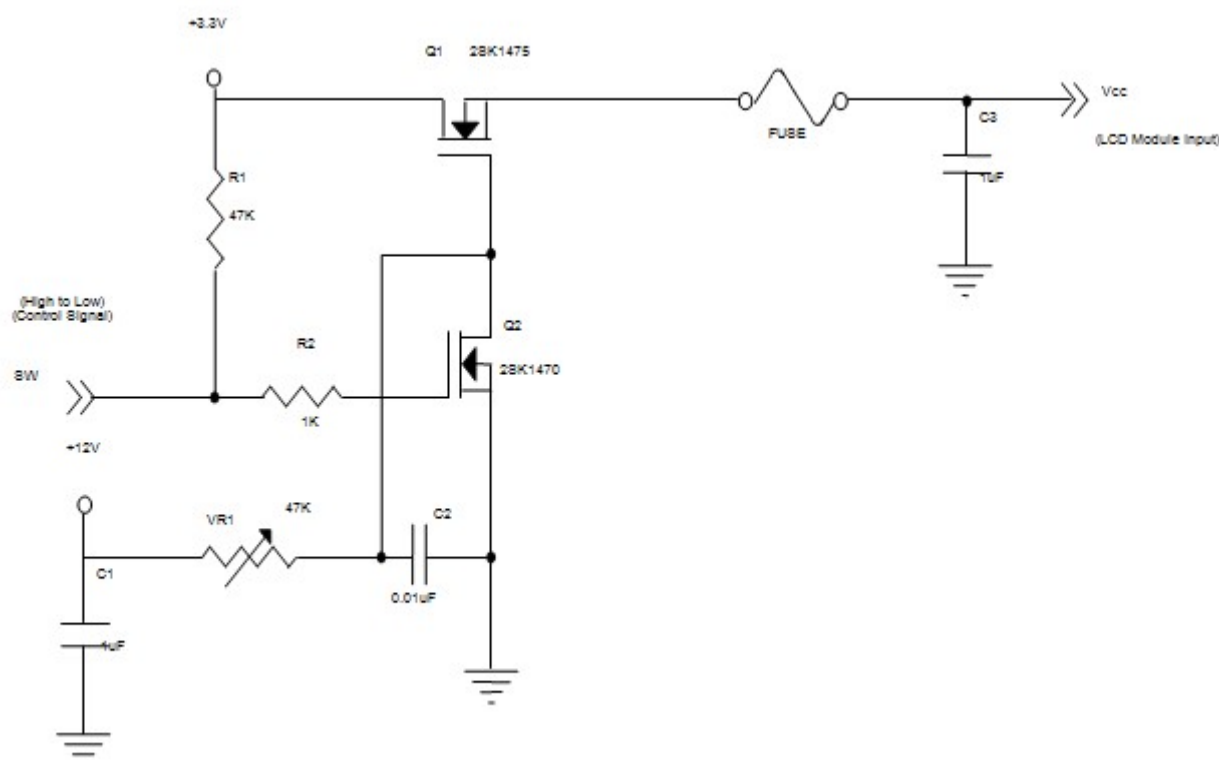
### 3.1 TFT LCD MODULE

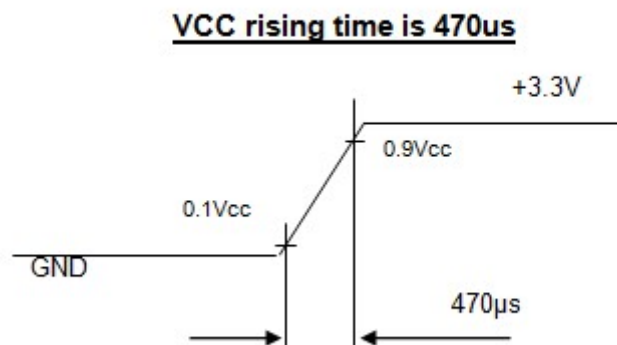
Ta = 25 ± 2 °C

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	3.0	3.3	3.6	V	(1)
Power Supply Ripple Voltage		VRP	-	-	100	mV	
Rush Current		IRUSH	-	-	4.0	A	(2)
Power Supply Current	White	ICC	-	575	690	mA	(3)
	Black		-	445	535	mA	
Power Consumption		PL	-	1.9	2.28	W	
LVDS differential input voltage		Vid	100	-	600	mV	
LVDS common input voltage		Vic	1.0	1.2	1,4	V	
Logic High Input Voltage		VIH	2.3	-	VCC	V	
Logic Low Input Voltage		VIL	0	-	0.7	V	
LVDS terminating resistor		RT	-	100	-	ohm	

Note (1) The assembly should be always operated within above ranges.

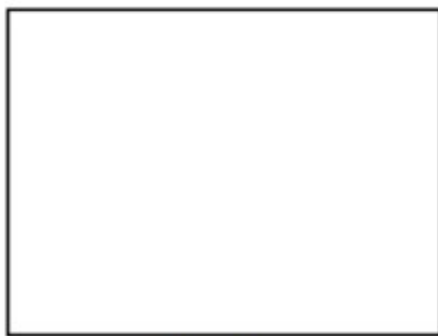
Note (2) Measurement Conditions:





Note (3) The specified power supply current is under the conditions at  $V_{cc} = 3.3\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ ,  $f_v = 60\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

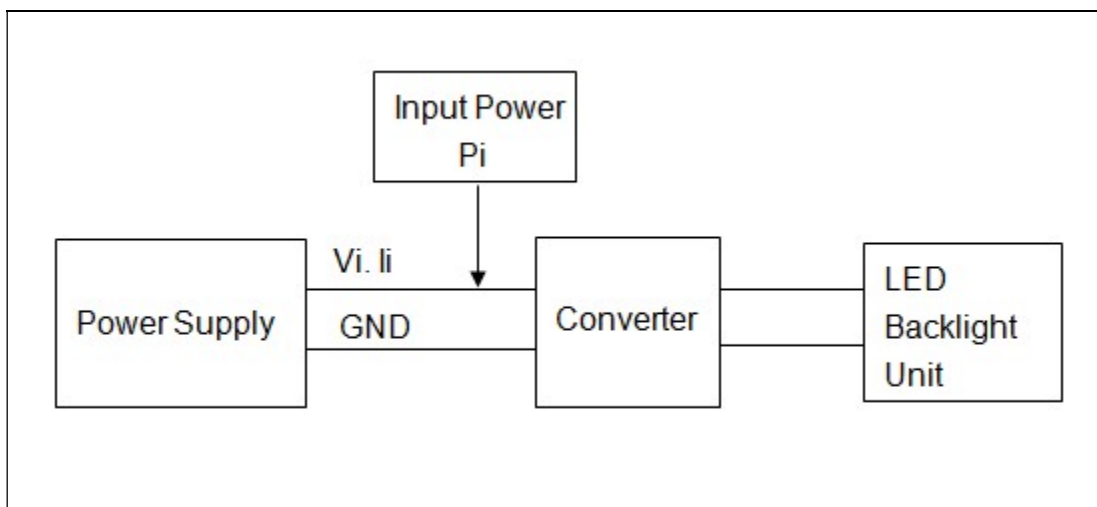


Active Area

## 3.2 BACKLIGHT UNIT

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Voltage		$V_i$	10.8	12.0	13.2	V	(Duty 100%)
Converter Input Ripple Voltage		$V_{iRP}$	-	-	350	mV	
Converter Input Current		$I_i$	-	0.38	0.44	A	@ $V_i = 12V$ (Duty 100%)
Converter Inrush Current		$I_{iRUSH}$	-	-	3.0	A	@ $V_i$ rising time = 20ms ( $V_i = 12V$ )
Input Power Consumption		PBL	-	4.5	5.3	W	(1)
EN Control Level	Backlight on	ENLED	2.5	3.3	5.0	V	
	Backlight off	(BLON)	0	-	0.3	V	
PWM Control Level	PWM High Level	Dimming	2.5	3.3	5.0	V	
	PWM Low Level	(E_PWM)	0	-	0.15	V	
PWM Noise Range		VNoise	-	-	0.1	V	
PWM Control Frequency		fPWM	190	200	20k	Hz	(2)
PWM Control Duty Ratio		-	5		100	%	(2), Suggestion @ 190Hz < f <sub>PWM</sub> < 1kHz
			20	-	100	%	(2), @ 1kHz ≤ f <sub>PWM</sub> < 20kHz
LED Life Time		LL	50,000	-	-	Hrs	(3)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) At 190 ~1kHz PWM control frequency, duty ratio range is restricted from 5% to 100%.

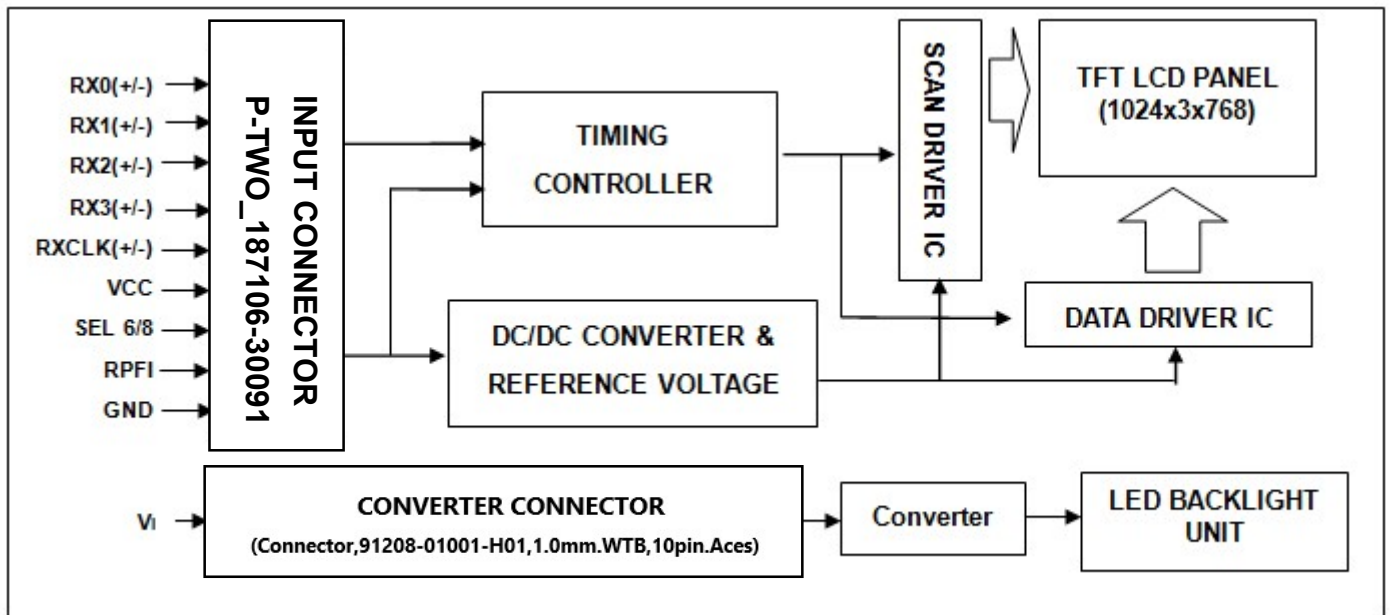
1K ~20kHz PWM control frequency, duty ratio range is restricted from 20% to 100%.

If PWM control frequency is applied in the range from 1KHz to 20KHz, The “non-linear” phenomenon on the Backlight Unit may be found. So It’s a suggestion that PWM control frequency should be less than 1KHz.

Note (3) The lifetime of LED is estimated data and defined as the time when it continues to operate under the conditions at  $T_a = 25 \pm 2 \text{ }^\circ\text{C}$  and Duty 100% until the brightness becomes  $\leq 50\%$  of its original value. Operating LED at high temperature condition will reduce life time and lead to color shift.

#### 4. BLOCK DIAGRAM

##### 4.1 TFT LCD MODULE



## 5. INTERFACE PIN ASSIGNMENT

### 5.1 TFT LCD MODULE

#### J1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VCC	Power supply: +3.3V	-
2	VCC	Power supply: +3.3V	-
3	VCC	Power supply: +3.3V	-
4	GND	Ground	-
5	GND	Ground	-
6	GND	Ground	-
7	RPFI	Reverse Panel Function (Display Rotation)	( 3 )
8	NC	No Connection	( 4 )
9	NC	No Connection	( 4 )
10	NC	No Connection	( 4 )
11	SEL6/8	LVDS 6/8 bit select function control, Low or NC → 8 bit Input Mode High → 6bit Input Mode	( 3 )
12	GND	Ground	-
13	NC	No Connection	( 4 )
14	GND	Ground	-
15	RX0-	Negative transmission data of pixel 0	-
16	RX0+	Positive transmission data of pixel 0	-
17	GND	Ground	-
18	RX1-	Negative transmission data of pixel 1	-
19	RX1+	Positive transmission data of pixel 1	-
20	GND	Ground	-
21	RX2-	Negative transmission data of pixel 2	-
22	RX2+	Positive transmission data of pixel 2	-
23	GND	Ground	-
24	RXCLK-	Negative of clock	-
25	RXCLK+	Positive of clock	-
26	GND	Ground	-
27	RX3-	Negative transmission data of pixel 3	-
28	RX3+	Positive transmission data of pixel 3	-
29	GND	Ground	-
30	NC	No Connection	( 4 )

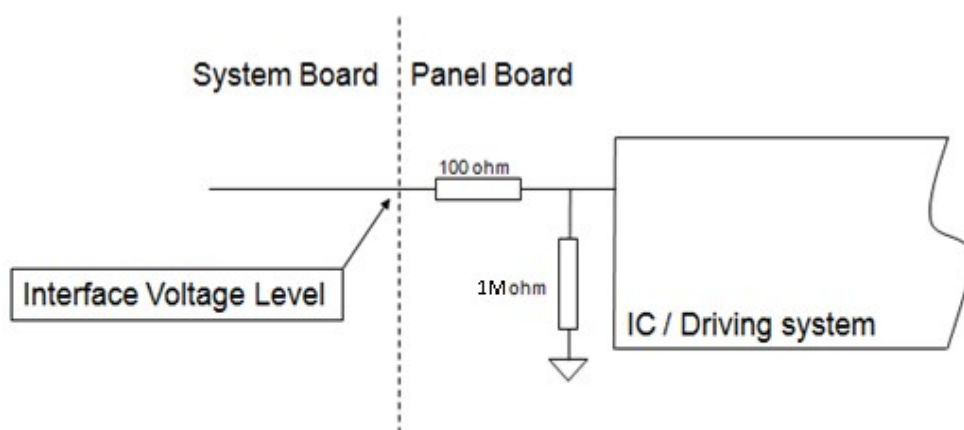
Note (1) Connector Part No.: P-TWO 187106-30091 or STM, MSCK2407P30.D or equivalent.

Note (2) User's connector Part No.: JAE FI-X30H(L) or equivalent.

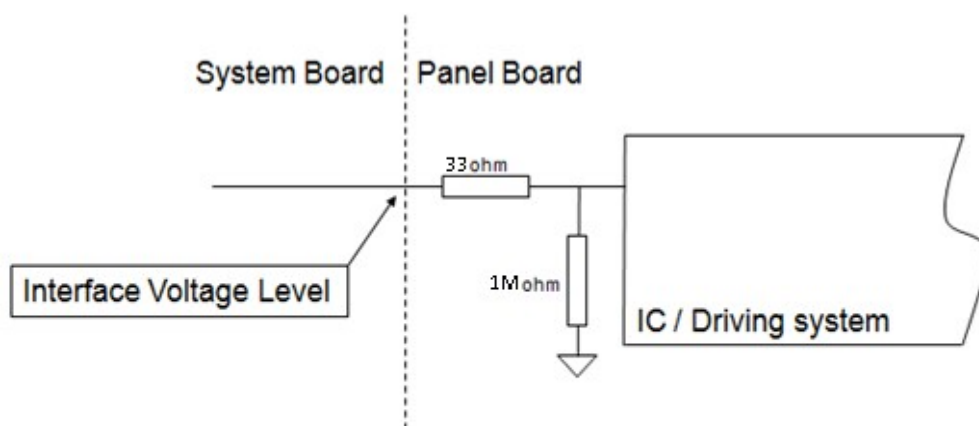
Note (3) "Low" stands for 0V. "High" stands for 3.3V. "NC" stands for "No Connected". The pin setting needs to be synchronized or leading with "Vcc".

Note (4) Pin8, Pin9, Pin10, Pin13, Pin30 input signals should be set to no connection or ground, this module would operate normally.

RPFI pin:



SEL6/8 pin:



## 5.2 BACKLIGHT UNIT (CONVERTER CONNECTOR PIN)

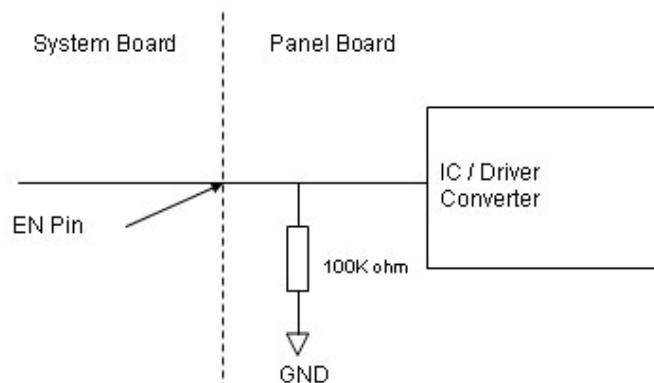
Pin	Symbol	Description	Remark
1	$V_i$	Converter input voltage	12V
2	$V_i$	Converter input voltage	12V
3	$V_i$	Converter input voltage	12V
4	$V_i$	Converter input voltage	12V
5	$V_{GND}$	Converter ground	Ground
6	$V_{GND}$	Converter ground	Ground
7	$V_{GND}$	Converter ground	Ground
8	$V_{GND}$	Converter ground	Ground
9	EN	Enable pin	3.3V, Note (3)
10	ADJ	Backlight Adjust	PWM Dimming (190-210Hz, Hi: 3.3VDC, Lo: 0VDC) , Note (3)

Note (1) Connector Part No.: ACES,91208-01001-H01 or equivalent

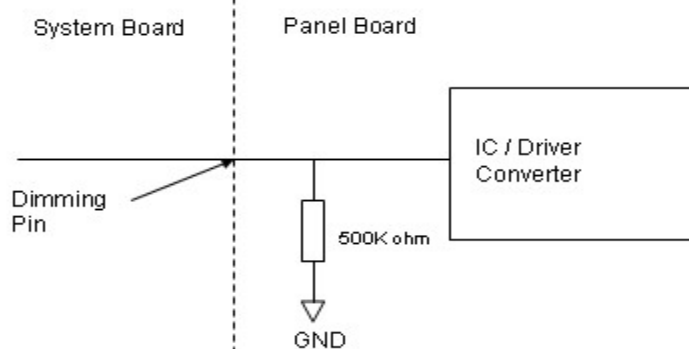
Note (2) User's connector Part No.: ACES,91209-01011 or equivalent

Note (3) EN(BLON), ADJ(E\_PWM) as shown below :

## BLON Pin



## E\_PWM Pin





## 5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS

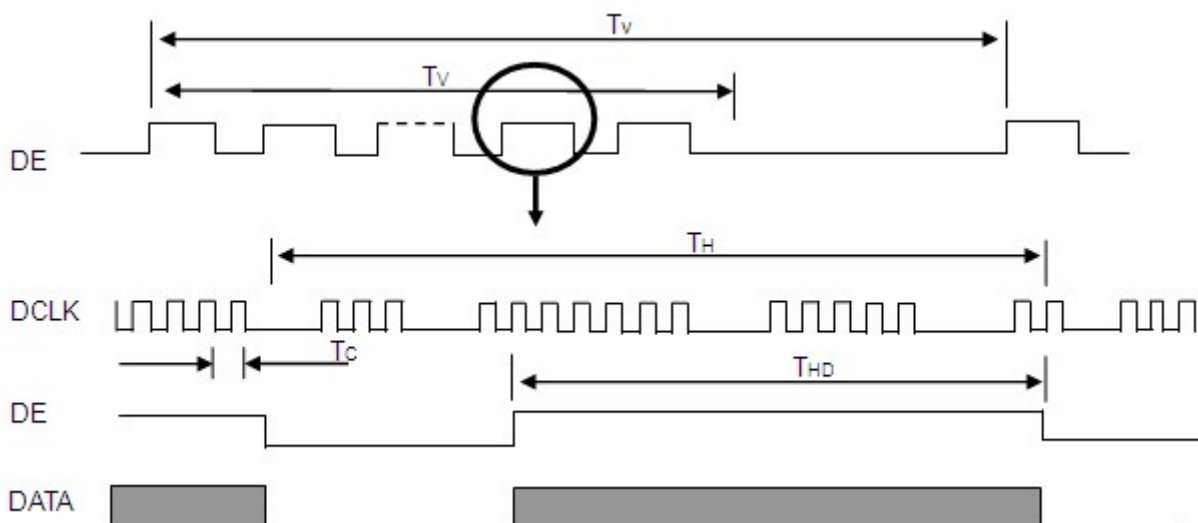
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	$F_c$	57.7	65	73.6	MHz	-
	Period	$T_c$	13.6	15.4	17.3	ns	
	Input cycle to cycle jitter	$T_{rd}$	---	---	200	ns	(a)
	Input Clock to data skew	TLVCCS	$-0.02 \cdot T_c$	---	$0.02 \cdot T_c$	ps	(b)
	Spread spectrum modulation range	$F_{clk\_mod}$	$0.987 \cdot F_c$	---	$1.013 \cdot F_c$	MHz	(c)
	Spread spectrum modulation frequency	$F_{SSM}$	---	---	200	KHz	
	High Time	$T_{ch}$	---	4/7	---	$T_{ch}$	
	Low Time	$T_{cl}$	---	3/7	---	$T_{ch}$	
Vertical Display Term	Frame Rate	$Fr$	---	60	---	Hz	$T_v = T_{vd} + T_{vb}$
	Total	$T_v$	776	806	838	Th	-
	Active Display	$T_{vd}$	768	768	768	Th	-
	Blank	$T_{vb}$	8	38	70	Th	-
Horizontal Display Term	Total	$T_h$	1240	1344	1464	Tc	$T_h = T_{hd} + T_{hb}$
	Active Display	$T_{hd}$	1024	1024	1024	Tc	-
	Blank	$T_{hb}$	216	320	440	Tc	-

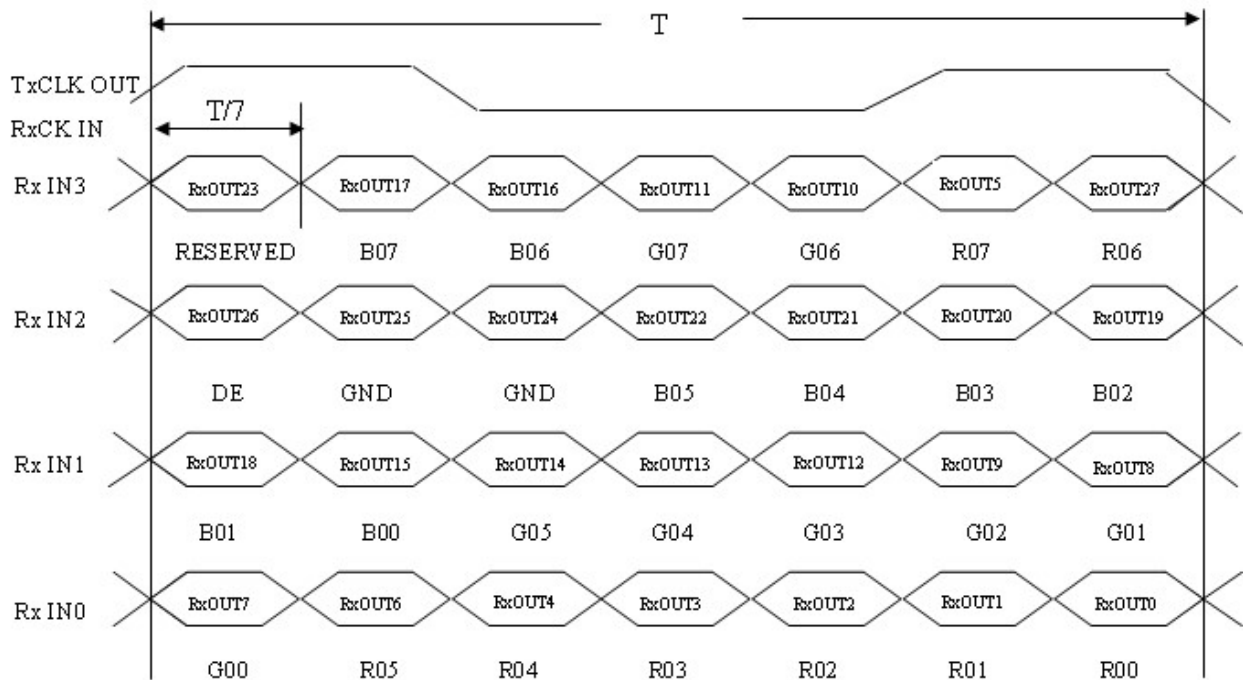
Note (1) Because this module is operated by DE only mode, Hsync and Vsync input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note (2) The  $T_v(T_{vd} + T_{vb})$  must be integer, otherwise, the module would operate abnormally.

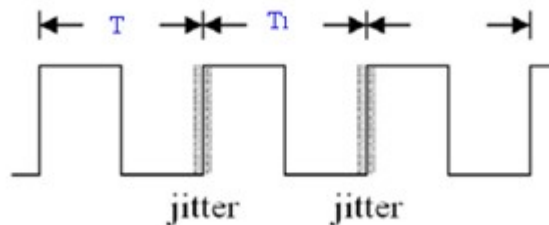
### INPUT SIGNAL TIMING DIAGRAM



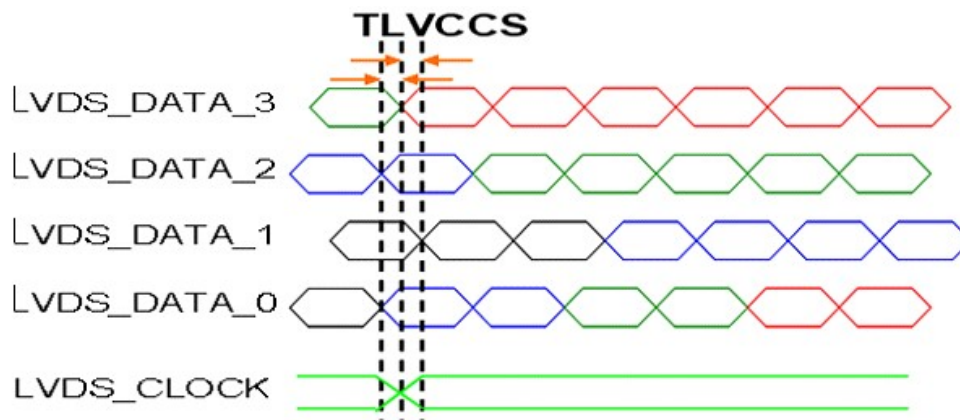
## TIMING DIAGRAM of LVDS



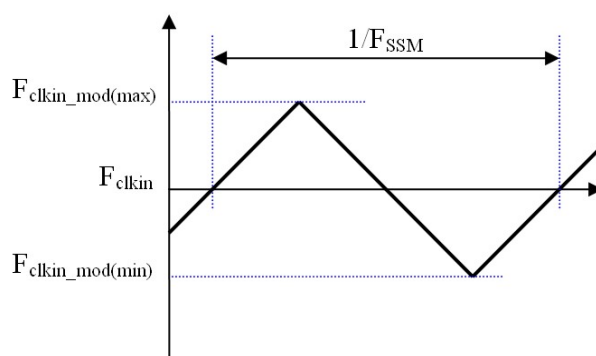
Note (a) The input clock cycle-to-cycle jitter is defined as below figures.  $Trcl = |T_1 - T_1|$



Note (b) Input Clock to data skew is defined as below figures.



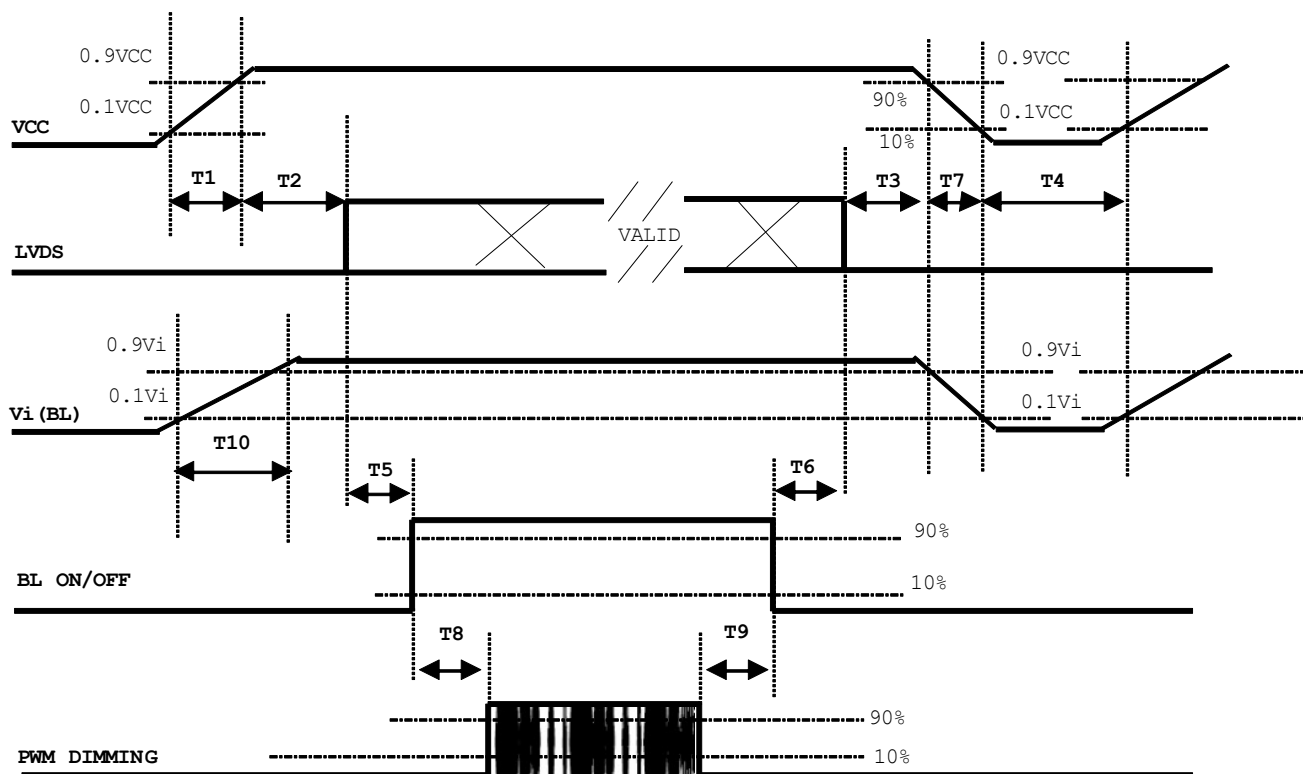
Note (c) The SSCG (Spread spectrum clock generator) is defined as below figures.



## 6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.

**Power ON/OFF sequence**



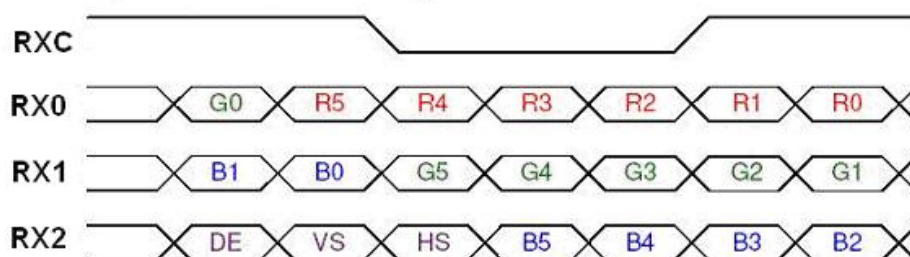
**Note:**

- (1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.
- (2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.
- (6) INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.
- (7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec".

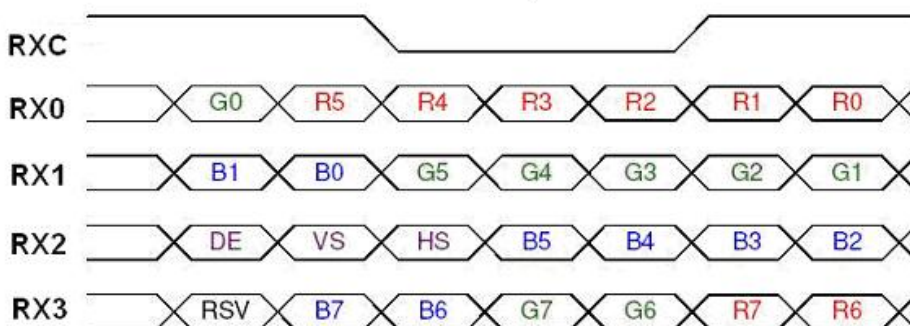
Parameter	Value			Units
	Min	Typ	Max	
T1	0.5	---	10	ms
T2	0	---	50	ms
T3	0	---	50	ms
T4	500	---	---	ms
T5	450	---	---	ms
T6	200	---	---	ms
T7	10	---	100	ms
T8	10	---	---	ms
T9	10	---	---	ms
T10	20	---	50	ms

## 6.3 THE INPUT DATA FORMAT

### SEL 6/8 = “High” for 6 bits LVDS Input



### SEL 6/8 = “Low” or “NC” for 8 bits LVDS Input



Note (1) R/G/B data 7: MSB, R/G/B data 0: LSB

Note (2) Please follow PSWG

Signal Name	Description	Remark
R7 R6 R5 R4 R3 R2 R1 R0	Red Data 7 (MSB) Red Data 6 Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB)	Red-pixel Data Each red pixel's brightness data consists of these 8 bits pixel data.
G7 G6 G5 G4 G3 G2 G1 G0	Green Data 7 (MSB) GreenData 6 GreenData 5 GreenData 4 GreenData 3 GreenData 2 GreenData 1 GreenData 0 (LSB)	Green-pixel Data Each green pixel's brightness data consists of these 8 bits pixel data.
B7 B6 B5 B4 B3 B2 B1 B0	Blue Data 7 (MSB) Blue Data 6 Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	Blue-pixel Data Each blue pixel's brightness data consists of these 8 bits pixel data.
RXCLKIN+ RXCLKIN-	LVDS Clock Input	
DE	Display Enable	
VS	Vertical Sync	
HS	Horizontal Sync	



## 6.4 SCANNING DIRECTION

The following figures show the image see from the front view. The arrow indicates the direction of scan.

**Fig.1 Normal Scan**



PCBA on the bottom side

**Fig.2 Reverse Scan**



PCBA on the bottom side

Fig. 1 Normal scan ( pin 7, RPFI = Low or NC )

Fig. 2 Reverse scan (pin 7, RPFI = High )

## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value and tolerance in "ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

### 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2 and all items are measured at the center point of screen except white variation. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rx	$\theta X=0^{\circ}, \theta Y=0^{\circ}$ Grayscale Maximum	0.599	0.649	0.699	-	(1), (5)
		Ry		0.290	0.340	0.390		
	Green	Gx		0.270	0.320	0.370		
		Gy		0.556	0.606	0.656		
	Blue	Bx		0.099	0.149	0.199		
		By		0.005	0.055	0.105		
	White	Wx		0.263	0.313	0.363		
		Wy		0.279	0.329	0.379		
Center Luminance of White		LC	300	350	-		(4), (5)	
Contrast Ratio		CR	700	1000	-		(2), (5)	
Response Time		TR	$\theta X=0^{\circ}, \theta Y=0^{\circ}$	-	13	18	-	(3)
		TF		-	12	17	-	
White Variation		$\delta W$	$\theta X=0^{\circ}, \theta Y=0^{\circ}$	72	80	-	%	(5), (6)
Viewing Angle	Horizontal	$\theta X+$	$CR \geq 10$	80	89	-	Deg.	(1), (5)
		$\theta X-$		80	89	-		
	Vertical	$\theta Y+$		80	89	-		
		$\theta Y-$		80	89	-		

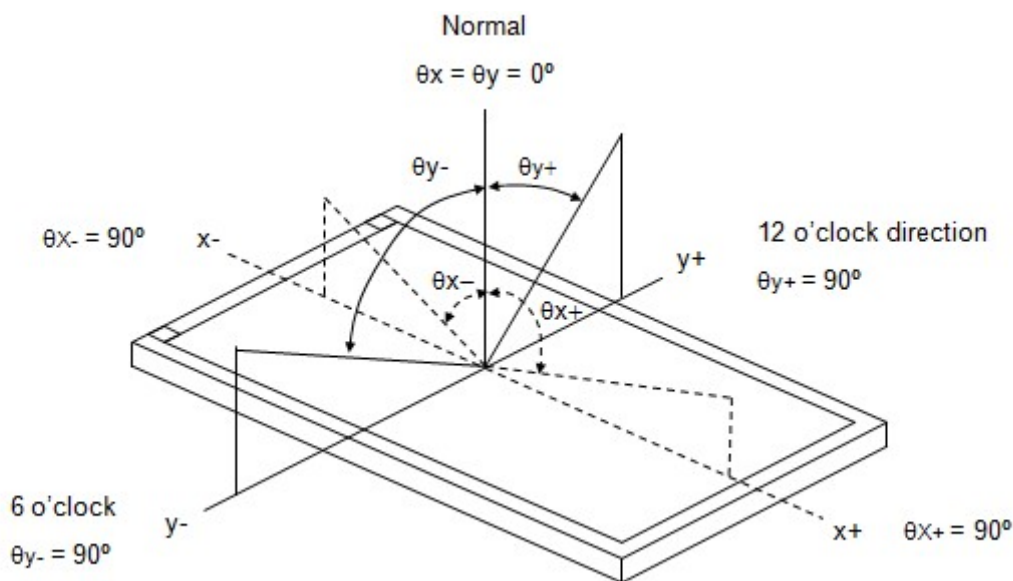
Definition :

Grayscale Maximum : Grayscale 255 (10 bits: grayscale 1023 ; 8 bits : grayscale 255 ; 6 bits: grayscale 63)

White : Luminance of Grayscale Maximum (All R,G,B)

Black : Luminance of grayscale 0 (All R,G,B)

Note (1) Definition of Viewing Angle ( $\theta_x$ ,  $\theta_y$ ):

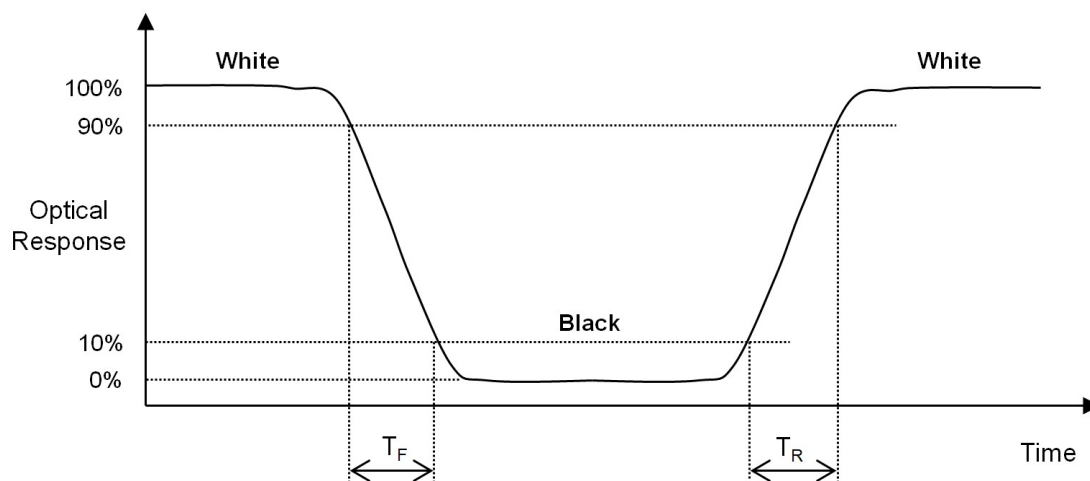


Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression at center point.

Contrast Ratio (CR) = White / Black Note

Note (3) Definition of Response Time ( $T_R$ ,  $T_F$ )

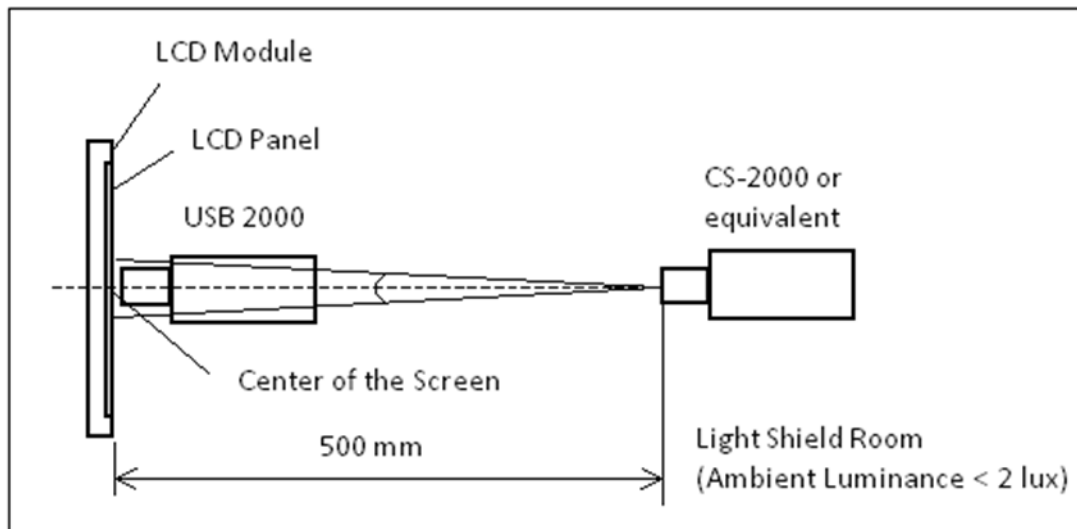


Note (4) Definition of Luminance of White ( $L_c$ ):

Measure the luminance of White at center point.

**Note (5) Measurement Setup:**

The LCD module should be stabilized at given temperature to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room. The measurement placement of module should be in accordance with module drawing.

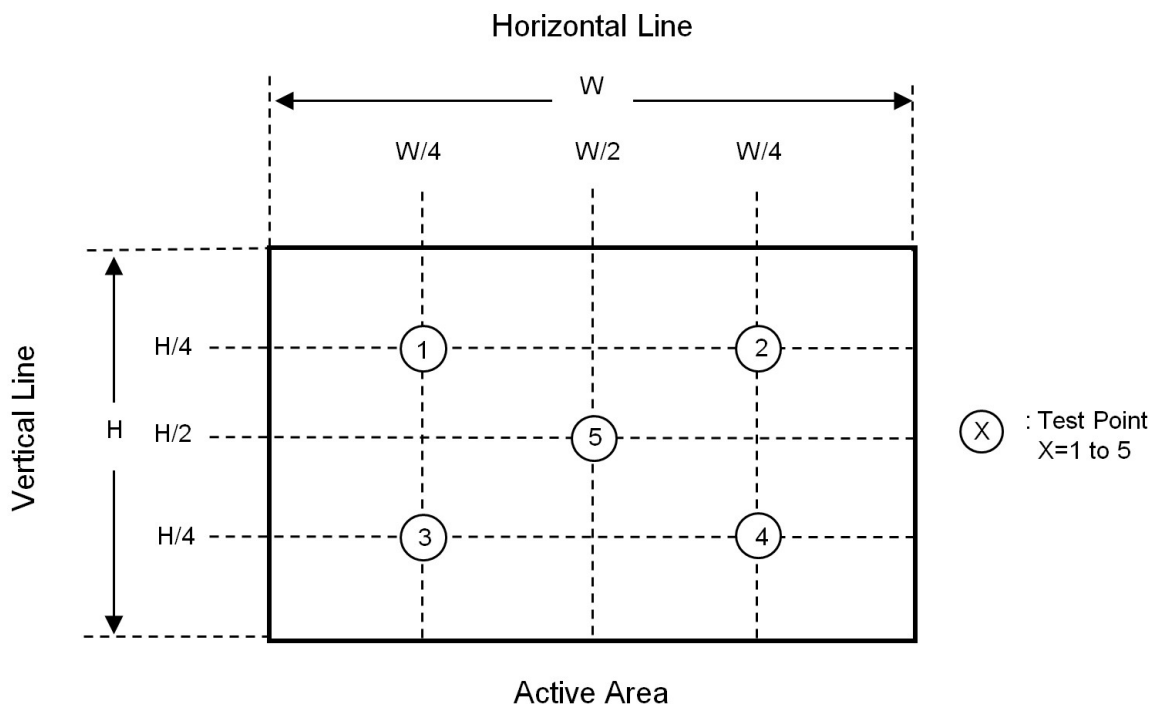


**Note (6) Definition of White Variation ( $\delta W$ ):**

Measure the luminance of White at 5 points.

Luminance of White :  $L(X)$  , where X is from 1 to 5.

$$\delta W = \frac{\text{Minimum } [L(1) \text{ to } L(5)]}{\text{Maximum } [L(1) \text{ to } L(5)]} \times 100\%$$



## 8. RELIABILITY TEST CRITERIA

Test Item	Test Condition	Note
High Temperature Storage Test	70°C, 240 hours	(1),(2) (4),(5)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour $\longleftrightarrow$ 70°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	70°C, 240 hours	
Low Temperature Operation Test	-20°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80%RH, 240hours	
ESD Test (Operation)	150pF, 330 $\Omega$ , 1 sec/cycle Condition 1 : panel contact, $\pm 8$ KV Condition 2 : panel non-contact $\pm 15$ KV	(1),(4)
Shock (Non-Operating)	50G, 11ms, half sine wave, 1 time for $\pm X$ , $\pm Y$ , $\pm Z$ direction	(2),(3)
Vibration (Non-Operating)	1.5G, 10 ~ 300 Hz sine wave, 10 min/cycle, 3 cycles each X, Y, Z direction	

Note (1) There should be no condensation on the surface of panel during test ,

Note (2) Temperature of panel display surface area should be 70°C Max.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (4) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

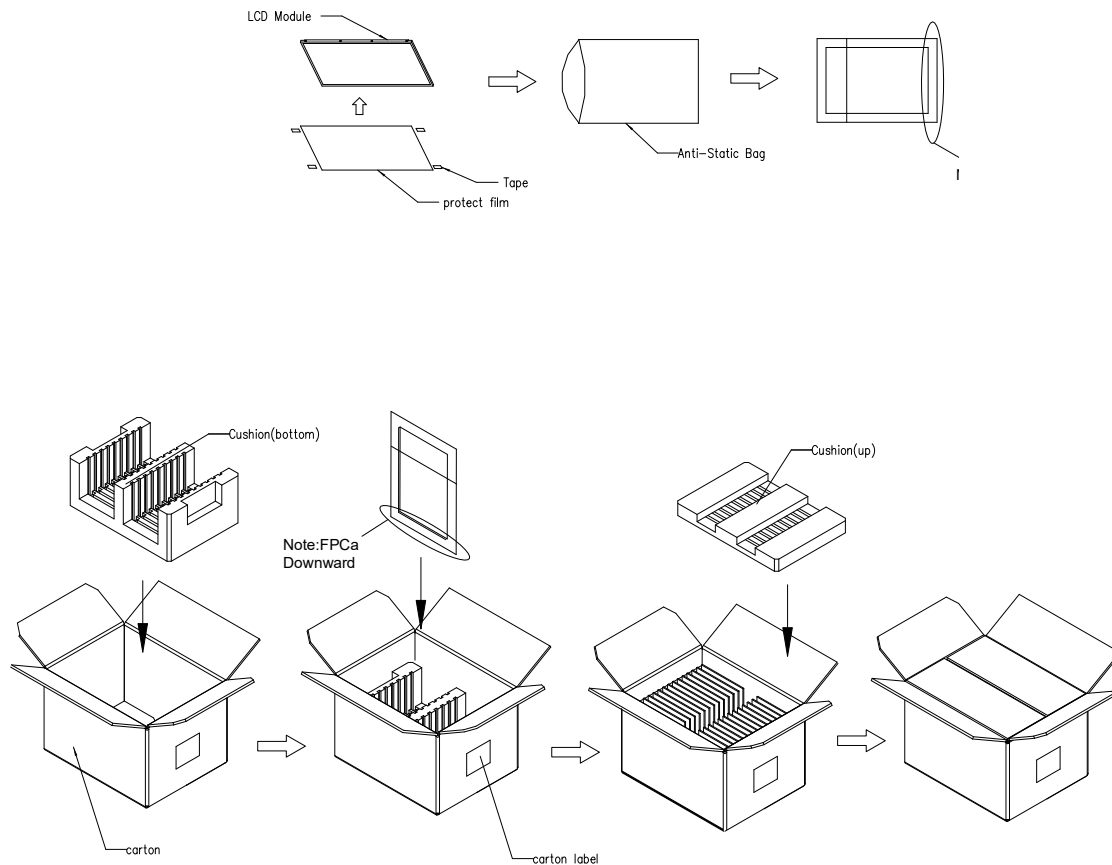
Note (5) Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

## 9. PACKAGING

### 9.1 PACKING SPECIFICATIONS

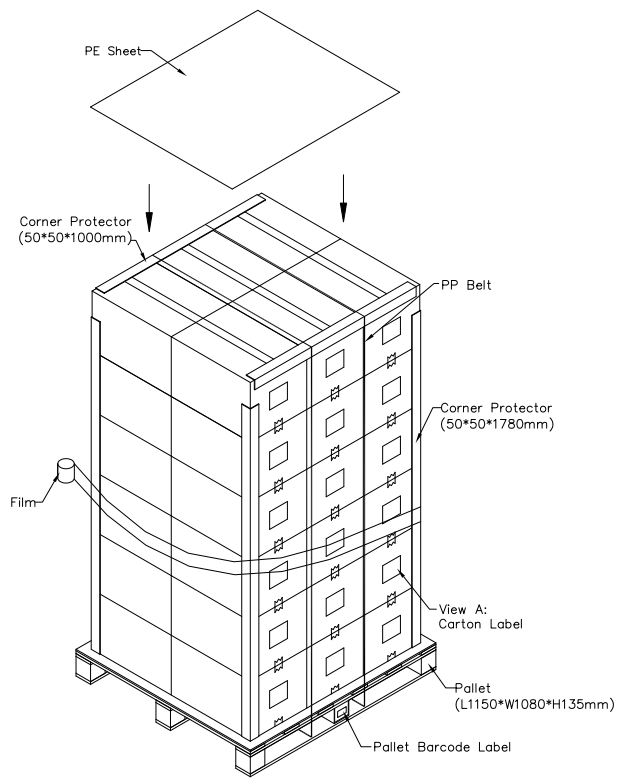
- (1) 26pcs LCD modules / 1 Box
- (2) Box dimensions: 490 (L) X 350 (W) X 320 (H) mm
- (3) Weight: approximately 11.3 Kg (26 modules per box)

### 9.2 PACKING METHOD

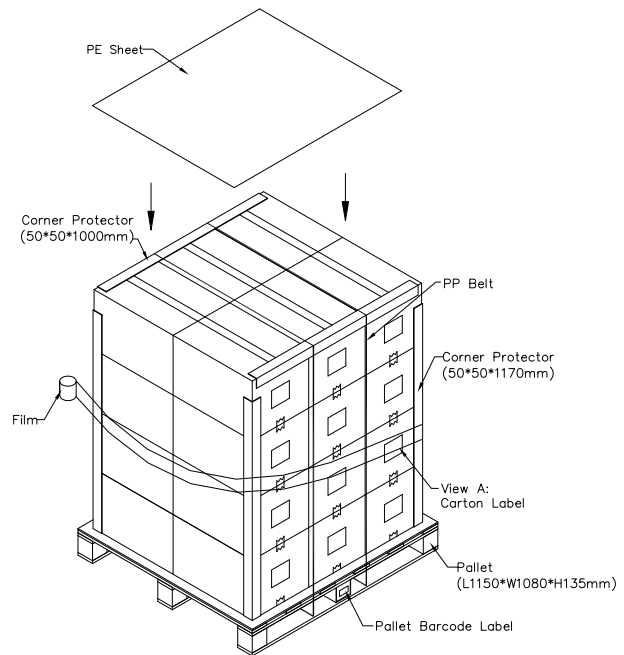


**Figure.9-1 packing method**

## Sea & Land Transportation

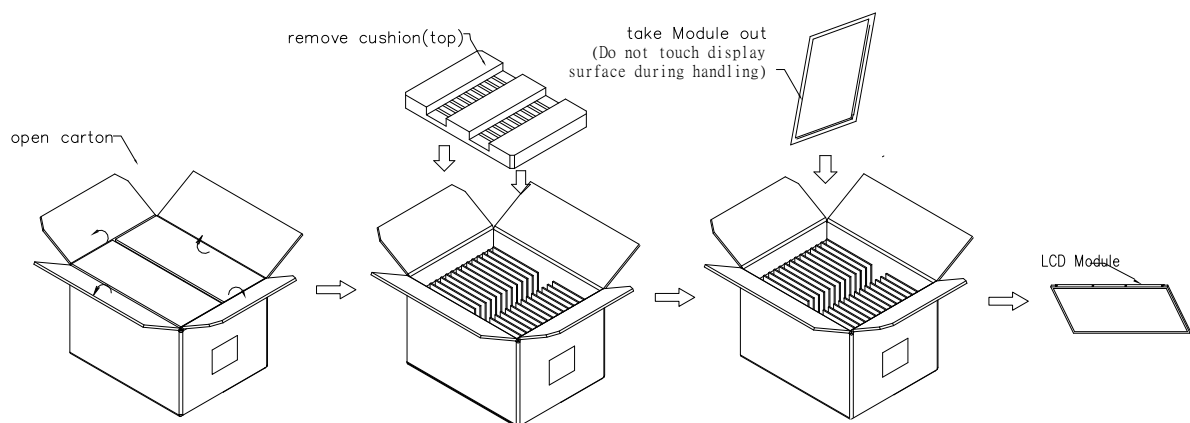


## Air Transportation



**Figure. 9-2 Packing method**

## 9.3 UN-PACKING METHOD

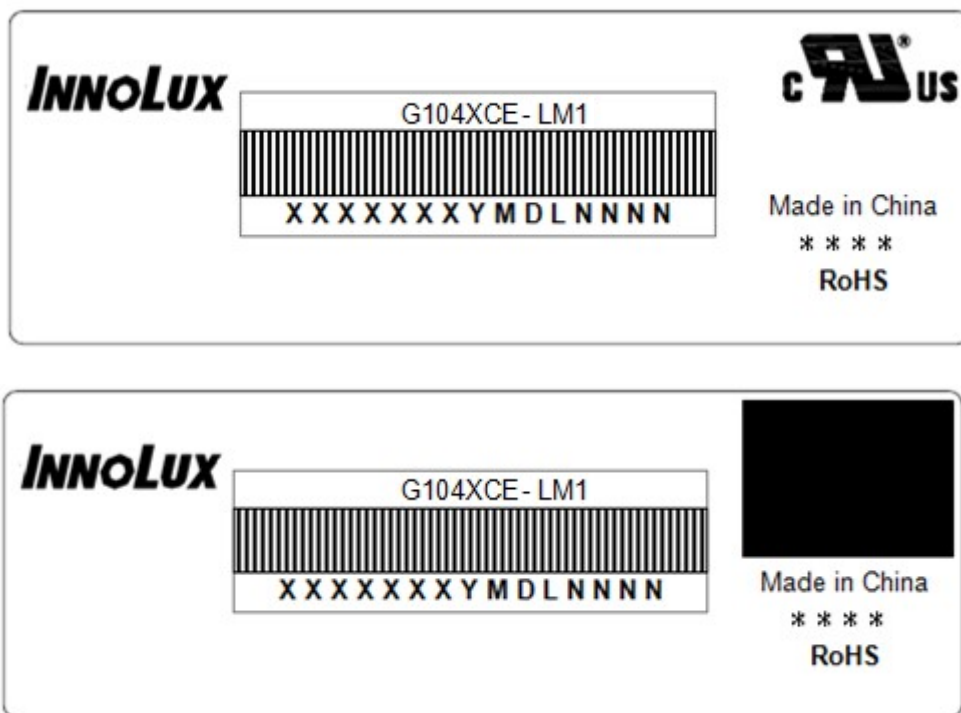


**Figure. 9-3 UN-Packing method**

## 10. DEFINITION OF LABELS

### 10.1 INNOLUX MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

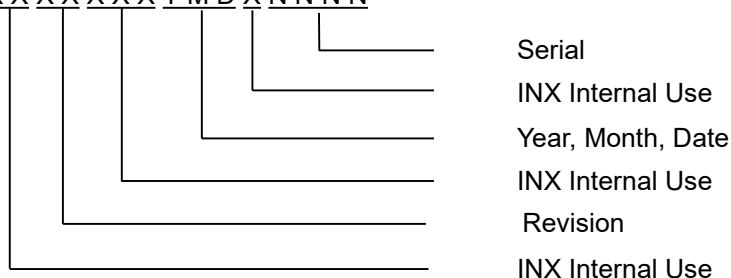


Note (1) Safety Compliance(UL logo) will open after C1 version.

(a) Model Name: G104XCE-LM1

(b) \* \* \* \* : Factory ID

(c) Serial ID: X X X X X X Y M D X N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2021~2029

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1<sup>st</sup> to 31<sup>st</sup>, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product



## 11. PRECAUTIONS

### 11.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

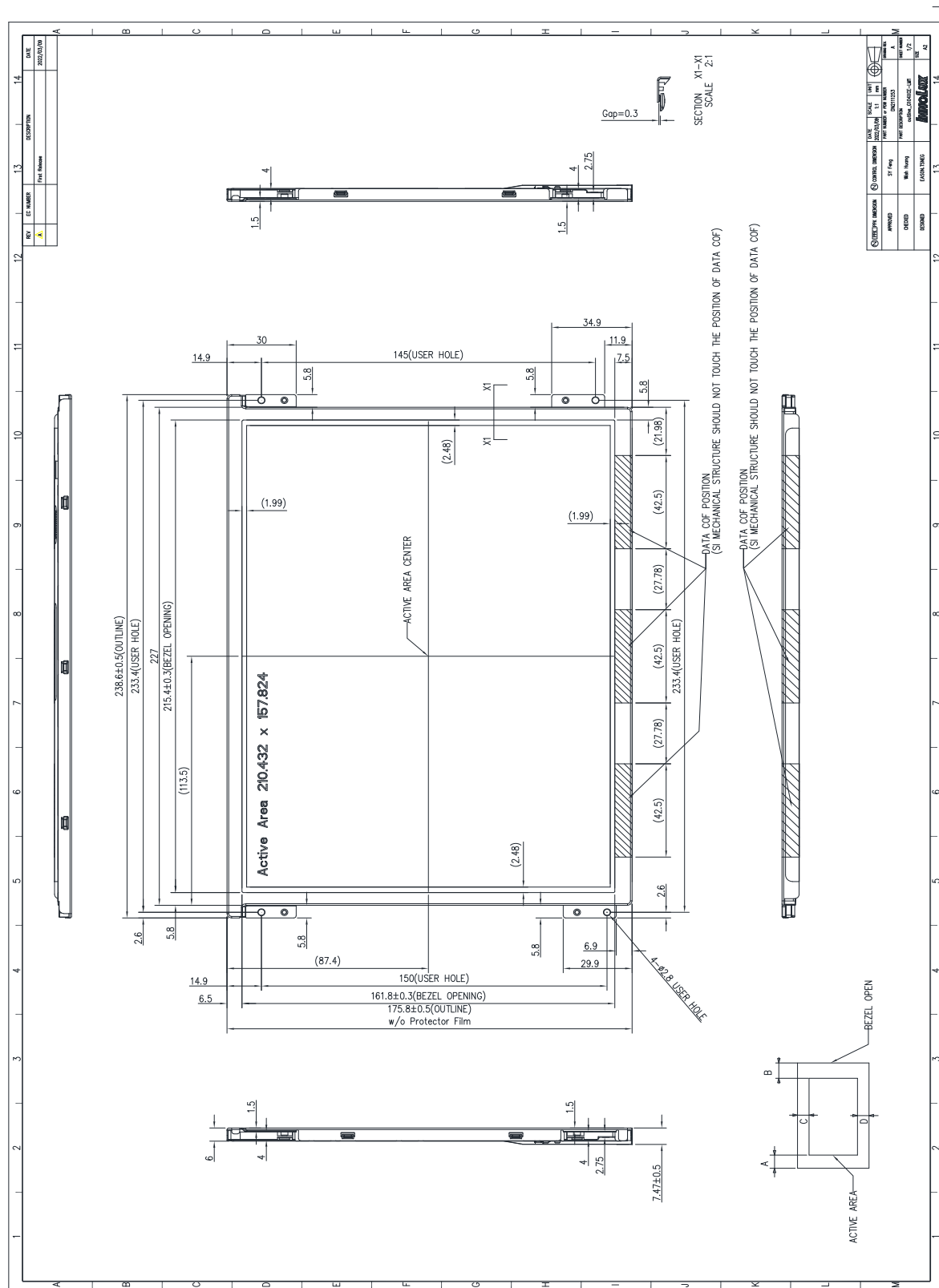
### 11.2 STORAGE PRECAUTIONS

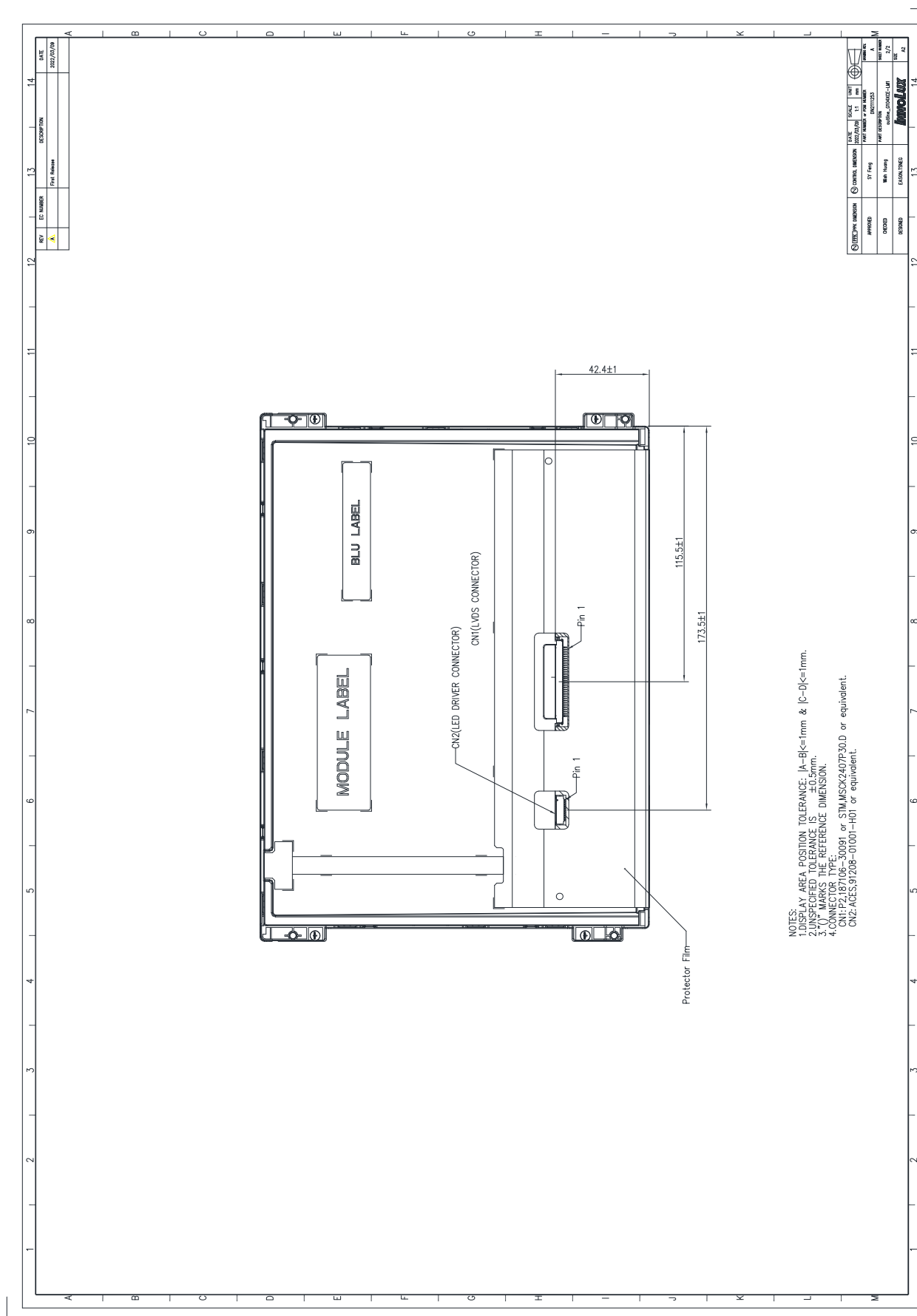
- (1) When storing for a long time, the following precautions are necessary.
  - (a) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 30°C at humidity 50+-10%RH.
  - (b) The polarizer surface should not come in contact with any other object.
  - (c) It is recommended that they be stored in the container in which they were shipped.
  - (d) Storage condition is guaranteed under packing conditions.
  - (e) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition
- (2) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (3) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (4) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

## 11.3 OTHER PRECAUTIONS

- (1) Normal operating condition
  - (a) Display pattern: dynamic pattern (Real display)
    - (Note) Long-term static display can cause image sticking.
- (2) Operating usages to protect against image sticking due to long-term static display
  - (a) Suitable operating time: under 16 hours a day.
  - (b) Static information display recommended to use with moving image.
  - (c) Cycling display between 5 minutes' information(static) display and 10 seconds' moving image.
- (3) Abnormal condition just means conditions except normal condition.


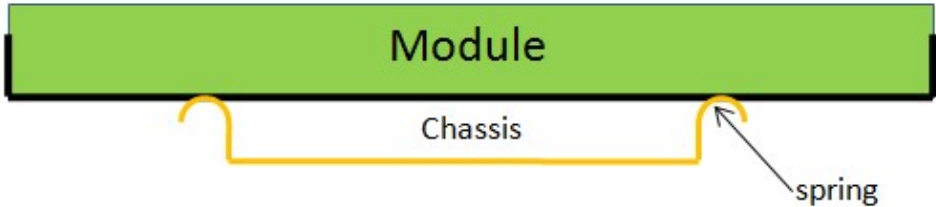

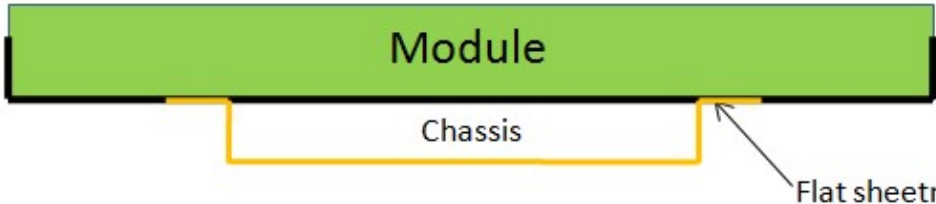

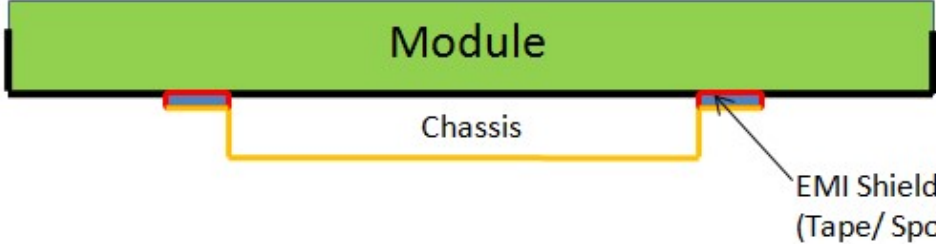
## 12. MECHANICAL CHARACTERISTIC

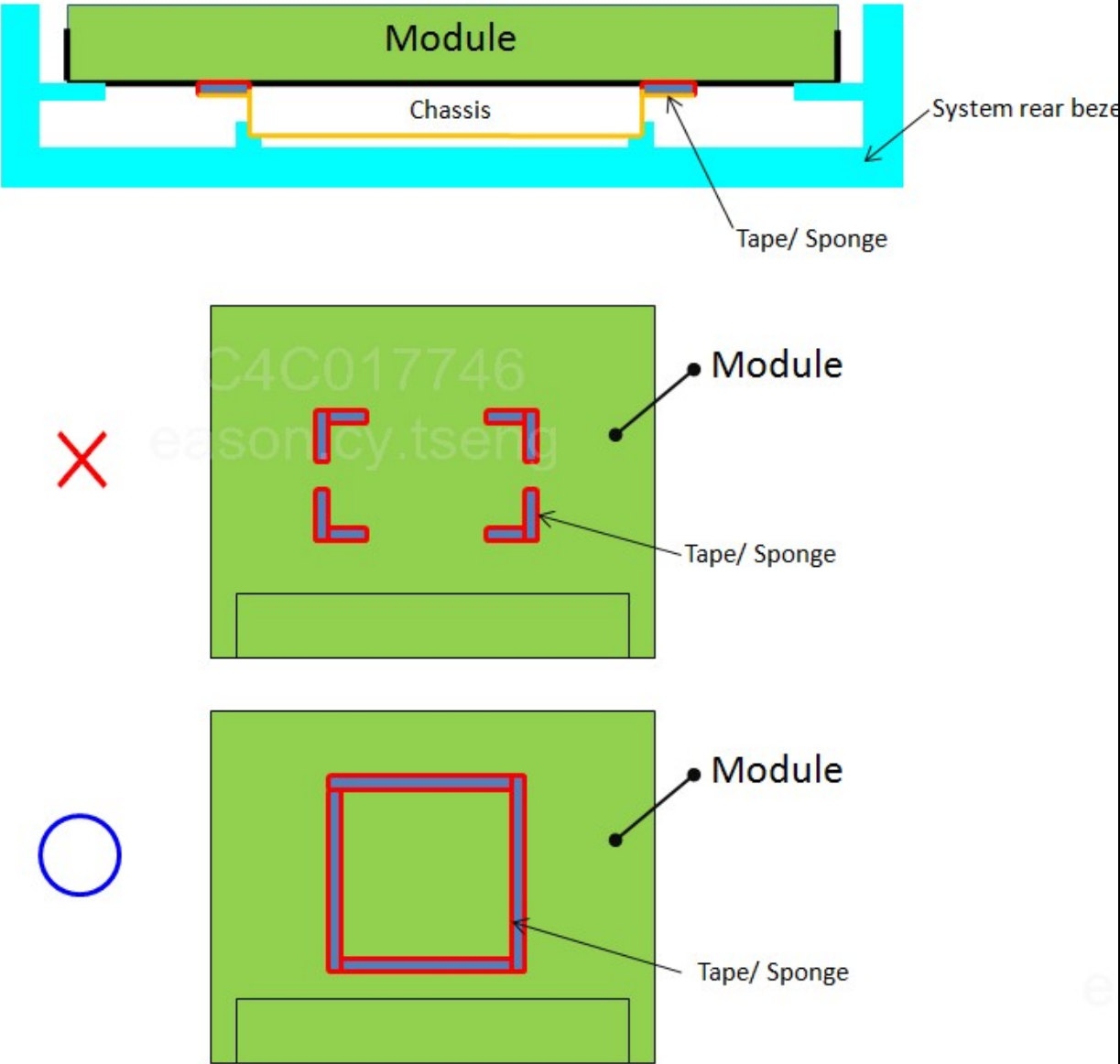


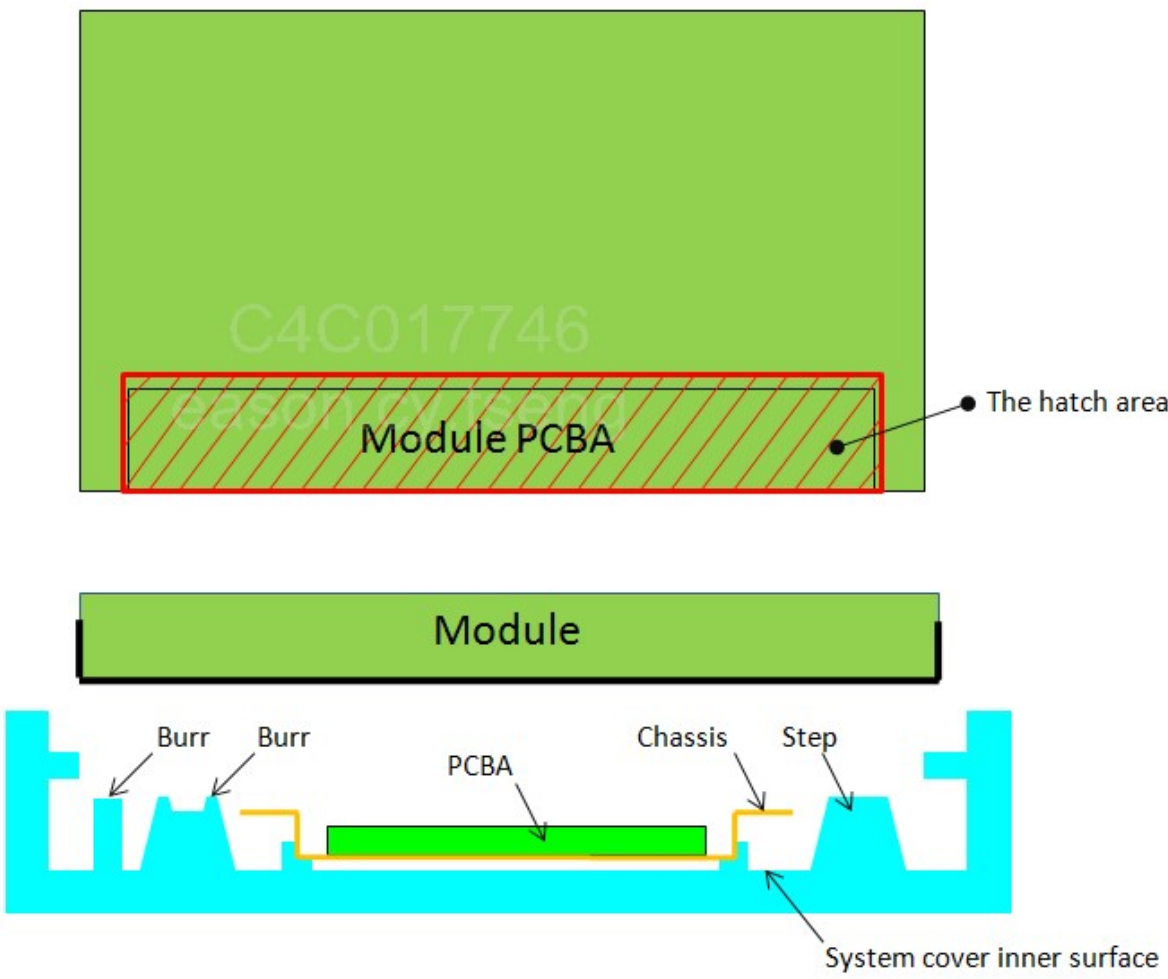


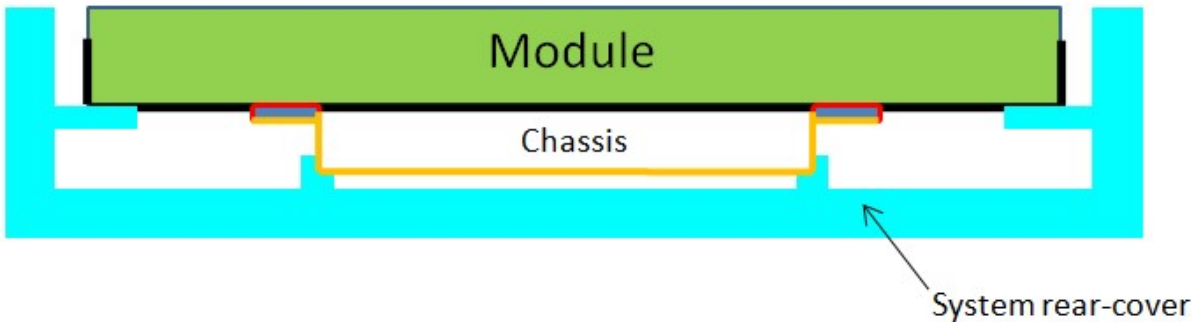
NOTES:  
1.DISPLAY AREA POSITION TOLERANCE: |A-B|≤1mm & |C-D|≤1mm.  
2.UNSPECIFIED TOLERANCE IS ±0.5mm.  
3.( ) MARKS THE REFERENCE DIMENSION.  
4.CONNECTOR TYPE: 00091 or STM/MSK2407530.0 or equivalent.  
CN2: AGES.91208-01001-H01 or equivalent.

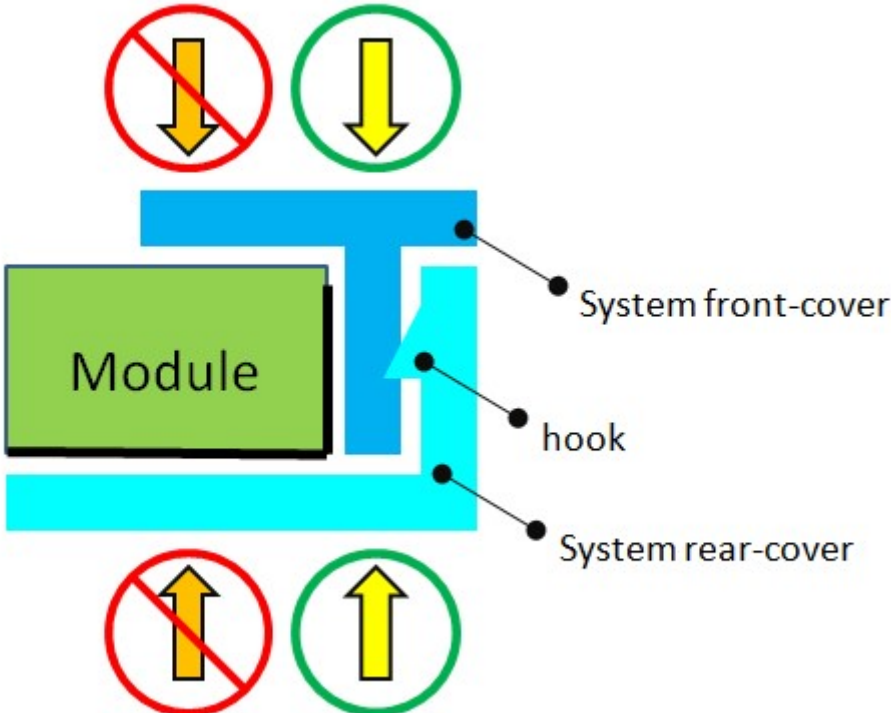
## Appendix . SYSTEM COVER DESIGN NOTICE

1	Set Chassis and IAVM Module touching Mode
	
	
	
Definition	<p>a. To prevent from abnormal display &amp; white spot after mechanical test, it is not recommended to use spring type chassis.</p> <p>b. We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, second is Flat sheet metal type chassis.</p>

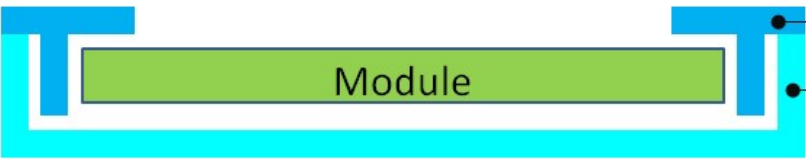
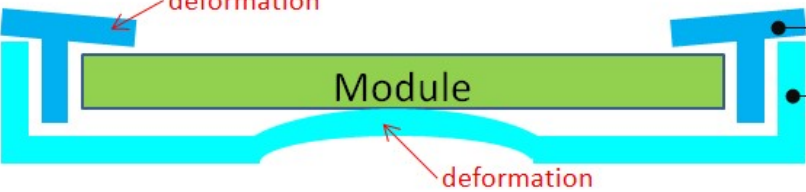
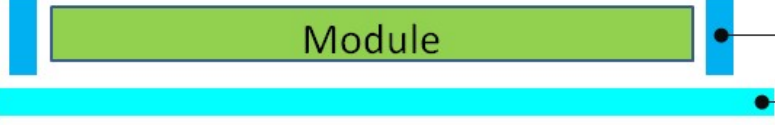
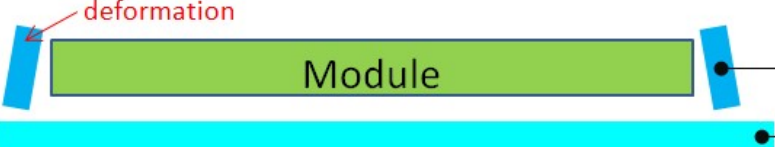
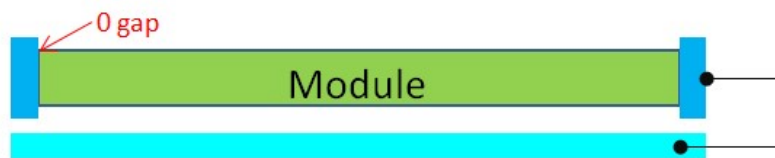
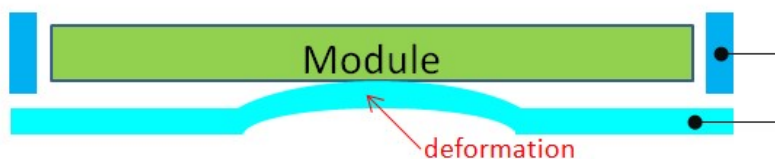
2	Tape/Sponge design on system inner surface
	
Definition	<p>a. To prevent from abnormal display &amp; white spot after mechanical test, we suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot.</p> <p>b. When using the Tape/Sponge, we suggest it be lay over between set chassis and Module rear cover. It is not recommended to add Tape/Sponge in separate location. Since each Tape/Sponge may act as pressure concentration location.</p>

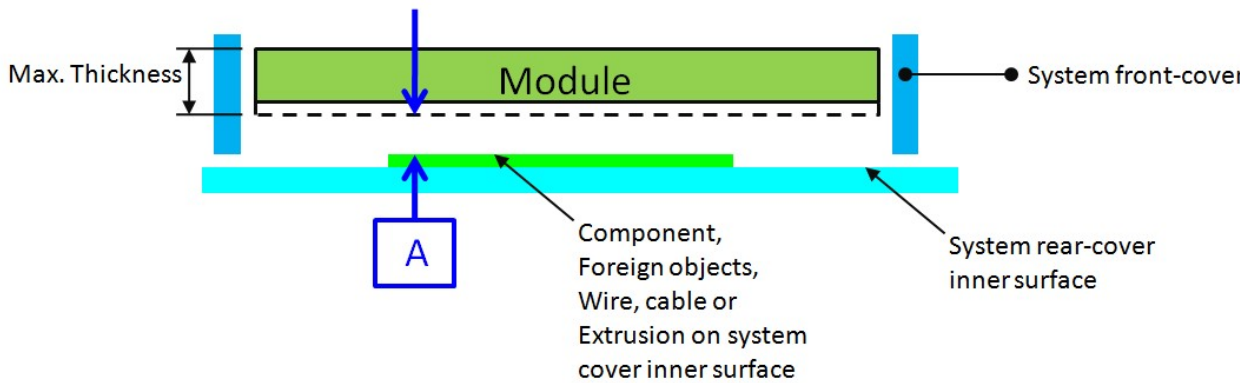
3	System inner surface examination
 <p>The diagram illustrates the system inner surface examination. The top part shows a green rectangular area representing the system cover inner surface, with a red hatched area labeled 'Module PCBA' and a label 'The hatch area' pointing to it. The bottom part shows a cross-section of the system cover inner surface, with labels for 'Burr', 'PCBA', 'Chassis', 'Step', and 'System cover inner surface'.</p>	
Definition	<p>a. The hatch area on Module PCBA should keep at least 1mm gap(X,Y,Z direction) to any structure with system cover inner surface.</p> <p>b. Burr, Step, PCB protrusion may cause stress concentration. White spot may occur during reliability test.</p>

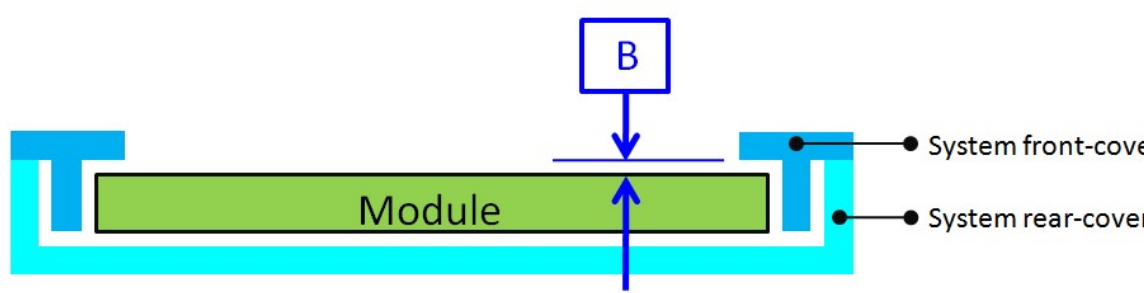
4	<b>Material used for system rear-cover</b>
	
Definition	<p>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss position for module's bracket are deformed open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</p>

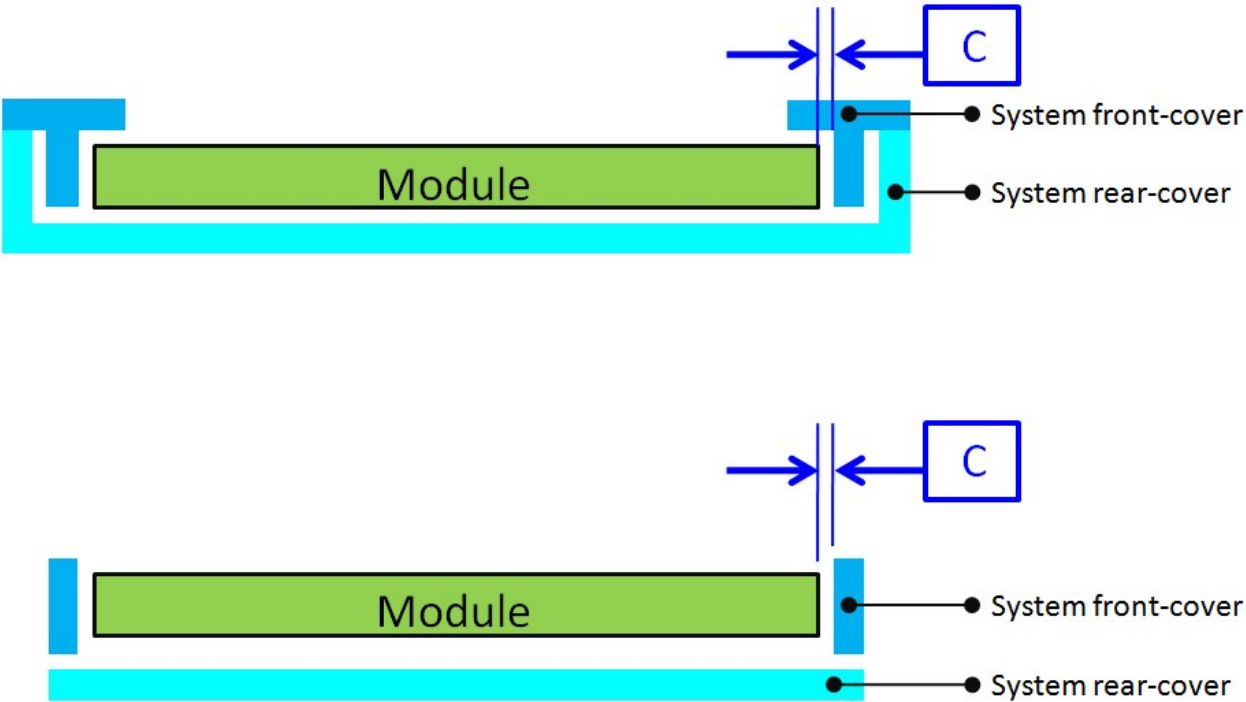
5	<b>Assembly SOP examination for system front-cover with hook structure</b>
	
Definition	<p>To prevent panel crack during system front-cover assembly process with hook structure, it is not recommended to press panel or any location that relate directly to the panel.</p>

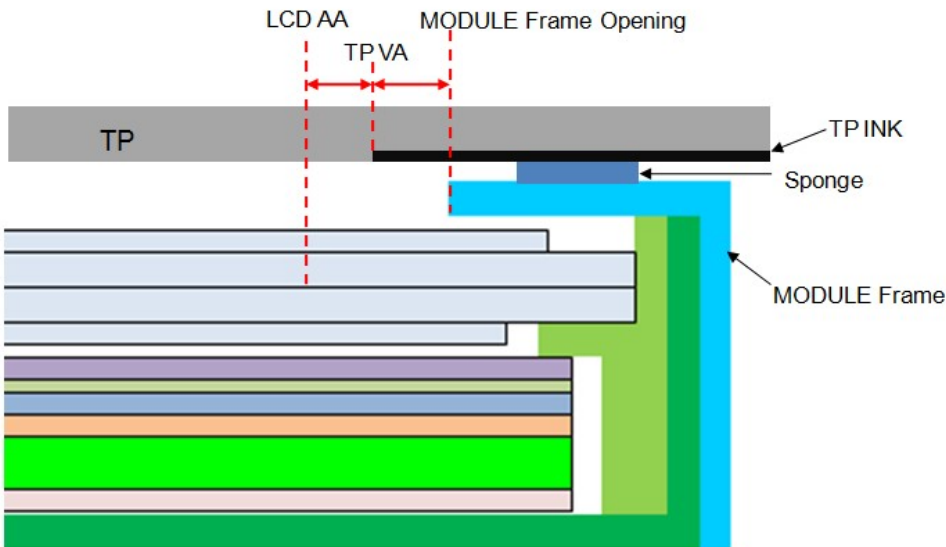


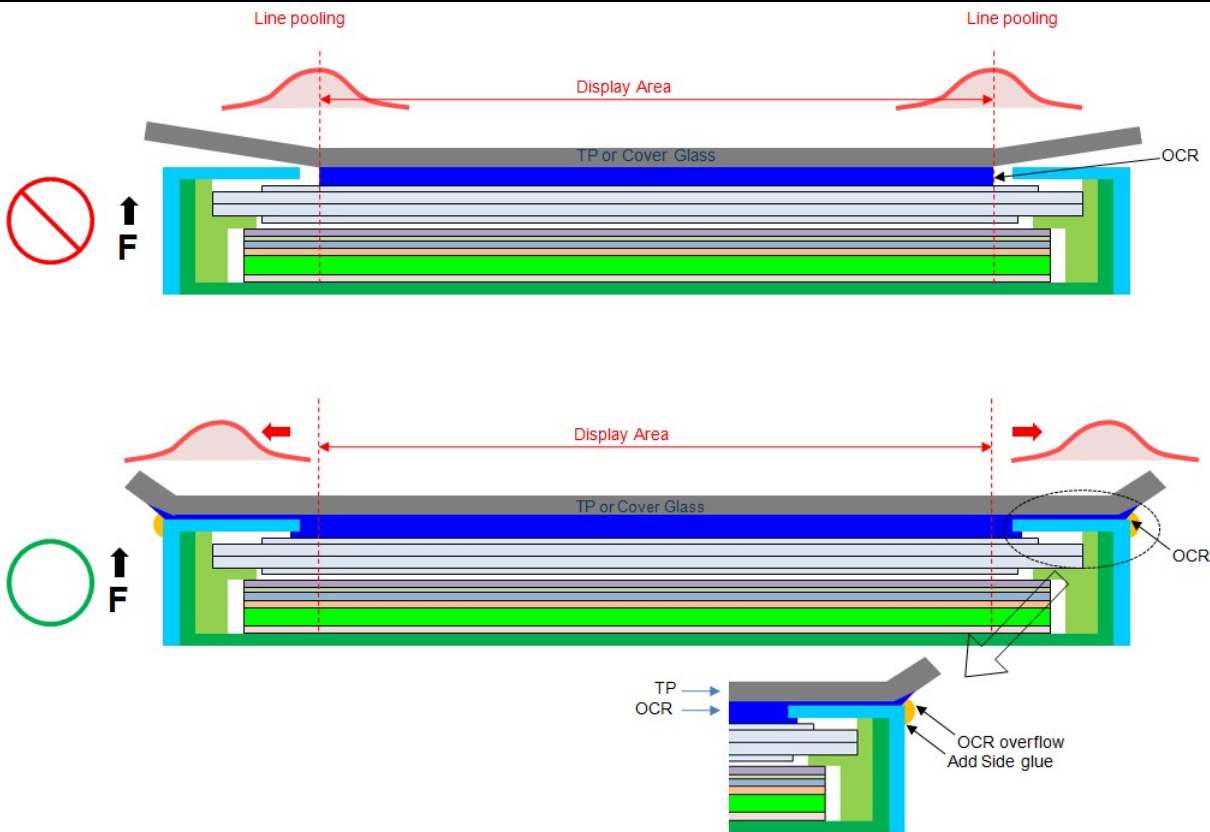
6	Permanent deformation of system cover after reliability test
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Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

7	Design gap A between panel & any components on system rear-cover
	
Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

8	Design gap B between system front-cover & panel surface
	
Definition	<p>Gap between system front-cover &amp; panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure.</p> <p>To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

9	Design gap C between panel & system front-cover or protrusions
 <p>The diagrams illustrate the required gap 'C' between the module and the system front-cover. In the top diagram, the module is positioned between the front-cover and the rear-cover, with a clear gap 'C' shown. In the bottom diagram, the module is closer to the front-cover, but a gap 'C' is still indicated, suggesting a minimum required distance.</p>	
Definition	<p>Gap between panel &amp; system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.</p> <p>The gap should be large enough to absorb the maximum displacement during the test.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

10	<b>Design distance between TP AA to LCD AA</b>
	
Definition	TP VA should avoid TP ink area covering LCD AA or causing the module frame to be exposed.

11	<b>Use OCR Lamination</b>
	
Definition	<ol style="list-style-type: none"> <li>1.OCR glue as possible beyond module, in order to avoid Line Pooling</li> <li>2.Add side glue to avoid Line Pooling</li> </ol>

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