



SPECIFICATION



HSD050JDW2-B00

5" - WVGA - LVDS

Version:

Date: 25.04.2023

Note: This specification is subject to change without prior notice

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TO : DATA MODUL

Date : Apr.25.2023

HannStar Product Information **(Formal)**

5" Color TFT-LCD Module

Model: **HSD050JDW2-B00**

Note:

- (1) Please contact HannStar Display Corp. before designing your product based on this module specification.
- (2) The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by HannStar for any intellectual property claims or other problems that may result from application based on the module described herein.
- (3) The mark “ ** ” of Model means sub-model code.

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Record of Revisions

Rev.	Date	Sub-Model	Description of change
1.0	Apr.25.2023	-B00	Formal Product Information was first released.

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1.0 GENERAL DESCRIPTION

1.1 Introduction

HannStar Display model HSD050JDW2-B00 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit with a back light system. This TFT LCD has a 5" (15:9) inch diagonally measured active display area with WSVGA (800 horizontal by 480 vertical pixel) resolution. HSD050JDW2-B00 is LCD module from HannStar.

1.2 Features

- 5" (15:9) inch configuration
- 16.7M color by 8 bit, LVDS interface
- ROHS / Halogen Free Compliance

1.3 Applications

- Automotive cluster

1.4 General information

Item	Specification	Unit	
Module Outline Dimension	120.6 (H) x 80 (V) x7.2 mm		
Display area	108(H) x 64.8(V)	mm	
Number of Pixel	800 RGB (H) x 480(V)	pixels	
Pixel pitch	0.135 (H) x 0.135 (V)	mm	
Pixel arrangement	RGB stripes ; square pixels		
Display mode	Normally Black, IPS pro		
NTSC	Typ. 70% by 1931	%	
Surface treatment	AG on Pol.		
Weight	95g typ	g	
Back-light	LED		
Power Consumption	Logic System (White Pattern)	0.5W (Max)	W
	B/L System	4.9W (Max)	W
Touch type	N/A		
Touch IC Model	N/A		
Touch Interface	N/A		
Finger	N/A		
X/Y Channel	N/A		

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1.5 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal (H)	119.1	120.6	122.1	mm
	Vertical (V)		80	80	mm
	Depth (D)		7.2		mm
Weight		—	95	105	g

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating

2.1.1 TFT LCD Module

Parameters	Symbol	Min.	Max.	Unit	Note
Power Supply voltage	VDD	0.3	4.0	V	

2.1 Environment Absolute Rating

2.2.1 Total Solution (LCD Module)

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T _{opa}	-40	85	°C	
Storage Temperature	T _{stg}	-40	90	°C	
De-rating Temperature (ambient)	T _{drat}		75	°C	

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3.0 OPTICAL CHARACTERISTICS

3.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast @ 25C (valid at perpendicular angle)	CR	$\theta=0$	800	—	—		(1)(2)
Response time	Rising	Normal viewing angle	Tr+Tf <22ms			msec	(1)(3)
	Falling						
Color gamut	S (%)		65	70	—	%	
White luminance (valid at perpendicular angle)	YL		1500	—	—	cd/m ²	(1)
Color chromaticity (CIE1931)	White	Wx	0.265	0.295	0.325		(1)(4)
		Wy	0.266	0.296	0.326		
	Red	Rx	0.610	0.640	0.670		
		Ry	0.305	0.335	0.365		
	Green	Gx	0.296	0.326	0.356		
		Gy	0.596	0.626	0.656		
	Blue	Bx	0.132	0.152	0.182		
		By	0.020	0.050	0.080		
Viewing angle	Hor.	θ_L	80°	—	—		(1)
		θ_R	80°	—	—		
	Ver.	θ_U	80°	—	—		
		θ_D	80°	—	—		
Brightness uniformity (9 point)	White	$\theta=0$	70%	—	—	—	
	Black		50%				(5)
Optima View Direction	Free						

3.2 Measuring Condition

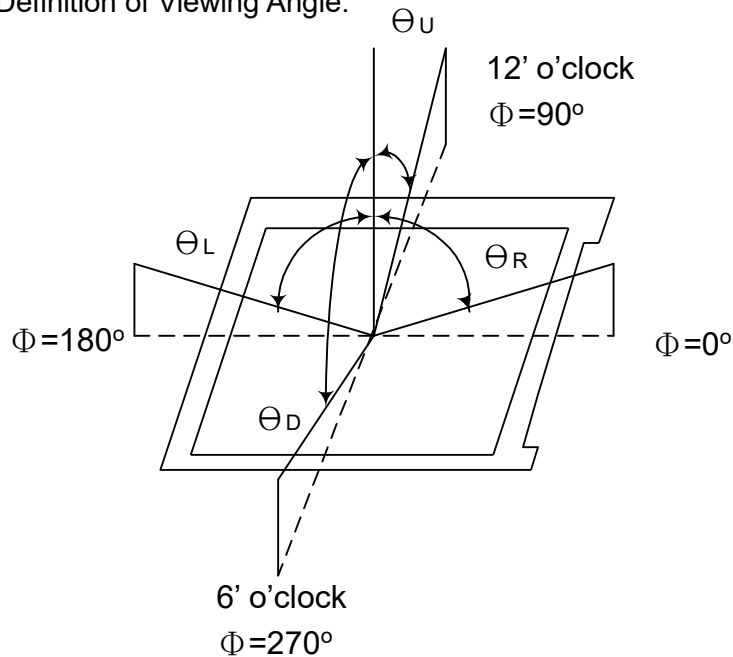
- Measuring surrounding : dark room
- LED current I_L : 80mA
- Ambient temperature : 25±2°C
- 15min. warm-up time.

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3.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.
- Measuring spot size : 20 ~ 21 mm

Note (1) Definition of Viewing Angle:

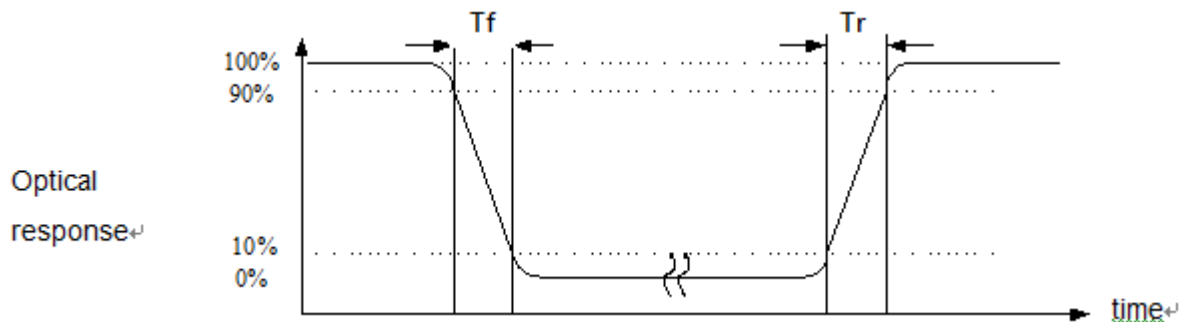


Note (2) Definition of Contrast Ratio (CR) :

Measured at the center point of panel
 Luminance with all pixels white

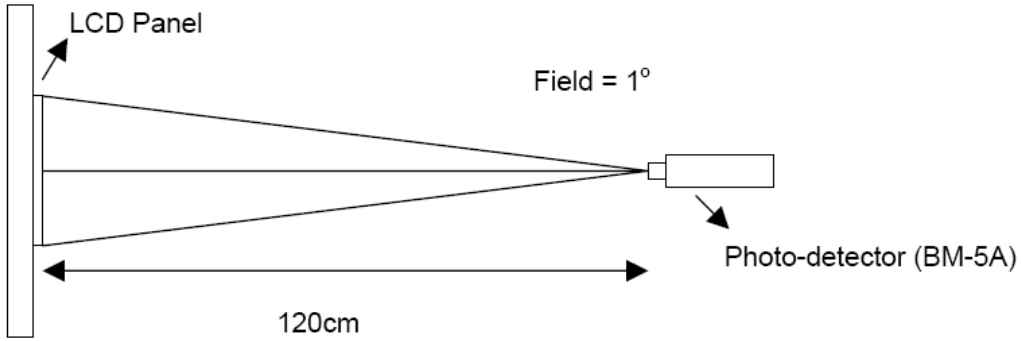
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F

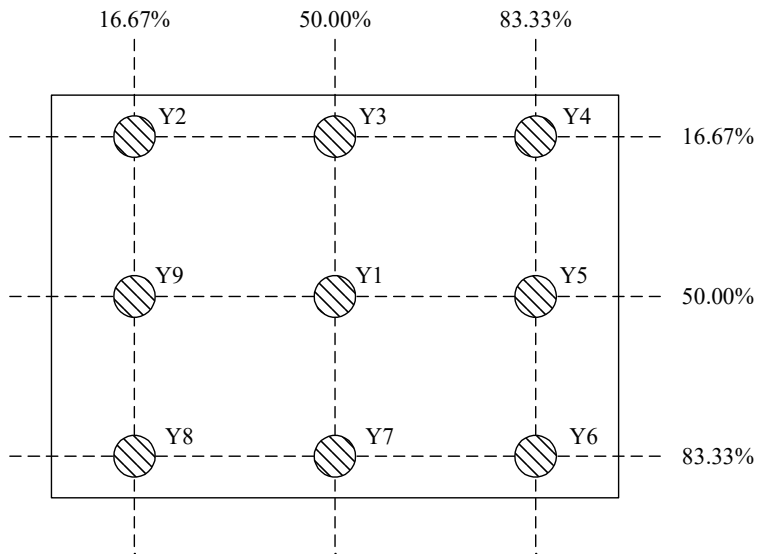


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Note (4) Definition of optical measurement setup



Note (5) Definition of brightness uniformity

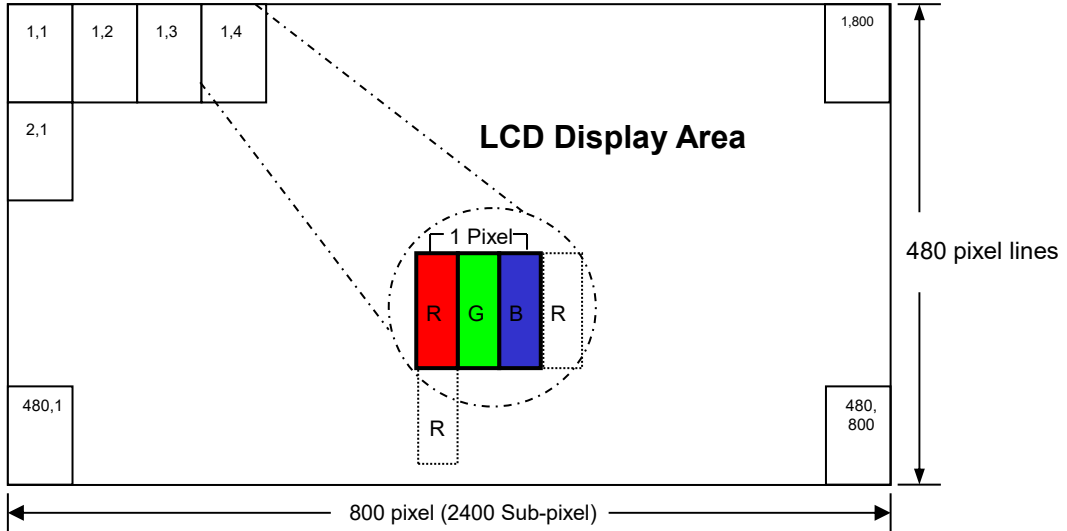


$$\text{Luminance uniformity} = \frac{(\text{Min Luminance of 9 points})}{(\text{Max Luminance of 9 points})} \times 100\%$$

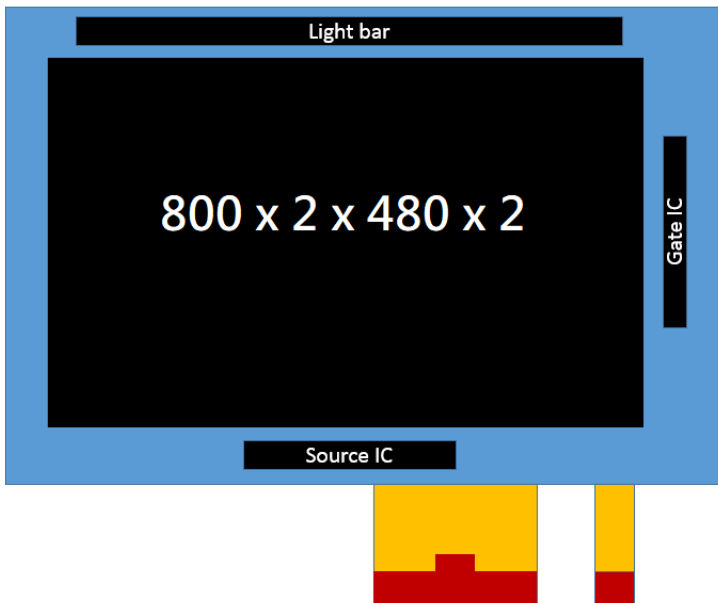
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4.0 BLOCK DIAGRAM

4.1 Pixel Format (*ps, with 2 Domain technology to improve viewing angle color shift)



4.2 TFT LCD Module (dual gate design):



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4.3 Relationship Between Displayed Color and Input

	Display	MSB				LSB				MSB				LSB				Gray scale Level								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0		B7	B6	B5	B4	B3	B2	B1	B0
Basic color	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	-
	Green	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	-
	Light Blue	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-
	Red	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-
	Purple	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	-
	Yellow	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	-
	White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-
Gray scale of Red	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark ↑	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L1
		L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L251
	↓ Light	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L252
		H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L253
	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L254	
Red	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Red L255	
Gray scale of Green	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark ↑	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L1
		L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L251
	↓ Light	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L252	
		L	L	L	L	L	L	L	L	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L253	
	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L254		
Green	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	Green L255		
Gray scale of Blue	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark ↑	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L1
		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L251
	↓ Light	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	L	L	L252
		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H	L	L253
	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L254	
Blue	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	Blue L255	
Gray scale of White & Black	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark ↑	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L1	
		L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L2	
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	L3...L251	
	↓ Light	H	H	H	H	H	H	L	L	H	H	H	H	H	L	L	H	H	H	H	H	L	L	L	L252	
		H	H	H	H	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	L	H	L	L253	
	H	H	H	H	H	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	L	L	L254		
White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	White L255		

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5.0 INTERFACE PIN CONNECTION

5.1 LCM FPC Pin Assignment:

FPC connector is used for electronics interface. The recommended model is FH41-50S-0.5SH manufactured by Hirose. FPC radius limit is 0.5mm.

Pin No.	Symbol	I/O	Function	Note
1	Connected to 2	-	Connector testing	
2	Connected to 1	-	Connector testing	
3	VCC	P	Logic Power Supply	
4	VCC	P	Logic Power Supply	
5	N.C.	-	Not Connected(Internal used for Hannstar)	VCC_OTP
6	VSS	P	Ground	
7	RESET	I	Global reset pin	Note 1
8	STBYB	I	Standby mode	Note 2
9	BISTEN	I	Enable built-in self test(BIST)function	Note 3
10	SHLR	I	Horizontal scan direction	Note 4
11	UPDN	I	Vertical scan direction	Note 4
12	VSS	P	Ground	
13	D11N	I	LVDS Signal D1-	
14	D11P	I	LVDS Signal D1+	
15	VSS	P	Ground	
16	D12N	I	LVDS Signal D2-	
17	D12P	I	LVDS Signal D2+	
18	VSS	P	Ground	
19	CK1N	I	LVDS Clock-	
20	CK1P	I	LVDS Clock+	
21	VSS	P	Ground	
22	D13N	I	LVDS Signal D3-	
23	D13P	I	LVDS Signal D3+	
24	VSS	P	Ground	
25	D14N	I	LVDS Signal D4-	
26	D14P	I	LVDS Signal D4+	
27	VSS	P	Ground	
28	N.C.	-	Not Connected	
29	N.C.	-	Not Connected	
30	VSS	P	Ground	
31	N.C.	-	Not Connected	
32	N.C.	-	Not Connected	
33	VSS	P	Ground	
34	N.C.	-	Not Connected	

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Pin No.	Symbol	I/O	Function	Note
35	N.C.	-	Not Connected	
36	VSS	P	Ground	
37	N.C.	-	Not Connected	
38	N.C.	-	Not Connected	
39	VSS	P	Ground	
40	N.C.	-	Not Connected	
41	N.C.	-	Not Connected	
42	VSS	P	Ground	
43	SCK	I	Clock signal of SPI	
44	VSS	P	Ground	
45	SCS	I	Chip select signal	
46	SDI	I	Serial data input of SPI	Note 5
47	SDO	O	Serial data output of SPI	Note 5
48	VSS	P	Ground	
49	Connected to 50	-	Connector testing	
50	Connected to 49	-	Connector testing	

I: input O: Output P: Power

Note 1 : Global reset pin: Active low to enter reset mode.

Note 2 : STBYB,active low.

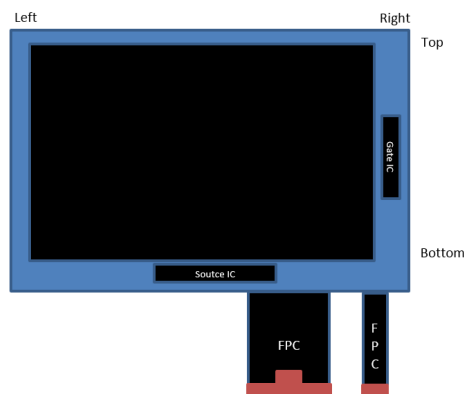
Note 3 : BISTEN,active high.

Note 4 : When SHLR="0", set right to left scan direction.

When SHLR ="1", set left to right scan direction.

When UPDN="1", set top to bottom scan direction.

When UPDN ="0", set bottom to top scan direction.



Note 5 : Support 3/4 wire SPI. Short SDI and SDO together for 3-wire SPI application.

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5.2 Light-bar FPC Pin Assignment:

Back-light module FPC connector is used on customer's PCB.

Pin No	Symbol	Description
1	A1	LED1+
2	A1	LED1+
3	A2	LED2+
4	A2	LED2+
5	THER+	Thermistor+
6	THER-	Thermistor-
7	C2	LED2-
8	C2	LED2-
9	C1	LED1-
10	C1	LED1-

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6.0 ELECTRICAL CHARACTERISTICS

6.1 TFT LCD Module

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	VDD	3.0	3.3	3.6	V	
Input signal voltage	V _{IH}	0.7 VDD	-	VDD	V	
	V _{IL}	0	-	0.3 VDD	V	
Current of power supply	IDD	-	-	150	mA	VDD = 3.3V / Note (1)

Note :

(1) : White Pattern & 60Hz ◦

(2) : The max permitted ripple of the power supply @Typ. 3.3V is +/-150mV.

6.2 Switching Characteristics for LVDS Receiver

6.2.1 LVDS DC electrical characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential Input High Threshold	V _{th}	100	—	—	mV	V _{CM} =1.2V
Differential Input Low Threshold	V _{tl}	—	—	-100	mV	
Input Current	I _{IN}	-10	—	+10	uA	
Differential input Voltage	V _{ID}	0.1	—	0.6	V	
Differential input common Mode voltage	V _{CM}	1	1.2	1.7- V _{ID} /2	V	

Single-ended:
LVCLKP(R),
LVCLKN(R),
LVD[3:0]P(R),
LVD[3:0]N(R)

Differential:
LVCLKP(R)-LVCLKN(R),
LVD[3:0]P(R)-
LVD[3:0]N(R)

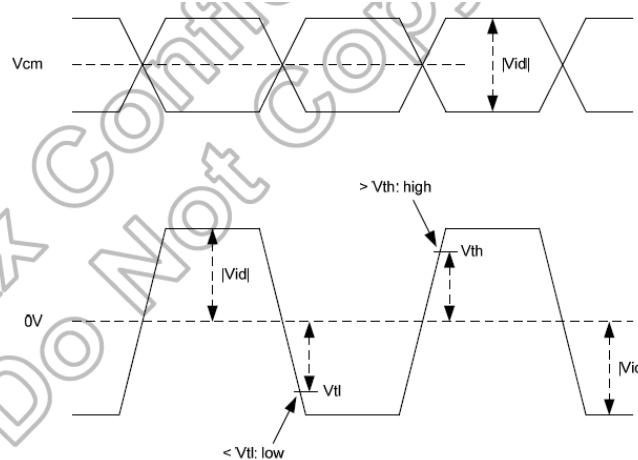
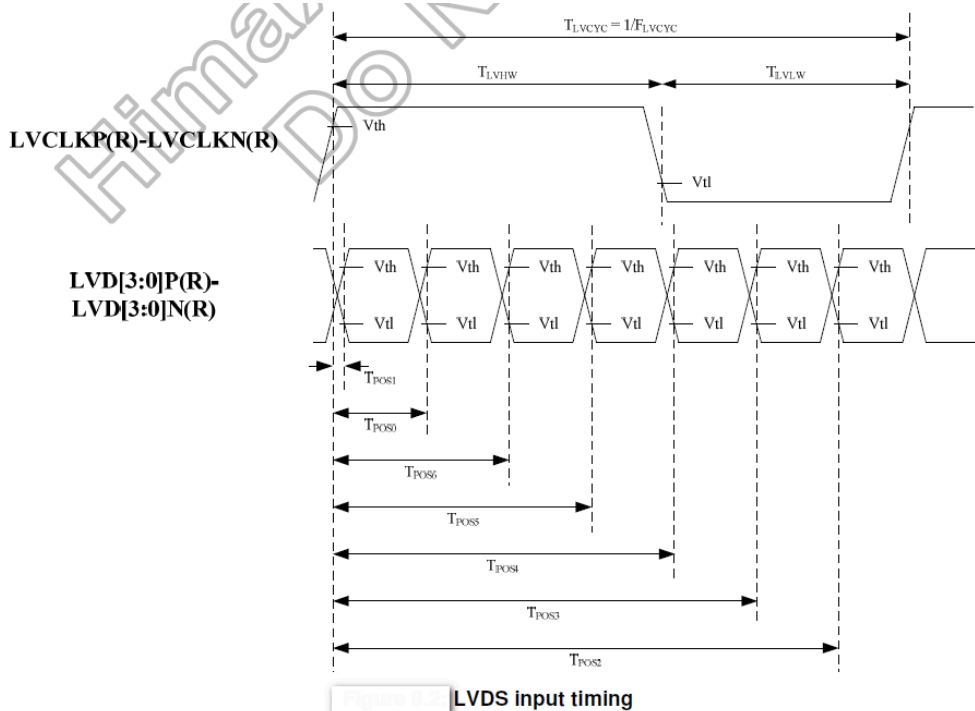


Figure 3-1 LVDS mode DC electrical characteristics

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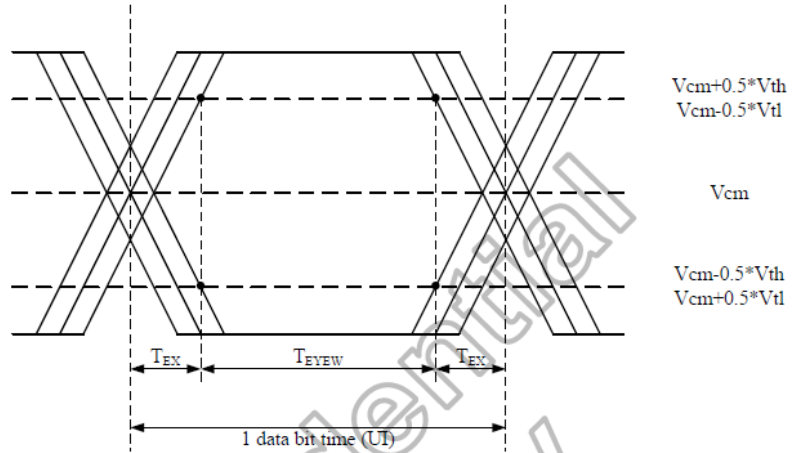
6.2.2 LVDS AC electrical characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	F_{LVCLYC}	15	-	110	MHz
Clock period	T_{LVCLYC}	9.52	-	-	Ns
1 data bit time	UI	-	1/7	-	T_{LVCLYC}
Clock high time	T_{LVCH}	-	4	-	UI
Clock low time	T_{LVCL}	-	3	-	UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6	-	-	UI
Input eye border	T_{EX}	-	-	-	UI
LVDS wake up time	T_{ENLVDS}	-	-	150	ms

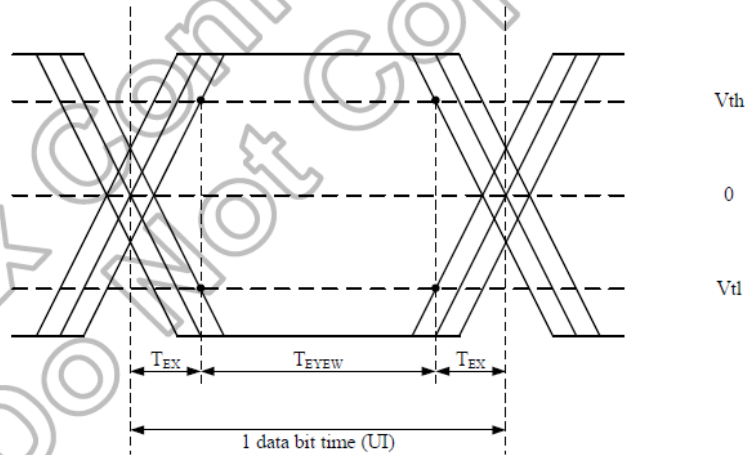


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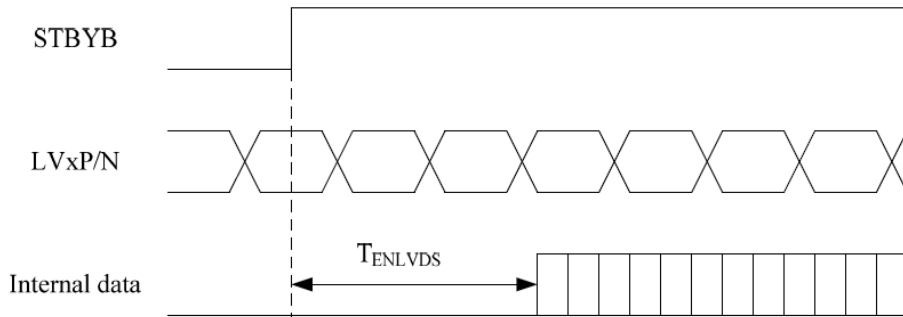
**Single-ended:
LVD[3:0]P,
LVD[3:0]N**



**Differential:
LVD[3:0]P-LVD[3:0]N**



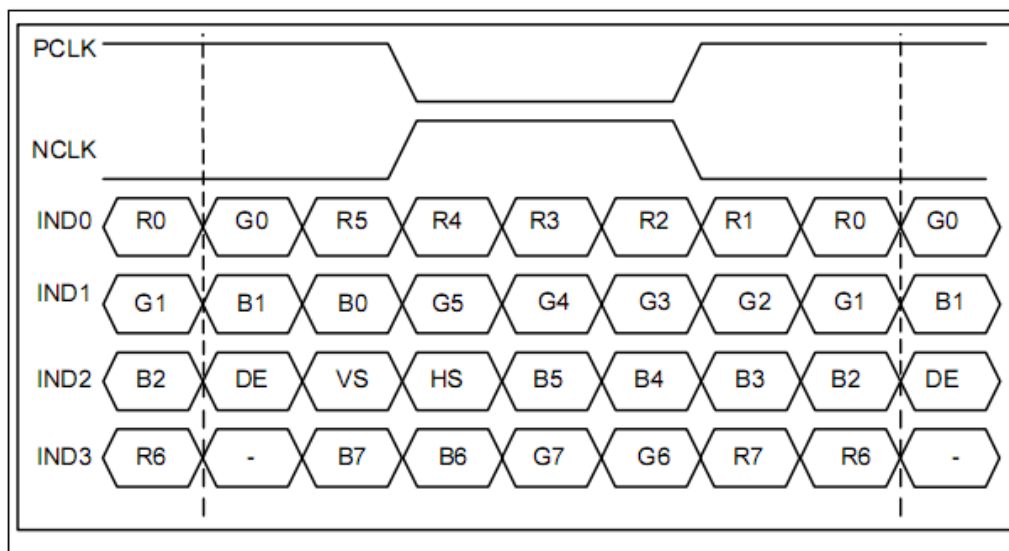
LVDS input eye diagram



LVDS wake up time

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6.3 Bit LVDS input



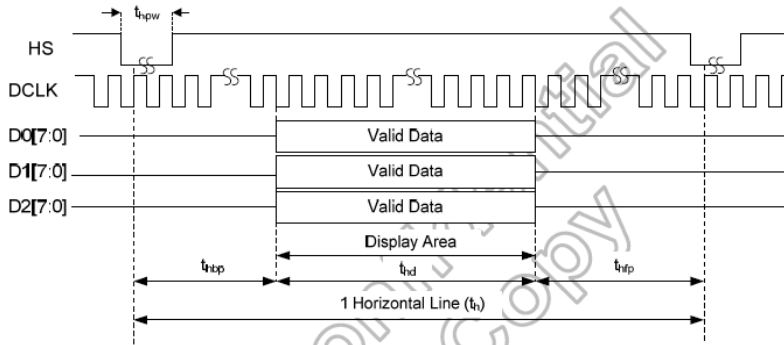
6.4 Interface Timing

6.4.1 Sync Mode(Default for DN5)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Frame Rate	--	-	60	-	Hz	
Vertical valid data	T_{vd}	480				
Vsync pulse width	T_{vpw}	1	3	254	Line	
Vsync back porch	T_{vbp}	-	24	-	Line	Note1
Vsync front porch	T_{vfp}	6	16	170	Line	
Vertical Total Time	T_v	488	520	750	Line	
Horizontal Display Time	T_{HD}	800			Clock	
Hsync pulse Width	T_{hpw}	6	12	254	Clock	
Hsync back porch	T_{hbp}	-	16	-	Clock	Note1
Hsync front porch	T_{hfp}	50	56	250	Clock	
Horizontal Total Time	T_H	855	872	1200	Clock	
Clock Rate	$1/T_{Clock}$	25.03	27.21	54	MHz	

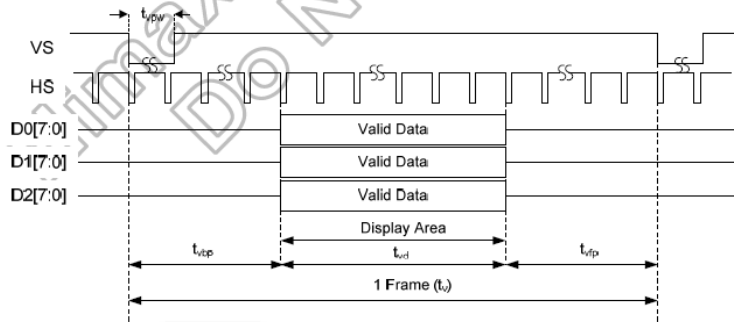
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• Horizontal



Horizontal input timing at Sync mode

• Vertical



Vertical input timing at Sync mode

Note1: Tvbp & Thbp are fixed to typical value.

6.4.2 LVDS with SSC

The LVDS receiver can support spread spectrum clock(SSC).Limitation is listed as below.

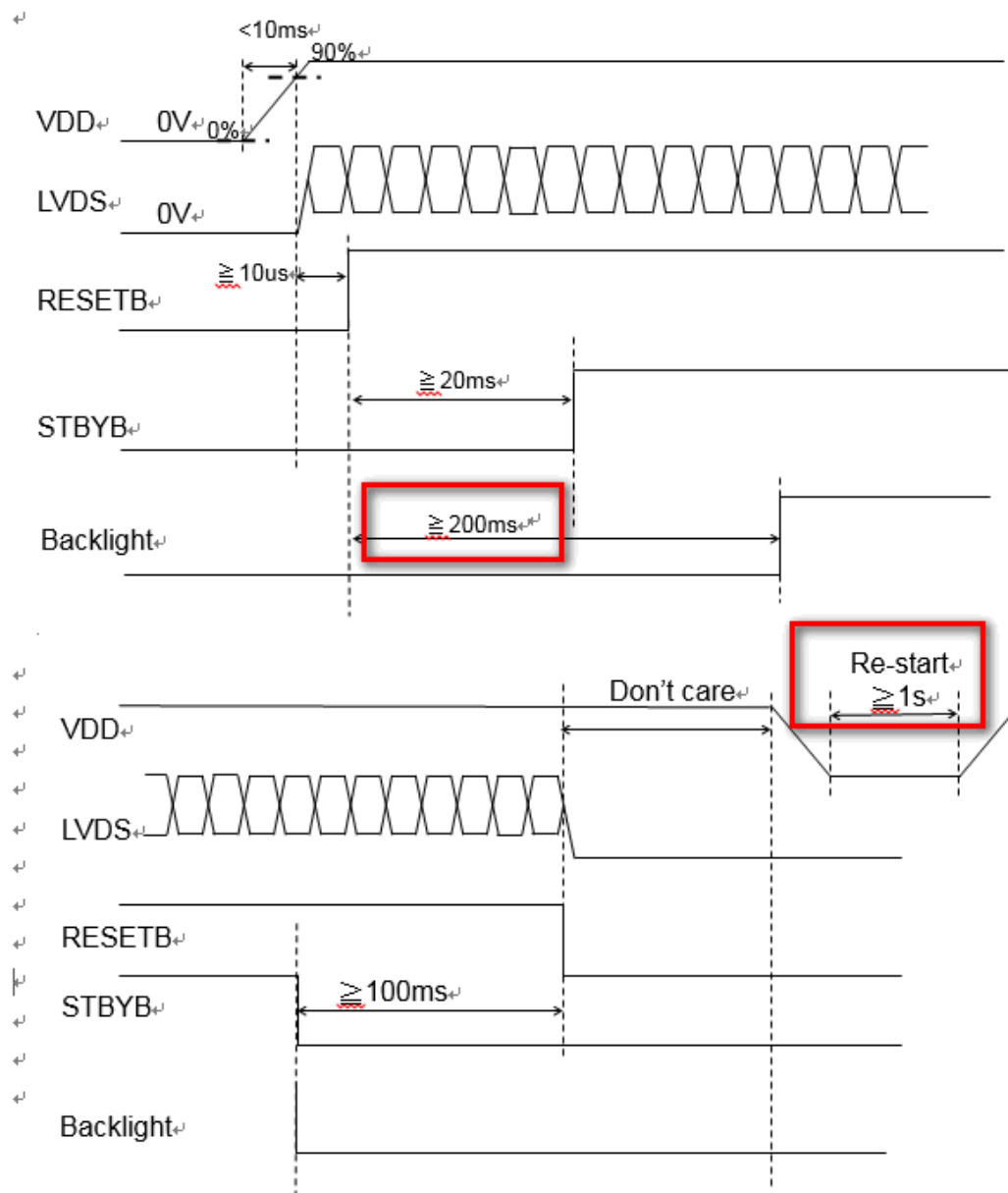
Parameter	Symbol	Condition	Spec.			Unit
			Min	Typ.	Max	
Modulation frequency	SSC _{MF}	LVDS clock frequency center at <80MHz~40MHz	$(F_{DCLK}/t_h)/1000$ (Horizontal line frequency)	-	150	KHz
		LVDS clock frequency center at <40MHz~15MHz		-	100	KHz
Modulation rate	SSC _{MR}	LVDS clock frequency + SSCMR in the range of 15MHz~110MHz	-	-	+/-3	%

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Note: F_{DCLK} is DCLK frequency, t_h is DCLK of 1 horizontal line.
 For example, F_{DCLK} is 54MHz, t_h is 1200DCLK, thus SSCMF should be larger than $(54\text{MHz}/1200)=45\text{KHz}$ (which is Horizontal line frequency)

6.5 Power On / Off Sequence

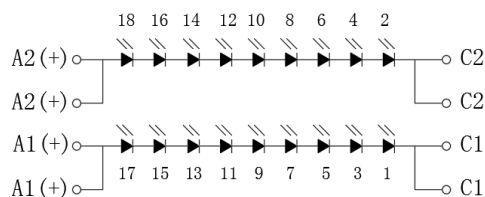
Note : LVDS signal must be activated before set STBYB signal to High.
 LVDS signal is not relevant before or after reset.



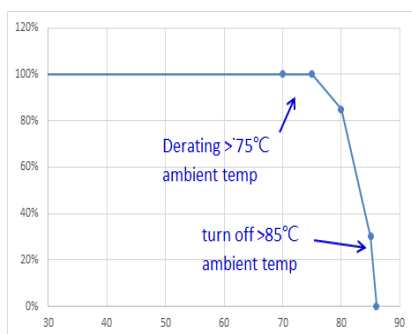
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6.6 Backlight Unit

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Current	I_F	--	--	80	mA	Ta=25°C
LED Voltage	V_F	--	--	30.6	Volt	Ta=25°C
LED Life-Time	N/A	10,000	--	--	Hour	Ta=25°C, 50% luminance



6.7 Backlight De-rating curve



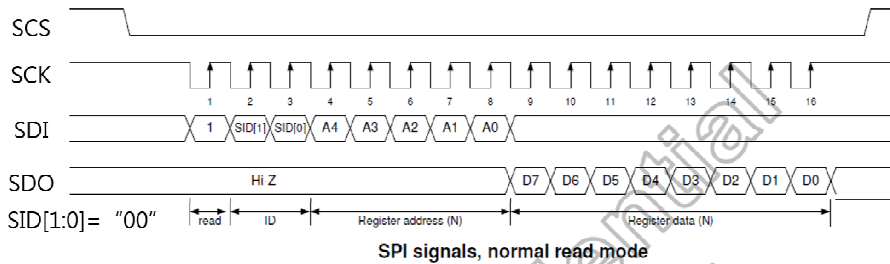
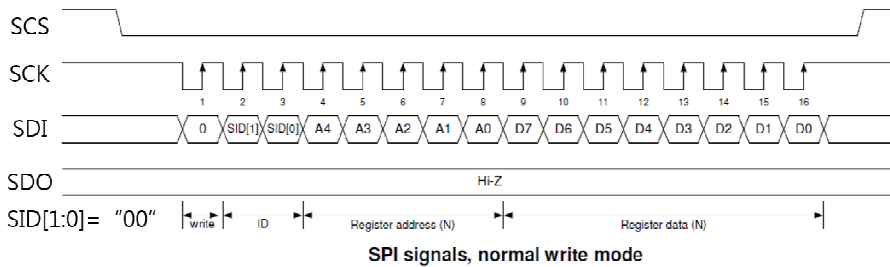
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6.8 BIST(Build-in self-test) Pattern

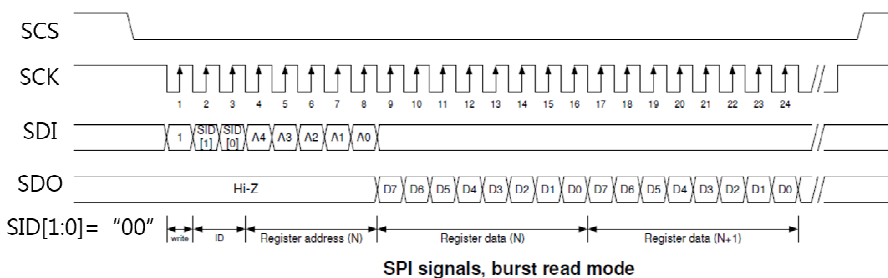
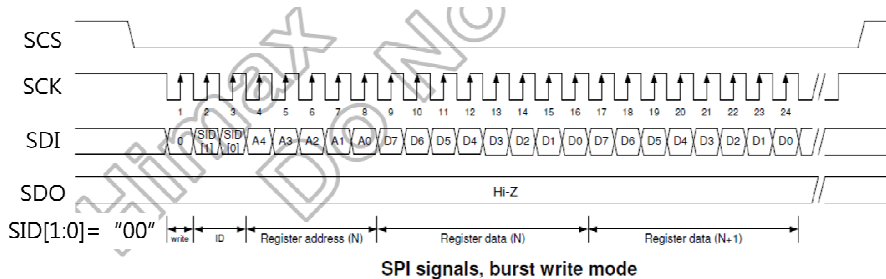


6.9 SPI Interface

6.9.1 SPI normal read/write mode

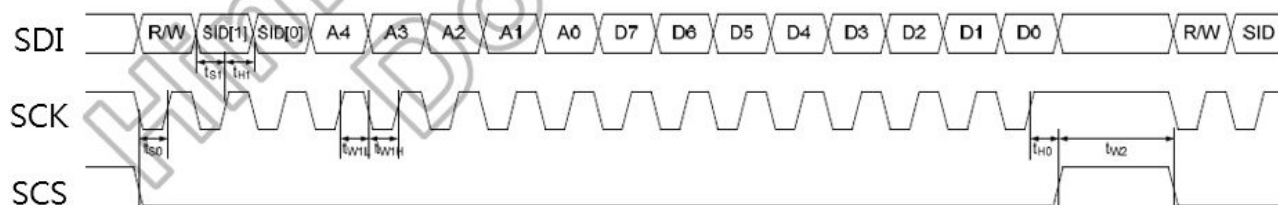


6.9.2 SPI burst read/write mode



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6.9.3 SPI Timing



SPI signal timing

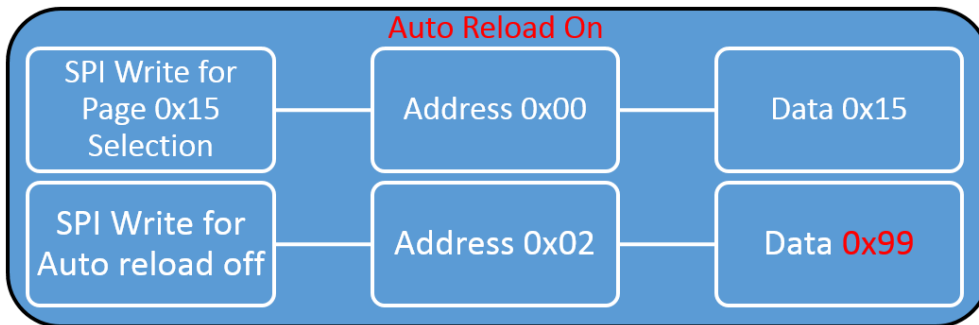
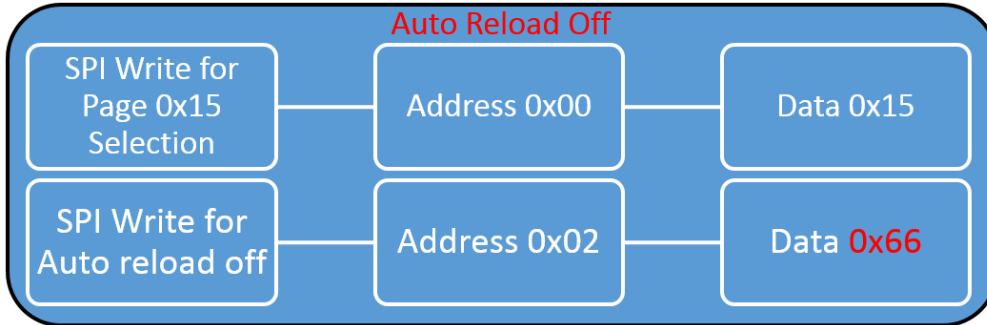
Parameter	Symbol	Conditions	Spec			Unit
			Min.	Typ.	Max.	
SDI Setup Time	t_{s0}	SCS to SCK	60	-	-	Ns
	t_{s1}	SDI to SCK	60	-	-	Ns
SDI Hold Time	t_{H0}	SCS to SCK	60	-	-	Ns
	t_{H1}	SDI to SCK	60	-	-	Ns
Pulse Width	t_{W1L}	SCK pulse width	100	-	-	Ns
	t_{W1H}	SCK pulse width	100	-	-	Ns
	t_{W2}	SCS pulse width	1	-	-	Us
Clock duty	-		40	50	60	%

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6.9.4 SPI register

6.9.4.1 Auto reload

Before read/write register content, auto reload function need to be off.

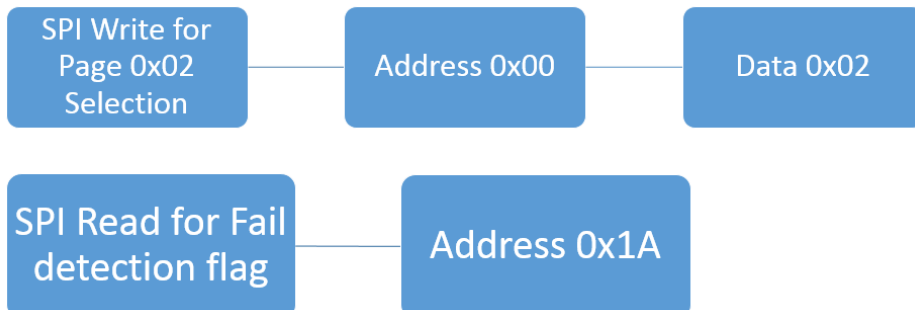


6.9.4.2 Fail detection flag(read only)

Page2_12h[6] for Fail flag Group Select(Fail_FLAG_GP_SEL).

0 for Group 1(Default). Page2_12h=0x35

1 for Group 2. Page2_12h=0x75



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Fail_FLAG_GP_SEL	Fail_FLAG[7:0]								Fail Function	Note
0 (Group 1)	-	-	-	-	-	-	-	1	LVDS lock	1
	-	-	-	-	-	-	1	-	GAS function	2
	-	-	-	-	-	1	-	-	Internal source circuit	3
	-	-	-	-	1	-	-	-	Tradition gate signal	4
	-	-	-	1	-	-	-	-	Self-protection mode	5
	-	-	1	-	-	-	-	-	EEPROM reload	6
	-	1	-	-	-	-	-	-	OTP trimming	7
	1	-	-	-	-	-	-	-	PFM abnormal	8
1 (Group 2)	-	-	-	-	-	-	-	1	Glass crack	9
	-	-	-	-	-	-	1	-	OTP reload	10

Note 1: No LVDS CLK or LVDS Timing out spec.

Note 2: GAS (gate all select). Any one of the following cases will trigger GAS function.

Cases 1. VCC lower than 2.5V Case 2. VSP lower than +4V Case 3. VSN higher than -4V.

Note 3: Source IC internal LD Signal fail.(Latch data signal fail in Source Driver)

Note 4: STV signal fail.

Note 5: No video (No LVDS CLK).

Note 6: Unused.

Note 7: Internal used for Hannstar.

Note 8: VSP/VSN power fail.

Note 9: Glass crack fail function detect is not available.

Note 10: OTP reload fail. Driver IC will compare the reload value with one of the default register value. If reload value is different than default value. The fail flag will be high.

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6.9.4.3 SPI register protected by auto-reload

Page0			Page1			Page2		
Group	Address	Data	Group	Address	Data	Group	Address	Data
	00	00		00	01		00	02
1	01	41	7	05	04	A	02	8F
	02	A1					03	4F
	03	2E					04	54
	04	50					05	35
							06	AF
							07	AF
							0E	08
							12	35
							13	15
							08	75
							09	75

Page3			Page6		
Group	Address	Data	Group	Address	Data
	00	03		00	06
D	01	05	E	01	05
	02	11		02	11
	03	0E		03	0E
	04	10		04	10
	05	0E		05	0E
	06	0E		06	0E
	07	15		07	15
	08	20		08	20
	09	2B		09	2B
	0A	2E		0A	2E
	0B	30		0B	30
	0C	25		0C	25
	0D	1E		0D	1E
	0E	23		0E	23
	0F	2E		0F	2E
10	18	10	18		
11	0E	11	0E		
12	1B	12	1B		
13	22	13	22		
14	1F	14	1F		

Page8			PageC			Page2		
Group	Address	Data	Group	Address	Data	Group	Address	Data
	00	08		00	0C		00	02
10	07	00	15	02	99	B	17	VCOM[8]
	08	1F						18

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Page9			PageA			PageB		
Group	Address	Data	Group	Address	Data	Group	Address	Data
	00	09		00	0A		00	0B
12	01	DGMA-R	13	01	DGMA-G	14	01	DGMA-B
	02			02			02	
	03			03			03	
	04			04			04	
	05			05			05	
	06			06			06	
	07			07			07	
	08			08			08	
	09			09			09	
	0A			0A			0A	
	0B			0B			0B	
	0C			0C			0C	
	0D			0D			0D	
	0E			0E			0E	
	0F			0F			0F	
	10			10			10	
	11			11			11	
	12			12			12	
	13			13			13	
	14			14			14	
15	15	15						
16	16	16						
17	17	17						
18	18	18						
19	19	19						
1A	1A	1A						
1B	1B	1B						
1C	1C	1C						
1D	1D	1D						
1E	1E	1E						

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7.0 RELIABILITY TEST ITEMS

No.	Item	Conditions	Remark
1	High Temperature Storage	Ta=+90°C, 500hrs	1, 2, 3
2	Low Temperature Storage	Ta=-40°C, 500hrs	1, 2, 3
3	High Temperature Operation	Ta=+85°C, 500hrs	1, 2, 3
4	Low Temperature Operation	Ta=-30°C, 500hrs	1, 2, 3
5	High Temperature and High Humidity (operation)	Ta=+60°C, 90%RH, 240hrs	1, 2, 3
6	Thermal Cycling Test (non operation)	-30°C(30min) → +85°C(30min), 100 cycles	1, 2, 3
7	Electrostatic Discharge	R=330Ω,C=150pF Contact = ± 8 kV, class B; Air = ± 15 kV, class B; 1 time for each point.	
8	Vibration	1.Random: 1.04G, 10~500Hz, XYZ, 30min/each direction 2.Sine: Freq.1.5G, 8~33.3Hz, Stoke: 1.3mmhz Sweep: 2.9G, 33.3~400 X/Z: 2hrs, Y:4hrs	
9	Shock	Half-Sine, 100G, 6ms, ±XYZ, 1time	
10	Vibration (with carton)	Random: 0.015G ² /Hz, 5~200Hz -6dB/Octave, 200~400Hz XYZ 2hrs/each direction	
11	Drop (with carton)	Drop height condition, basis on the product weight and follow QB100-0027 1 corner, 3 edges, 6 surfaces	

Note1: There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

Note2: The test result shall be evaluated after the sample has been left at room temperature and humidity for 2 hours without load. No condensation shall be accepted. The sample shall be free from defects:

(Air bubble in the LCD 、 Seal leak 、 Non-display 、 Missing segments 、 Glass crack).

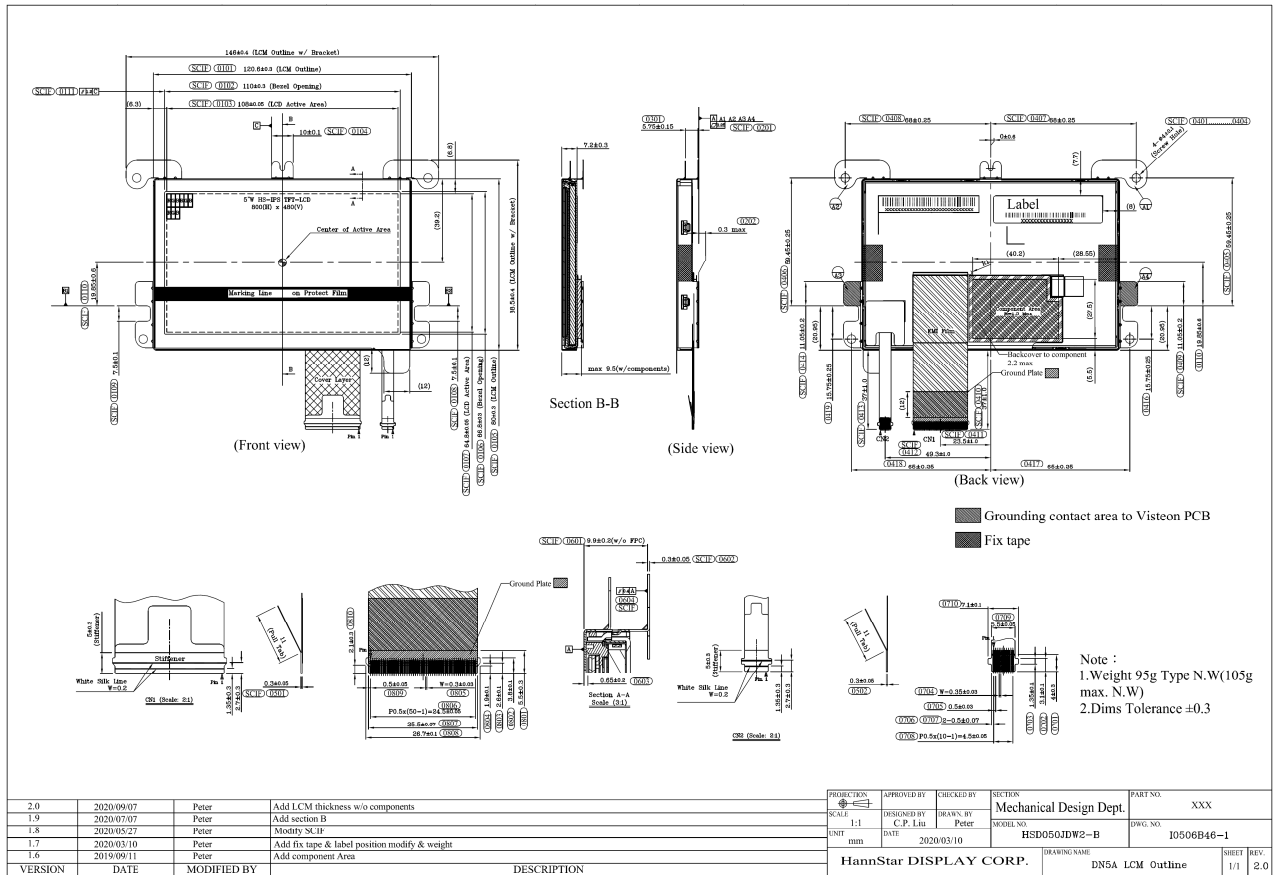
Note3: The test condition definition panel's surface temperature.

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8.0 OUTLINE DIMENSION

Unit : mm

Protective foil with pull tape will be added on finish good.



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9.0 LOT MARK

9.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

Code 1,2,3,4,5,6: HannStar internal flow control code.

Code 7: production location.

Code 8: production year.

Code 9: production month.

Code 10,11,12,13,14,15: serial number.

Note (1) Production Year: Code 8 is defined by the last number of the year, for example

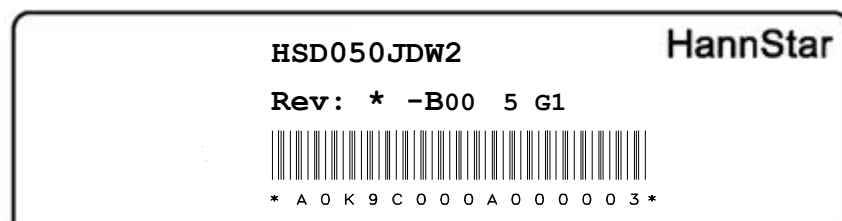
Year	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025
Mark	6	7	8	9	0	1	2	3	4	5

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

9.2 Detail of Lot Mark

- (1) Below label is attached on the backside of the LCD module. See Section 8.0: Outline Dimension.
- (2) The detail of Lot Mark is attached as below.
- (3) This is subject to change without prior notice.



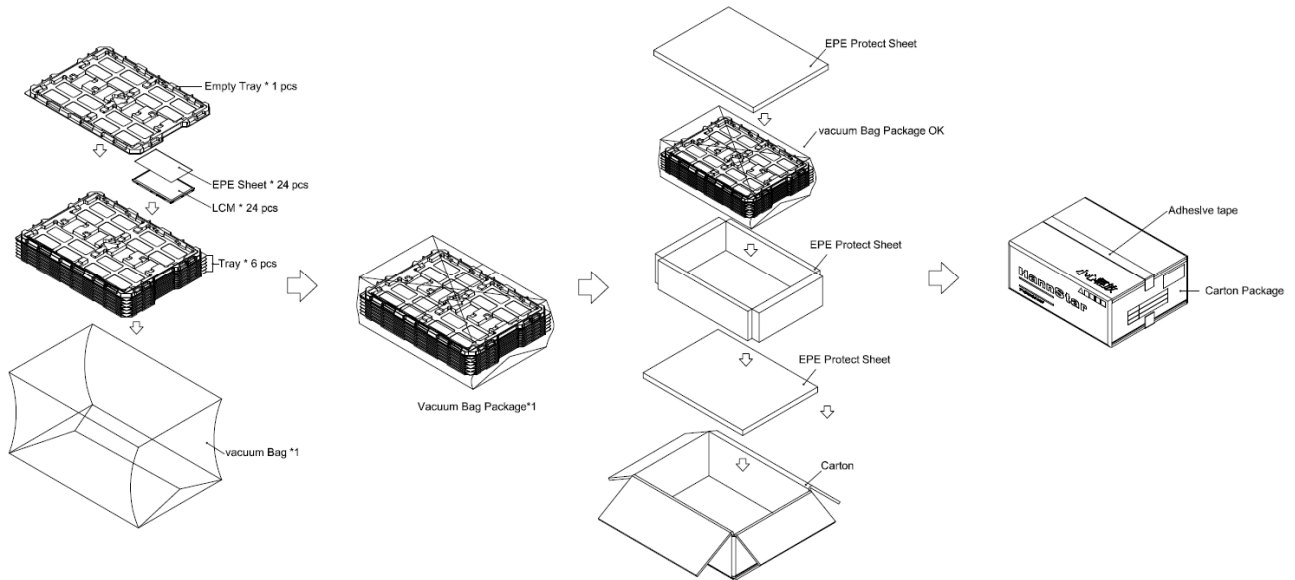
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10.0 PACKAGE SPECIFICATION

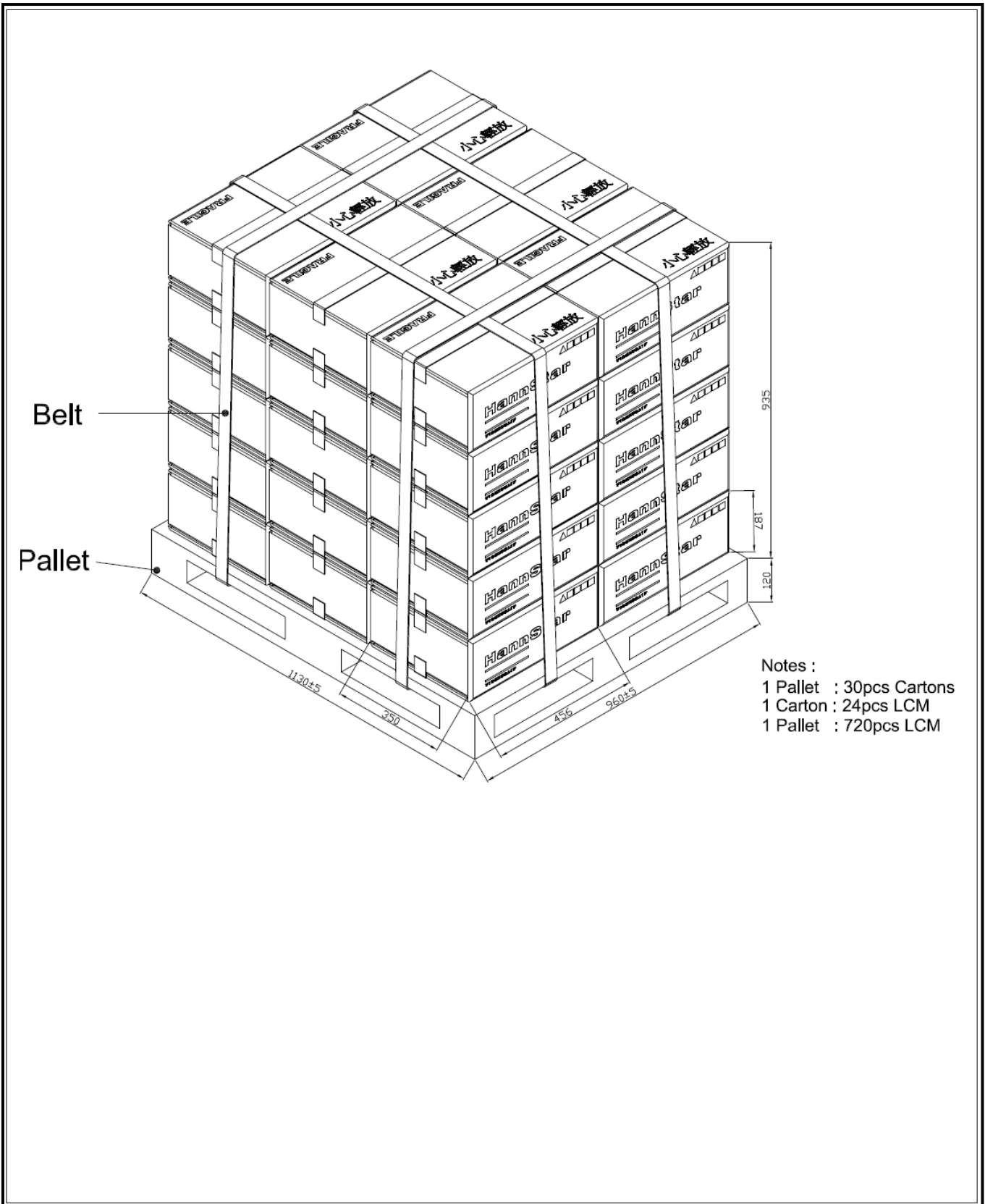
10.1 Packing form

- (1) Package quantity in one carton: 24 pieces (6 trays x 4pcs)
- (2) Carton size: 456 mm×350 mm×187 mm.

10.2 Packing assembly drawings (24pcs/CTN)



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11.0 GENERAL PRECAUTION

11.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

11.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

11.3 Breakage of LCD Panel

13.3.1. If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

13.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

13.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

13.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

11.4 Electric Shock

13.4.1. Disconnect power supply before handling LCD module.

13.4.2. Do not pull or fold the LED cable.

13.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

11.5 Absolute Maximum Ratings and Power Protection Circuit

13.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

13.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

13.5.3. It's recommended to employ protection circuit for power supply.

11.6 Operation

13.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

13.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

13.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

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13.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

13.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

11.7 Mechanism

Please mount LCD module by using mounting holes arranged in four corners tightly.

11.8 Static Electricity

13.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

13.8.2 Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

11.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

11.10 Disposal

When disposing LCD module, obey the local environmental regulations.

11.11 Optical Bonding

Before CL/TP bonding, LCM must pre baking by 80°C/8hr.



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