DATA MODUL

SPECIFICATION

HannStar

HSD070GWW5-900001-P

7" - WXGA - MIPI

Version: 1.0
Date: 18.10.2023

Note: This specification is subject to change without prior notice

TO : DATA MODUL

Date : Oct.18.2023

HannStar Product Information

(Formal)

7” Color TFT-LCD Module

Model: **HSD070GWW5-900001-P**

Note: (1) The information contained herein is tentative and may be changed without prior notices.

(2) Please contact HannStar Display Corp. before designing your product based on this module specification.

(3) The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by HannStar Display Corp. for any intellectual property claims or other problems that may result from application based on the module described herein.

Record of Revisions

Rev.	Date	Sub-Model	Description of change
1.0	Oct.18.2023	-900001-P	Formal Product Information was first released

Contents

1.0 GENERAL DESCRIPTION

Introduction

HannStar Display model HSD070GWW5-900001-P is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back- light system. This TFT LCD has a 7.0 inch (10:16) diagonally measured active display area with WXGA (800 horizontal by 1280 vertical pixel) resolution.

1.1 Features

- 7 inch configuration
- 16.7M color by MIPI 4lane interface
- ROHS / Halogen Free Compliance

1.2 Applications

- TFT LCD Monitor
- Industrial Application
- Amusement

1.3 General information

Item		Specification	Unit
LCM outline dimension(LCM)		99.81(W) x 161.66(H) x 2.48(D)	mm
Display area		94.2(W) x 150.72(H)	mm
Number of Pixel		800RGB x 1280	pixels
Pixel pitch		0.11775(W) x 0.11775(H)	mm
Pixel arrangement		RGB Vertical Stripe	
Display mode		Normally Black	
Interface		MIPI	
NTSC		60	%
Surface treatment		AG	
Weight		79.5(Typ.)	g
Power Consumption	Logic System	0.135(Typ.)	W
	B/L System	1.28(Typ.)	W

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Analog Supply voltage	VCC	2.5	6.6	V	GND=0
Digital supply voltage	IOVCC	1.65	3.6	V	GND=0
Logic Input voltage	Vin	-0.3	IOVCC+0.3	V	GND=0

Note (1):

Permanent damage may occur to the LCD module if beyond this specification.

Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2):

Ta =25±2℃

2.1 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_{opa}	-20	70	℃	(3),(4)
Storage Temperature	T_{stg}	-30	80	℃	(3),(4)

Note (3):

If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note (4):

The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

3.0 OPTICAL CHARACTERISTICS

3.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast		CR	Θ=0 Normal viewing angle	600	800	—		(1)(2)
Response time		Tr		—	10	15	msec	(1)(3)
		Tf			20	25	msec	(1)(3)
White luminance		Y_L		300	350	—	cd/m^2	(1)(4)
Color Gamut		S(%)		—	60	—	%	
Color chromaticity (CIE1931)	White	W_x		0.272	0.302	0.332		(1)(4)
		W_y		0.286	0.316	0.346		
	Red	R_x		0.597	0.627	0.657		
		R_y		0.324	0.354	0.384		
	Green	G_x		0.331	0.361	0.391		
		G_y		0.563	0.593	0.623		
	Blue	B_x		0.115	0.145	0.175		
		B_y		0.038	0.068	0.098		
Viewing angle	Hor.	Θ_L	CR>10	—	85	—		
		Θ_R		—	85	—		
	Ver.	Θ_U		—	85	—		
		Θ_D		—	85	—		
Brightness Uniformity		B_{UNI}	Θ=0	80	--		%	(5)
Optima View Direction		ALL						

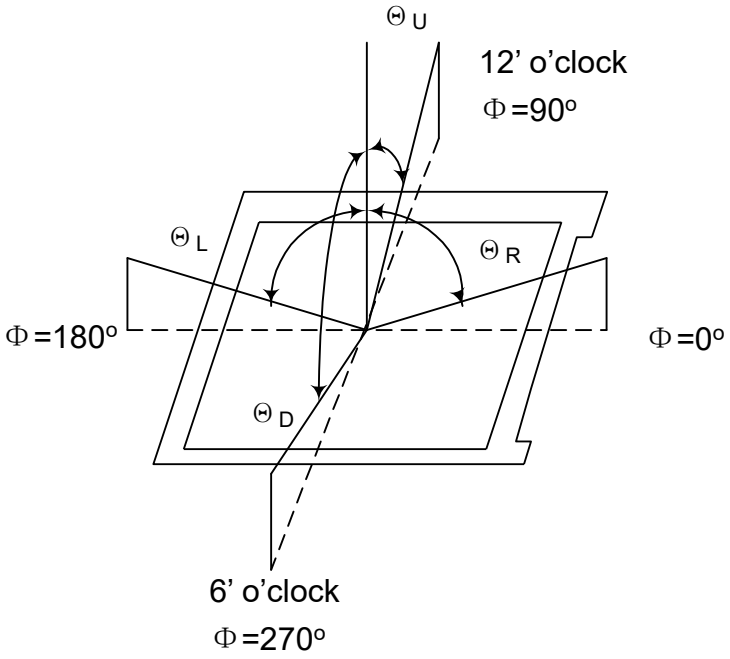
3.2 Measuring Condition

- Measuring surrounding：dark room
- LED current I_L：80mA
- Ambient temperature：25±2°C
- 15min. warm-up time.

3.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-7A for other optical characteristics.
- Measuring spot size: 20 ~ 21 mm

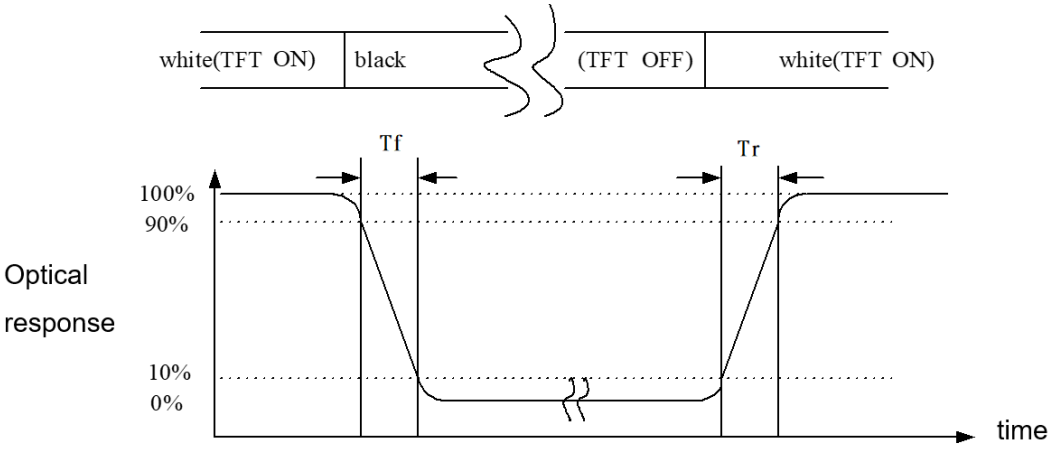
Note (1) Definition of Viewing Angle:



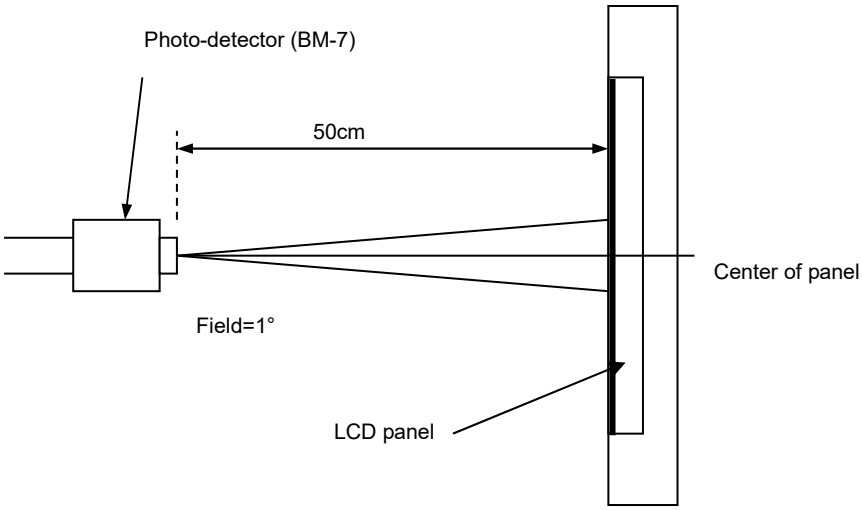
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

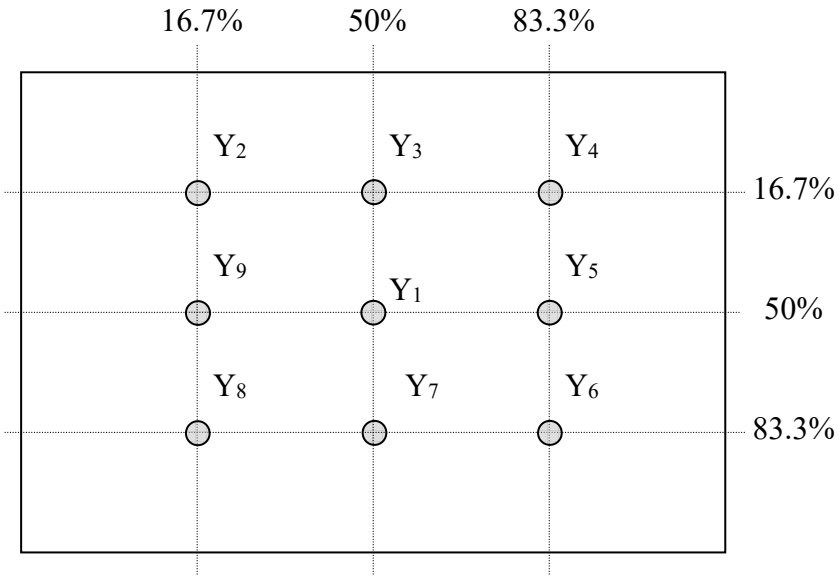
Note (3) Definition of Response Time : Sum of Tr and Tf



Note (4) Definition of optical measurement setup



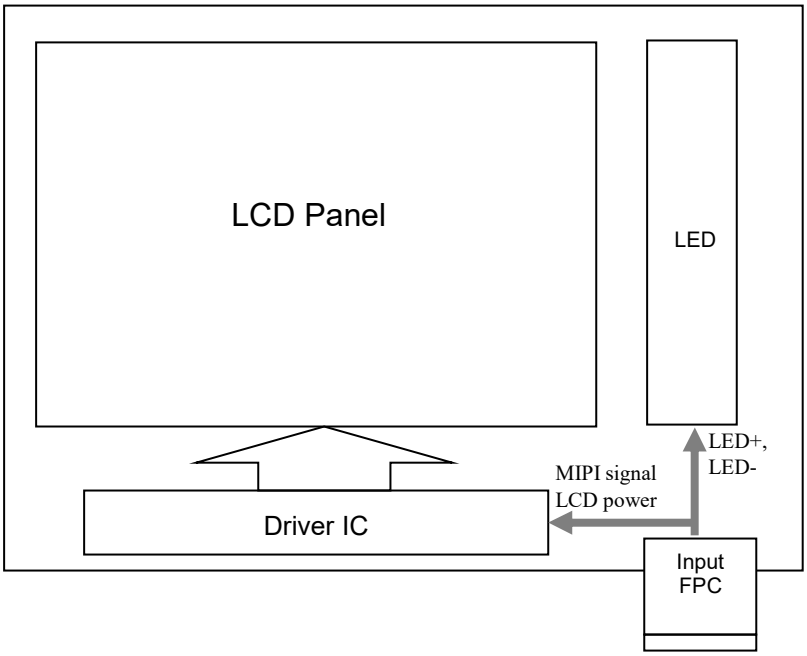
Note (5) Definition of brightness uniformity



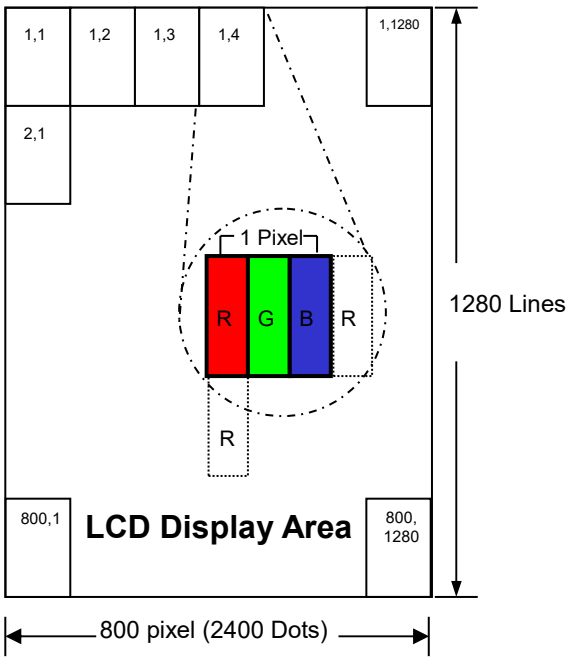
$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

4.0 BLOCK DIAGRAM

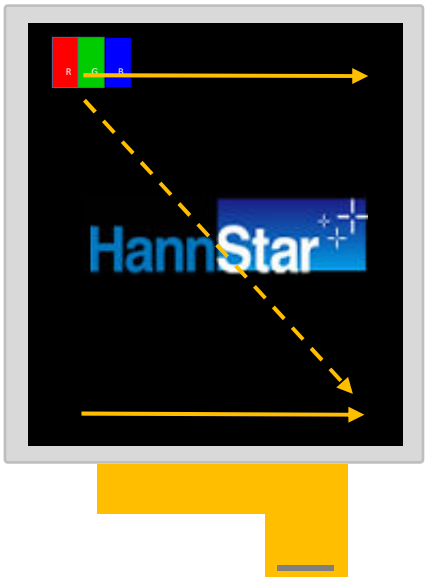
4.1 TFT LCD Module



4.2 Pixel Format



4.3 Display Scanning Direction



5.0 INTERFACE PIN CONNECTION

5.1FPC Pin Assignment

The used Connector：AEX630124 manufactured by AEX

No.	Symbol	Functions
1	MIPI_D0N	Negative polarity of low voltage differential data0 signal
2	MIPI_D0P	Positive polarity of low voltage differential data0 signal
3	GND	Power Ground
4	MIPI_D1N	Negative polarity of low voltage differential data1 signal
5	MIPI_D1P	Positive polarity of low voltage differential data1 signal
6	GND	Power Ground
7	MIPI_CLKN	Negative polarity of low voltage differential clock signal
8	MIPI_CLKP	Positive polarity of low voltage differential clock signal
9	GND	Power Ground
10	MIPI_D2N	Negative polarity of low voltage differential data2 signal
11	MIPI_D2P	Positive polarity of low voltage differential data2 signal
12	GND	Power Ground
13	MIPI_D3N	Negative polarity of low voltage differential data3 signal
14	MIPI_D3P	Positive polarity of low voltage differential data3 signal
15	GND	Power Ground
16	VDDIN	VDDIN PIN
17	VDDIN	VDDIN PIN
18	GND	Power Ground
19	RESET	Reset Pin(For display driver)
20	GND	Power Ground
21	LED_PWM	LED_PWM PIN
22	GND	Power Ground
23	AVEE	AVEE PIN
24	AVDD	AVDD PIN
25	GND	Power Ground
26	LED-	Power supply for backlight cathode input terminal.
27	LED-	Power supply for backlight cathode input terminal.
28	LED+	Power supply for backlight anode input terminal.
29	LED+	Power supply for backlight anode input terminal.
30	NC	Not connect

Notes:

1. NC pin must be retained; this pin can’t contact GND or other signal
2. GND pin must ground contact, cannot be floating

6.0 ELECTRICAL CHARACTERISTICS

6.1 TFT LCD Module

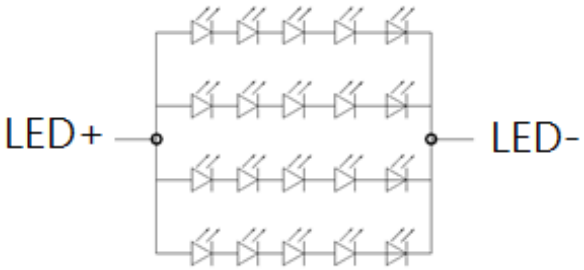
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	VDDIN	1.65	-	3.6	V	
Positive Voltage input	AVDD	5.3	5.5	5.8	V	
Negative Voltage input	AVEE	-5.8	-5.5	-5.3	V	
Supply current	I_{VDDIN}	-	25	31.25	mA	VDDIN=1.8V, @white pattern
Positive Voltage input current	I_{AVDD}	-	8	10	mA	AVDD=5.5V, @white pattern
Negative Voltage input current	I_{AVEE}	-	8	10	mA	AVEE=-5.5V, @white pattern
Logic input voltage	VIH	0.7*VDDIN	-	VDDIN	V	
	VIL	GND	-	0.3*VDDIN	V	

6.2 Backlight Unit

Parameter	Symbol	Min	Typ	Max	Units	Condition
LED Light Bar Current	ILED	--	80	--	mA	Ta=25℃
LED Light Bar Voltage	VLED+	14	16	18	Volt	Ta=25℃
LED Life-Time	N/A	20,000	--	--	Hour	Ta=25℃ Note (1)

Note (1) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃. and ILED=80mA. The LED lifetime could be decreased if operating ILED is larger than 80mA. The constant current driving method is suggested.

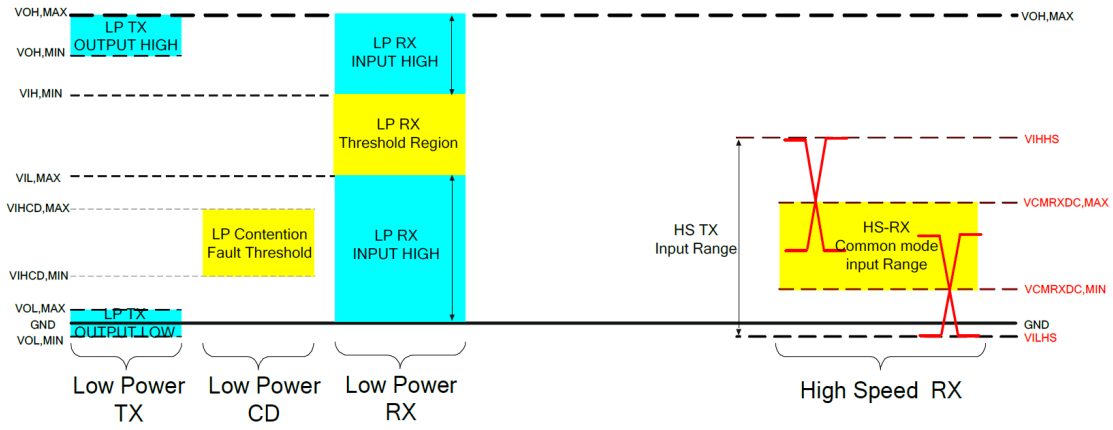
Note (2) LED Light Bar Circuit



6.3 MIPI characteristics

6.3.1 The electrical specifications of HS and LP

6.3.1.1 HS and LP signal levels



6.3.1.2 The Electronic Characteristics of Low-Power Transmitter (TX)

LP-TX DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
V_{OL}	Thevenin output low level	-50	-	50	mV	
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1)Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

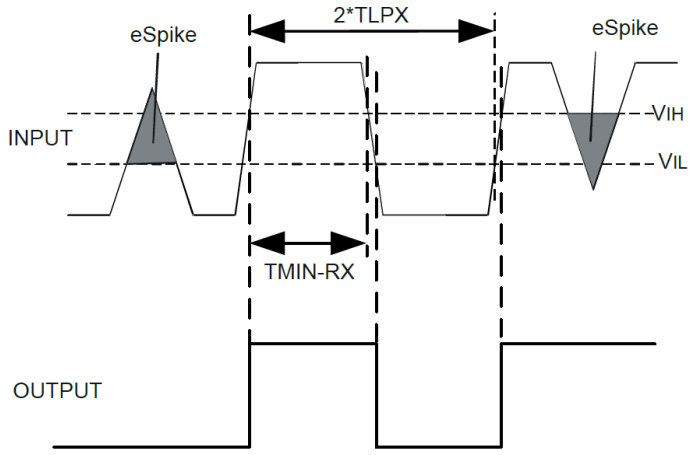
LP-TX AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0pF	30	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 5pF	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 20pF	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 70pF	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (VO,INST- 700)	-	-	mV/ns	(1),(8),(9)
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
C_{LOAD}	Load capacitance	-	-	70	pF	-

Note: (1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
(2) When the output voltage is between 400 mV and 930 mV.
(3) Measured as average across any 50 mV segment of the output signal transition.
(4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
(5) This value represents a corner point in a piecewise linear curve.
(6) When the output voltage is in the range specified by VPIN(absmax).
(7) When the output voltage is between 400 mV and 700 mV.
(8) Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
(9) When the output voltage is between 700 mV and 930 mV.

6.3.1.3 The Electronic Characteristics of Receiver (RX)

Input Glitch Rejections of Low-Power Receivers



LP-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input threshold	880	-	-	mV	-
V_{IL}	Logic 0 input threshold, not in ULP state	-	-	550	mV	-

LP-RX AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	1, 2, 3
T_{MIN}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state
(2) An impulse less than this will not change the receiver state.
(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
(4) An input pulse greater than this shall toggle the output.

HS-RX DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDTL}	Differential input low threshold	-70	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.
(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

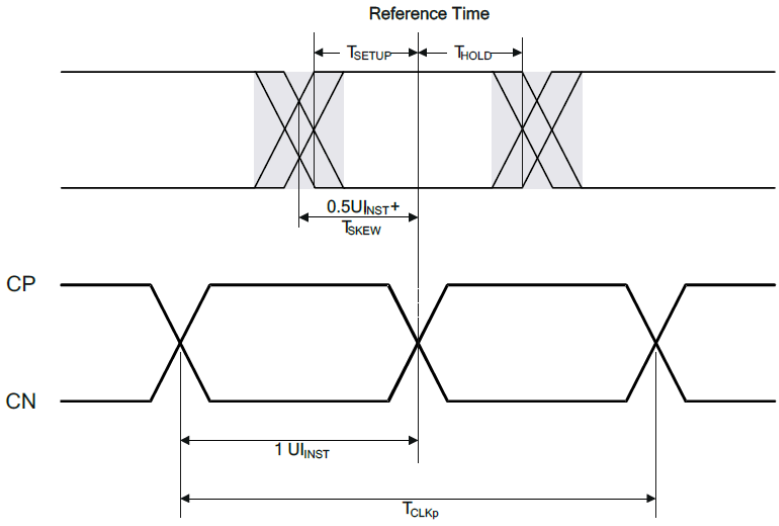
HS-RX AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV_{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) ΔVCMRX(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

6.3.1.4 High-Speed Data-Clock Timing

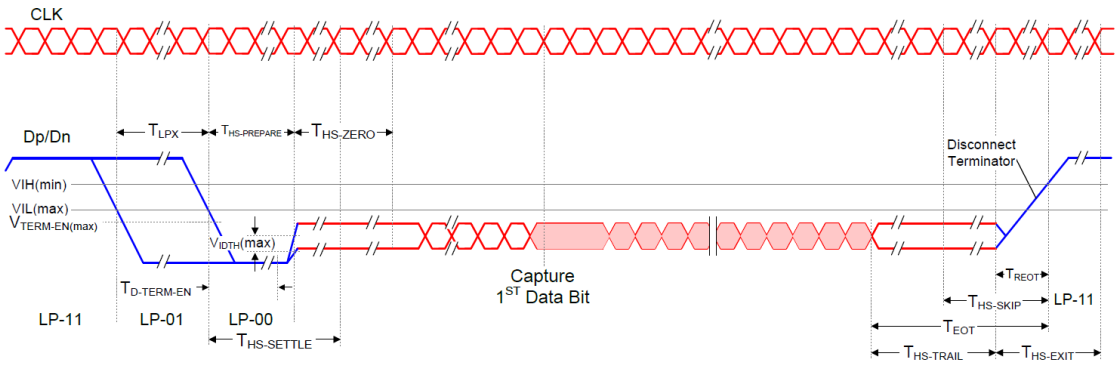
Data to Clock Timing Definitions



Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [RX]	$T_{SETUP[RX]}$	0.15	-	-	UIINST	1
Clock to Data Hold Time [RX]	$T_{HOLD[RX]}$	0.15	-	-	UIINST	1

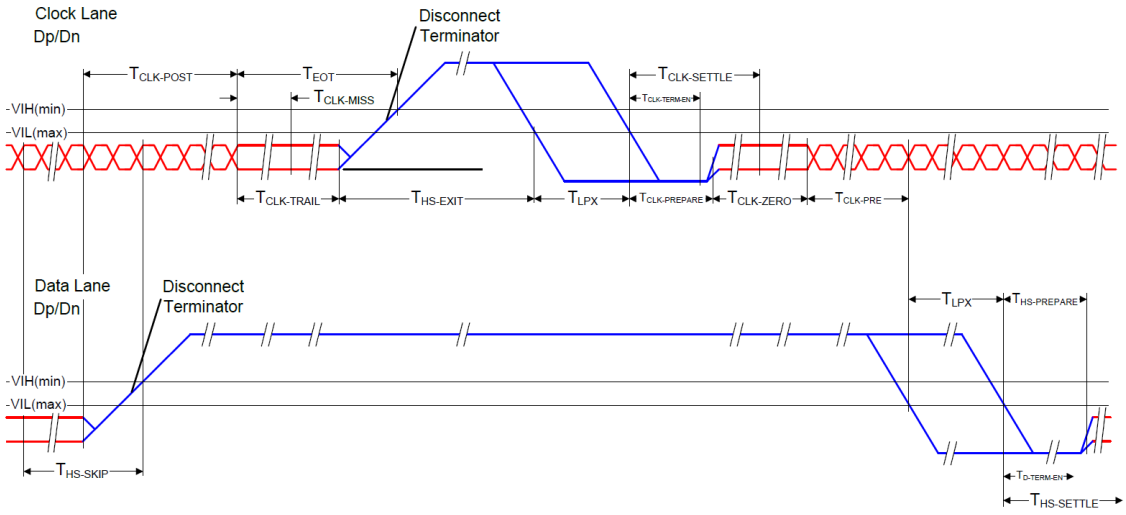
Note: (1) Total setup and hold window for receiver of 0.3*UIINST.

6.3.2 Burst Mode Data Transmission



Parameter	Description	Min	Typ	Max	UNIT
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 + 4*UI	-	85 + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 + 10*UI	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination.	-	-	35 + 4*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions.	85 + 6*UI	-	145 + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 + n*4*UI)	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

6.3.3 Switching the Clock Lane between Clock Transmission and Low-Power Mode

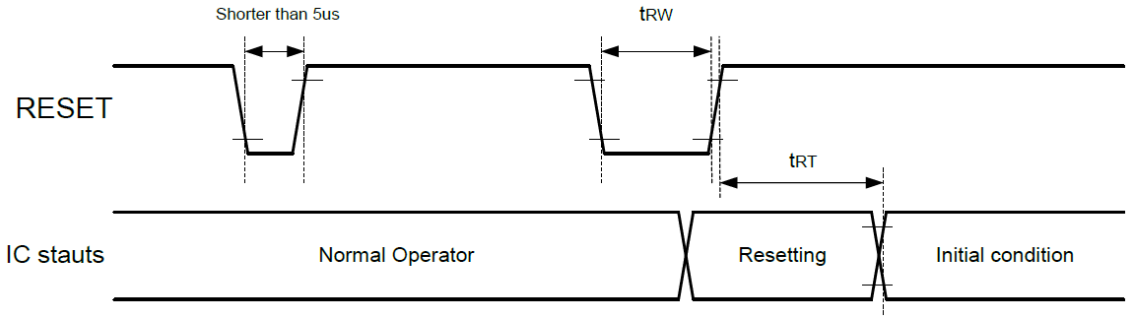


Parameter	Description	Min	Typ	Max	UNIT
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode.	60 + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8*UI	-	-	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination.	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100	-	-	ns

6.3.4 Timings for DSI Video mode

Item	Symbol	Value			Unit
		Min.	Typ.	Max.	
HS low pulse width	HS	10	20	30	DCK
Horizontal back porch	HBP	52	60	70	DCK
Horizontal front porch	HFP	50	60	70	DCK
Horizontal blanking period	HBLK	112	140	170	DCK
Horizontal active area	HDISP	800			DCK
Pixel Clock	PCLK	71	75	82	MHz
Vertical low pulse width	VS	2	4	40	Line
Vertical back porch	VBP	14	20	40	Line
Vertical front porch	VFP	8	20	60	Line
Vertical blanking period	VBK	24	44	180	Line
Vertical active area	-	1280			Line
Vertical Refresh rate	VRR	60			Hz

6.4 Reset input timings



Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESET	10	-	μs
t_{RT}	Reset complete time(3)	-	-	5 (Note 4)	ms
		-	-	120 (Note 5, 6)	ms

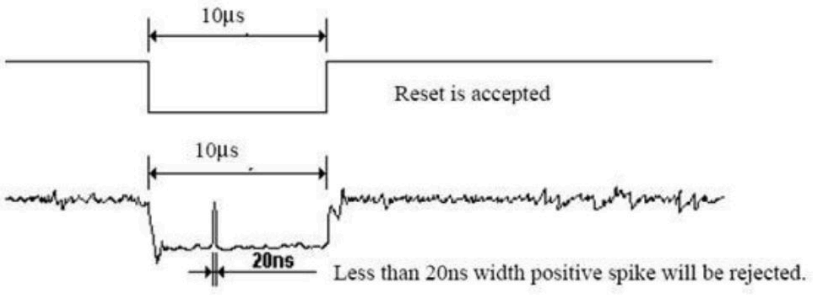
Note:

(1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(3) Spike Rejection also applies during a valid reset pulse as shown below:



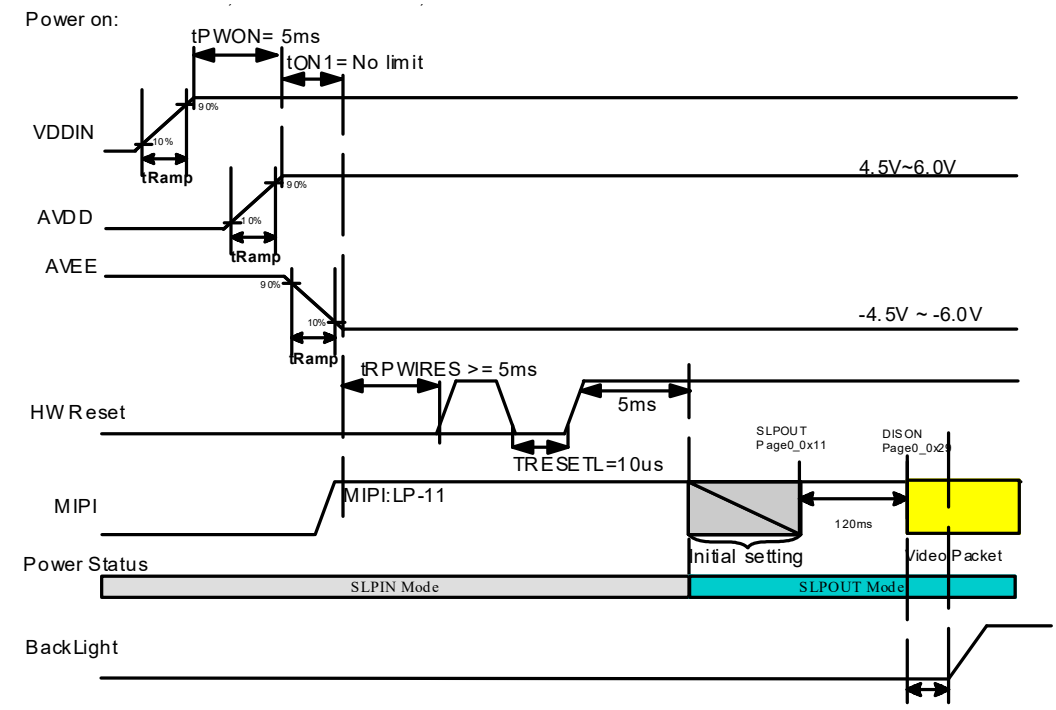
(4)When Reset is applied during Sleep In Mode.

(5)When Reset is applied during Sleep Out Mode.

(6) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(7) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

6.5 Power Sequence



Note: tON1: The space time between AVDD Power On and AVEE Power On. tBLON>=0 us

7.0 RELIABILTY TEST ITEMS

7.1 Test condition

No.	Item	Conditions	Remark
1	High Temperature Storage	Ta=+80℃, 240hrs	1,2,3
2	Low Temperature Storage	Ta=-30℃, 240hrs	1,2,3
3	High Temperature Operation	Ta=70℃, 240hrs	1,2,3
4	Low Temperature Operation	Ta=-20℃,240hrs	1,2,3
5	High Temperature and High Humidity (operation)	Ta=60℃, 90%RH, 240Hrs	1,2,3
6	Thermal Cycling Test (non operation)	-30℃(0.5hr)←→80℃(0.5hr),200cycle	1,2,3

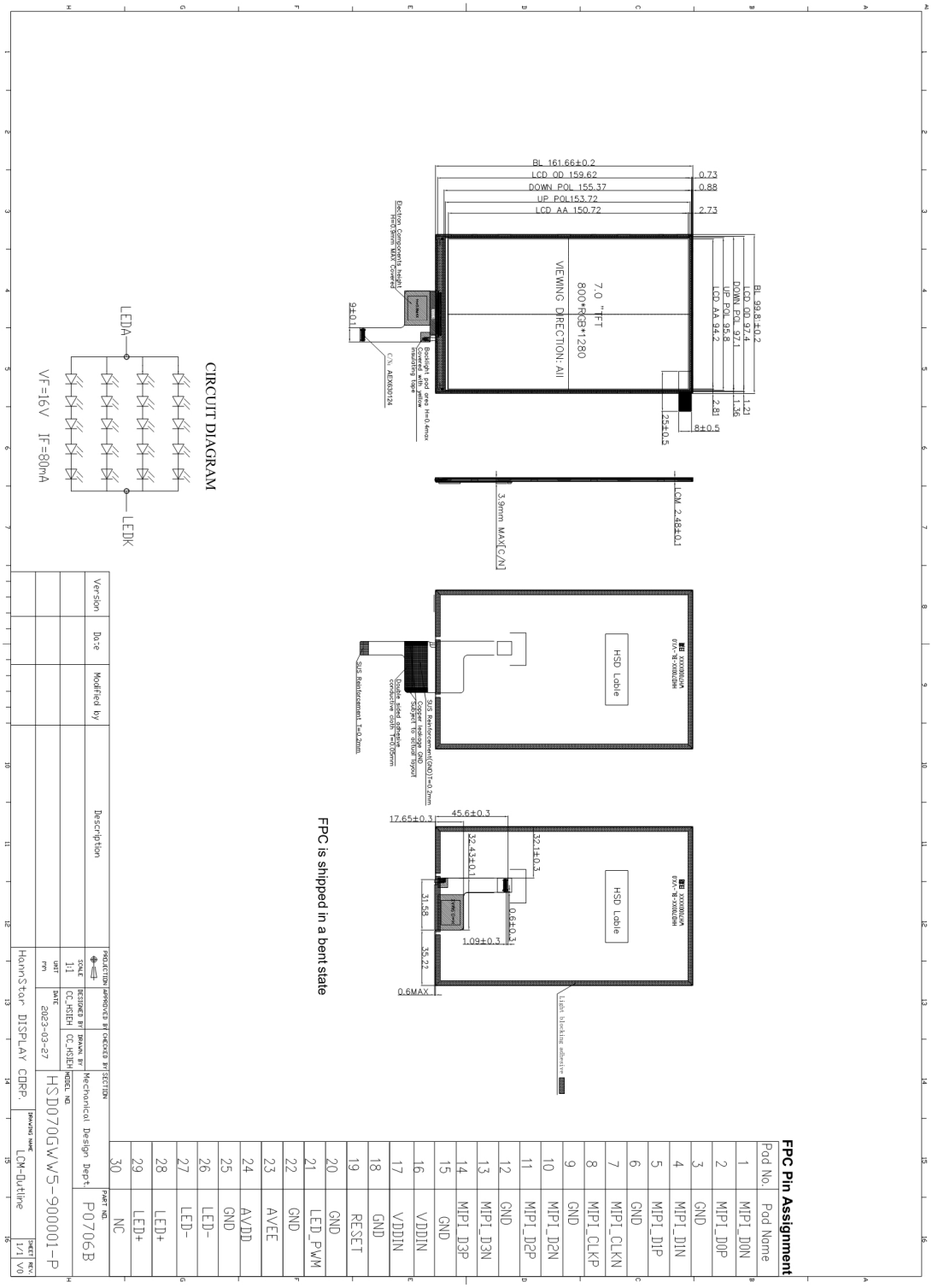
Note1: There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

Note2: All of the function & cosmetic Judgment basis base on room temperature.
(The tested module must have enough recovery time at least 2 hours at room temperature.)

Note3: The test condition definition panel's surface temperature.

8.0 OUTLINE DIMENSION

Unit : mm



FPC Pin Assignment

Pod No.	Pod Name
1	MIPI_DON
2	MIPI_DOP
3	GND
4	MIPI_DIN
5	MIPI_DIP
6	GND
7	MIPI_CLKN
8	MIPI_CLKP
9	GND
10	MIPI_D2N
11	MIPI_D2P
12	GND
13	MIPI_D3N
14	MIPI_D3P
15	GND
16	VDDIN
17	VDDIN
18	GND
19	RESET
20	GND
21	LED_PWM
22	GND
23	AVEE
24	AVDD
25	GND
26	LED-
27	LED-
28	LED+
29	LED+
30	NC

Version | Date | Modified by | Description

HannStar DISPLAY CORP. | Mechanical Design Dept. | HSD070GWW5-900001-P | P0706B | LCM-Outline | 1:1 | V0

Note: General tolerance: +/- 0.3mm

9.0 LOT MARK

9.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Code 1,2,3,4,5,6: HannStar internal flow control code.
Code 7: production location.
Code 8: production year.
Code 9: production month.
Code 10,11,12,13,14,15: serial number.

Note (1) Production Year: Code 8 is defined by the last number of the year, for example

Year	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Mark	6	7	8	9	0	1	2	3	4	5	6

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

9.2 Detail of Lot Mark

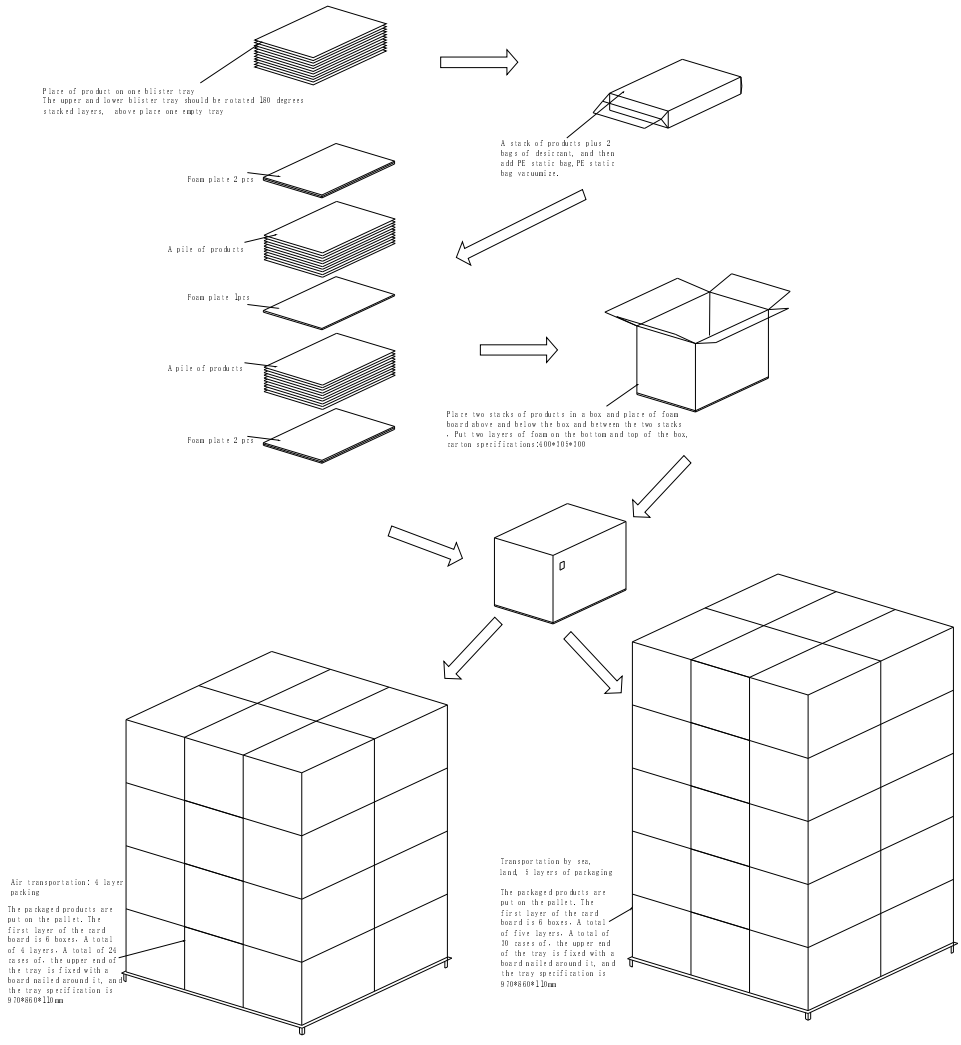
(1) Below label is attached on the backside of the LCD module. See Section 8.0: Outline Dimension.
(2) The detail of Lot Mark is attached as below.
(3) This is subject to change without prior notice.

10.0 PACKAGE SPECIFICATION

10.1 Packing Form

Packaging material	Standard	Quantity
BOX	400*305*300mm	1
Blister tray	380*285*0.8mm	26
Foam	360*265*10mm	5
Vacuum bag	650*500*0.075mm	2
Module	HSD070GWW5-900001-P	96

10.2 Pallet Drawing



11.0 GENERAL PRECAUTION

11.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

11.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

11.3 Breakage of LCD Panel

11.3.2. If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

11.3.3. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

11.3.4. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

11.3.5. Handle carefully with chips of glass that may cause injury, when the glass is broken.

11.4 Electric Shock

11.4.1. Disconnect power supply before handling LCD module.

11.4.2. Do not pull or fold the LED cable.

11.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

11.5 Absolute Maximum Ratings and Power Protection Circuit

11.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

11.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

11.5.3. It's recommended to employ protection circuit for power supply.

11.6 Operation

11.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.
11.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
11.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.
11.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
11.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

11.7 Mechanism

Please mount LCD module by using mounting holes arranged in four corners tightly.

11.8 Static Electricity

11.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
11.8.2 Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

11.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

11.10 Disposal

When disposing LCD module, obey the local environmental regulations.

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