DATA MODUL

SPECIFICATION

HannStar

HSD101GWW5-A01-P

10.1” – 1280 x 800 – LVDS

Version: 1.0
Date: 06.06.2023

Note: This specification is subject to change without prior notice

TO : DATA MODUL

Date : JUN.06.2023

HannStar Product Specification

(Formal)

10.1” Color TFT-LCD Module

Model: HSD101GWW5-A01-P

Note:

(1) Please contact HannStar Display Corp. before designing your product based on this module specification.

(2) The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by HannStar for any intellectual property claims or other problems that may result from application based on the module described herein.

(3) The mark “ ** ” of Model means sub-model code.

Record of Revisions

Rev.	Date	Sub-Model	Description of change
1.0	JUN.06.2023	-A01-P	Formal Product Information was first released.

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

HannStar Display model HSD101GWW5-A01-P is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, driving IC and a back light system. This TFT LCD has a 10.1(16:10) inch diagonally measured active display area with 1280x800 (1280 horizontal by 800 vertical pixel) resolution.

1.2 Features

- 10.1 inch configuration
- 16.7M color by 8 bit R.G.B. signal input
- RoHS Compliance & Halogen Free

1.3 Applications

- TFT LCD Monitor
- Industrial Application
- Amusement
- Vehicle

1.4 General information

Item		Specification	Unit
Outline Dimension		226 (H)x148 (V) x 4.5 (T) (Typ.) w/o FPC 226 (H)x148 (V) x 7.7 (T) (Typ.) with FPC	mm
Display area		216.96(H)x135.6(V)	mm
Number of Pixel		1280 RGB (H) x 800 (V)	pixels
Pixel pitch		0.1695 (H)x0.1695 (V)	mm
Pixel arrangement		RGB Vertical Stripe	
Display mode		Normally Black	
Interface		LVDS	
NTSC		50 (Typ.)	%
Surface treatment		Anti-glare, Hard-Coating (3H)	
Weight		238 (Typ.)	g
Power Consumption	Logic System	0.891 (Typ.)	W
	B/L System	3.96 (Typ.)	W

1.5 Mechanical Information

Item		Min.	Typ.	Max.	Unit
Module Size	Horizontal (H)	225.7	226	226.3	mm
	Vertical (V)	147.7	148	148.3	mm
	Depth (D)	4.3	4.5	4.7	mm
Weight		233	238	243	

2.0 ABSOLUTE MAXIMUM RATINGS

2.1 Electrical Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	Vcc	-0.5	4	V	GND=0
Logic Signal Input Level	VI	-0.5	VCC+0.3	V	
LED power Supply Voltage	VLED	-0.3	27	V	
EN, PWM input voltage	VEN, Vpwm	-0.3	VLED	V	

Note

(1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Ta =25±2℃

2.2 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_{opa}	-20	70	℃	
Storage Temperature	T_{stg}	-30	80	℃	

3.0 OPTICAL CHARACTERISTICS

3.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast		CR	Θ=0 Normal viewing angle	800	1000	—		(1)(2)
Response time	Rising	Tr+Tf		—	25	35	msec	(1)(3)
White luminance (Center)		Y_L		450	500	—	cd/m^2	(1)(4)
Color chromaticity (CIE1931)	White	W_x		0.260	0.290	0.320		(1)(4)
		W_y		0.280	0.310	0.340		
	Red	R_x		0.563	0.593	0.623		
		R_y		0.310	0.340	0.370		
	Green	G_x		0.333	0.363	0.393		
		G_y		0.550	0.580	0.610		
	Blue	B_x		0.109	0.139	0.169		
		B_y		0.07	0.100	0.13		
Viewing angle	Hor.	$Θ_L$	CR>10	—	80	—		
		$Θ_R$		—	80	—		
	Ver.	$Θ_U$		—	80	—		
		$Θ_D$		—	80	—		
Brightness uniformity		B_{UNI}	Θ=0	75	80	—	%	(5)
Optima View Direction		Free						

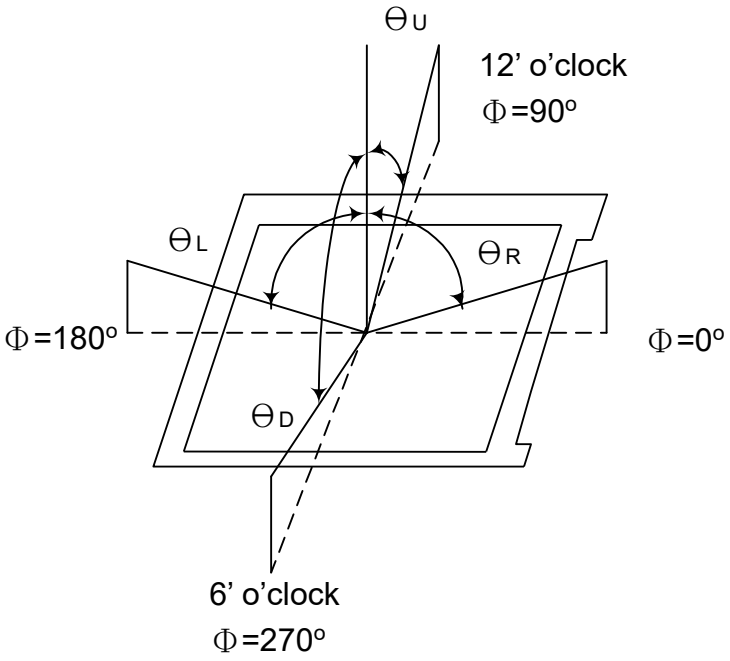
3.2 Measuring Condition

- Measuring surrounding：dark room
- Ambient temperature：25±2°C
- 15min. warm-up time.

3.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.
- Measuring spot size：20 ~ 21 mm

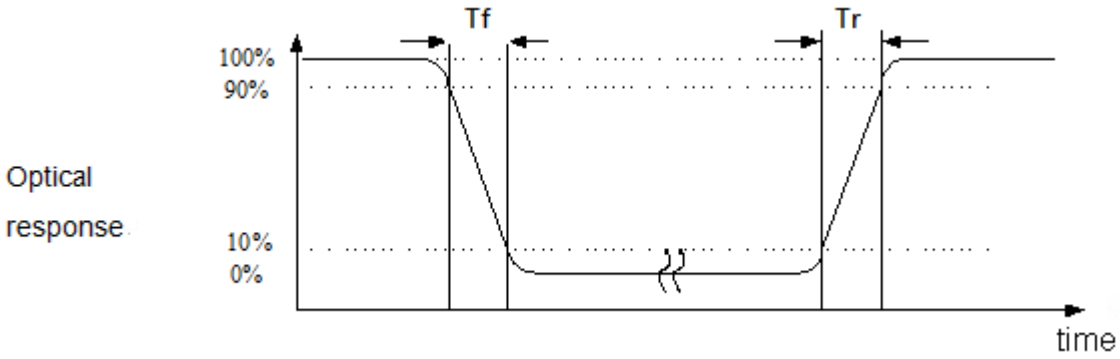
Note (1) Definition of Viewing Angle:



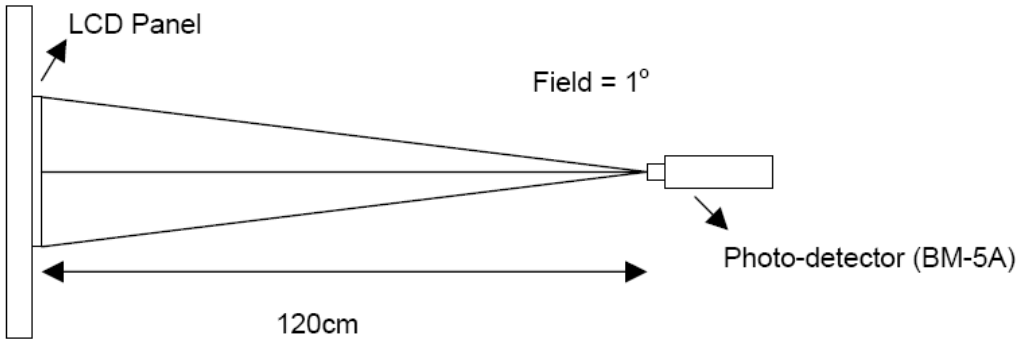
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

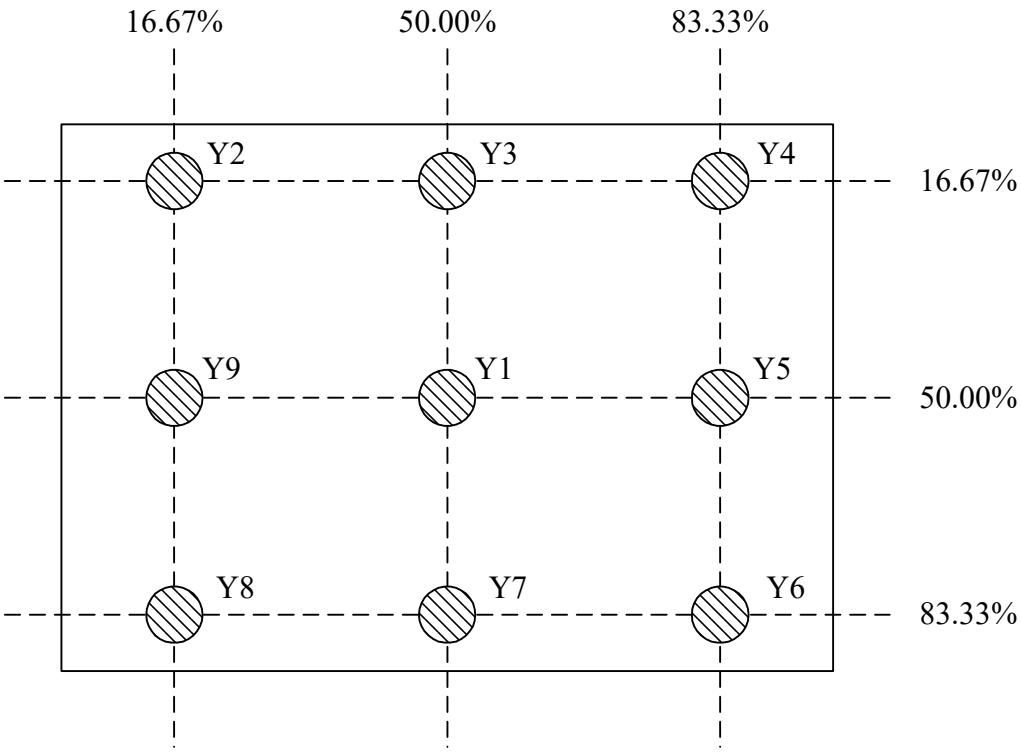
Note (3) Definition of Response Time: Sum of Tr and Tf



Note (4) Definition of optical measurement setup



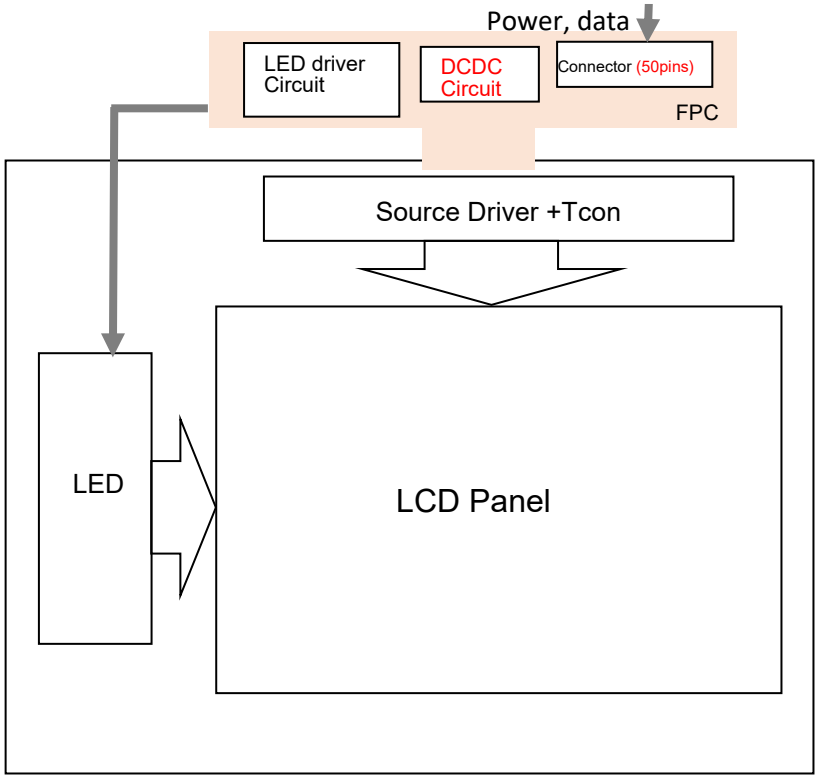
Note (5) Definition of brightness uniformity



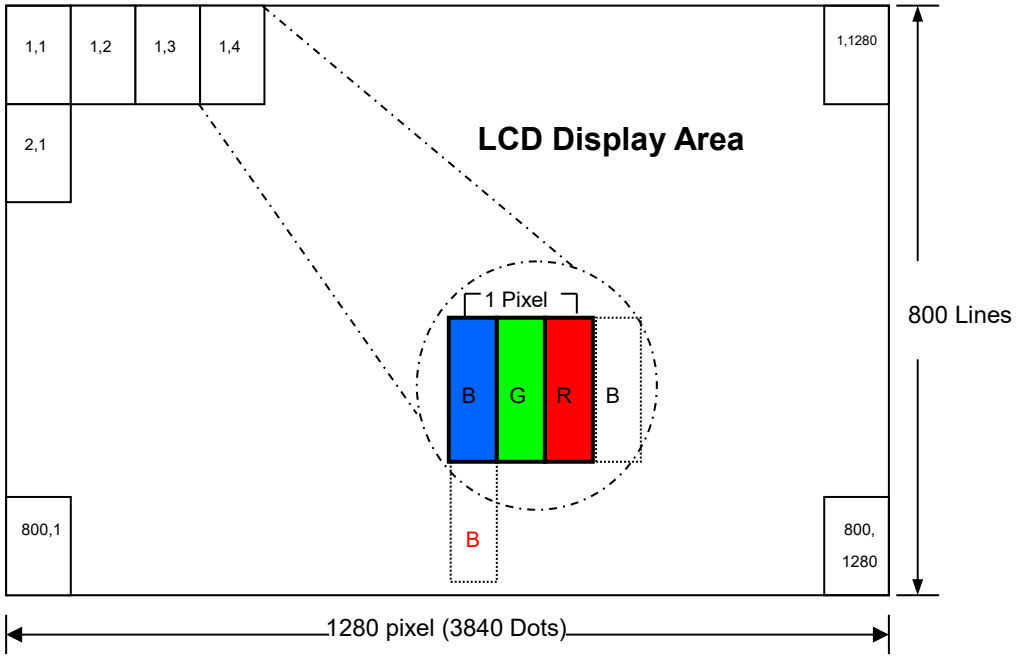
$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

4.0 BLOCK DIAGRAM

4.1 TFT LCD module



4.2 Pixel Format



5.0 INTERFACE PIN CONNECTION

5.1 FPC Pin Assignment:

Terminal no.	Symbol	I/O	Function
1	GND	P	Ground
2	GND	P	Ground
3	VDD	P	Power Supply +3.3V
4	VDD	P	Power Supply +3.3V
5	VDD	P	Power Supply +3.3V
6	GND	P	Ground
7	Reset	I	Reset input signal. RESET = 1, normal operation RSET = 0, The controller is in reset state
8	STBYB	I	Standby mode. Normally pull high. STBYB = 0, timing controller, source driver will turn off, all output are High-Z. STBYB = 1, normal operation.
9	GND	P	Ground
10	GND	P	Ground
11	RIN0-	I	-LVDS differential data input(R0-R5,G0)
12	RIN0+	I	+LVDS differential data input(R0-R5,G0)
13	GND	P	Ground
14	GND	P	Ground
15	RIN1-	I	-LVDS differential data input(G1-G5,B0-B1)
16	RIN1+	I	+LVDS differential data input(G1-G5,B0-B1)
17	GND	P	Ground
18	GND	P	Ground
19	RIN2-	I	-LVDS differential data input(B2-B5,DE,VS,HS)
20	RIN2+	I	+LVDS differential data input(B2-B5,DE,VS,HS)
21	GND	P	Ground
22	GND	P	Ground
23	CLKIN-	I	-LVDS differential clock input
24	CLKIN+	I	+LVDS differential clock input
25	GND	P	Ground
26	GND	P	Ground
27	RIN3-	I	-LVDS differential data input(R6-R7,G6-G7,B6-B7)
28	RIN3+	I	+LVDS differential data input(R6-R7,G6-G7,B6-B7)
29	GND	P	Ground
30	GND	P	Ground
31	SEL68	I	Selection for either 6bit or 8bit LVDS input: SEL68 = ” High” or “NC”, accepts 8bit LVDS data input; SEL68 = ” Low”, accepts 6bit LVDS data input.
32	SCL_I2C	I	I2C Serial communication clock input. If not used, please float this pin.
33	GND	P	Ground
34	SDA_I2C	I/O	I2C Serial communication data input and output. If not used, please float this pin.
35	GND	P	Ground

36	CSB	I	SPI Serial communication enables. Normally pull high. If not used, please float this pin.
37	SCL	I	SPI Serial communication clock input. If not used, please float this pin.
38	GND	P	Ground
39	SDA	I/O	SPI Serial communication data input and output. If not used, please float this pin.
40	CMD_SEL	I	Command interface selection. CMD_SEL=”High”, I2C interface. CMD_SEL=”Low”, SPI interface. SPI/I2C command can’t receive at the same time.
41	A0	I	Serial interface (I2C) Compatible Device Address Bit 0 input. A0 = 1 : slave address=4F A0 = 0 : slave address=4E
42	GND	P	Ground
43	VPWM_EN	I	System PWM Logic Input Level
44	VLED_EN	I	LED enable input level
45	VLED_GND	P	LED Ground
46	VLED_GND	P	LED Ground
47	VLED_GND	P	LED Ground
48	VLED	P	LED Power Supply
49	VLED	P	LED Power Supply
50	VLED	P	LED Power Supply

5.2 Relationship Between Displayed Color and Input

	Display	MSB R7	R6	R5	R4	R3	R2	R1	LSB R0	MSB G7	G6	G5	G4	G3	G2	G1	LSB G0	MSB B7	B6	B5	B4	B3	B2	B1	LSB B0	Gray scale Level
Basic color	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	-
	Green	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	-
	Light Blue	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-
	Red	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-
	Purple	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	-
	Yellow	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	-
	White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-
Gray scale of Red	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L1
	↑	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L2
	↑					:							:								:					L3…L251
	↓	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L252
	Light	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L253
		H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L254
	Red	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	Red L255
Gray scale of Green	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L1
	↑	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L2
	↑					:							:								:					L3…L251
	↓	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L252
	Light	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L253
		L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L254
	Green	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	Green L255
Gray scale of Blue	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L1
	↑	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L2
	↑					:							:								:					L3…L251
	↓	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L252
	Light	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H	L253
		L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L254
	Blue	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	Blue L255
Gray scale of White & Black	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L0
	Dark	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L1
	↑	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L2
	↑					:							:								:					L3…L251
	↓	H	H	H	H	H	H	L	L	H	H	H	H	H	H	L	L	H	H	H	H	H	H	L	L	L252
	Light	H	H	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	L	H	L253
		H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	L	L254
	White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	White L255

6.0 ELECTRICAL CHARACTERISTICS

6.1 TFT LCD Module

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	Vcc	3.0	3.3	3.6	V	
Current of Vcc	Ivcc	-	270	320	mA	Red, Green or Blue pattern, Vcc=3.3V, @60Hz
Input signal voltage	ViH	0.8*Vcc	-	Vcc	V	
	ViL	0	-	0.2*Vcc	V	

Note: Measure the power supply voltage and current with the pins of the FPC connector (U5).

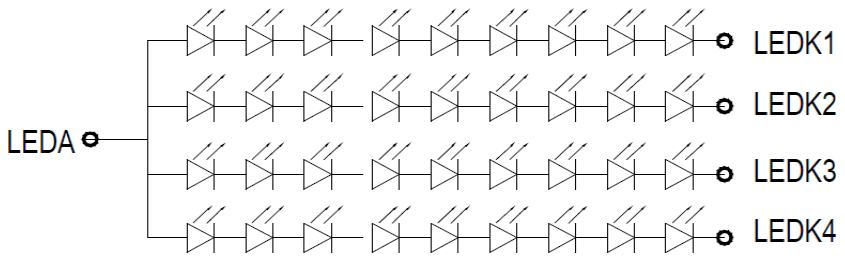
6.2 Backlight Unit

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED power Supply Voltage	VLED	11.5	12	12.5	V	
Current of VLED	I_{LED}	--	330	350	mA	
EN, PWM input voltage	ViH	1.9	--	VLED	V	BL On
	ViL	0	--	0.8	V	BL off
PWM Dimming Frequency	F_{PWM}	100	--	30K	Hz	
LED Life-Time	N/A	30,000	--	--	Hour	Ta=25℃ Note (2)

Note (1) Measure the power supply voltage and current with the pins of the FPC connector (U5).

Note (2) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ºC, and IF=120mA(30mA*4) indicated in the above table until the brightness becomes less than 50%.

Note (3) LED light Bar circuit

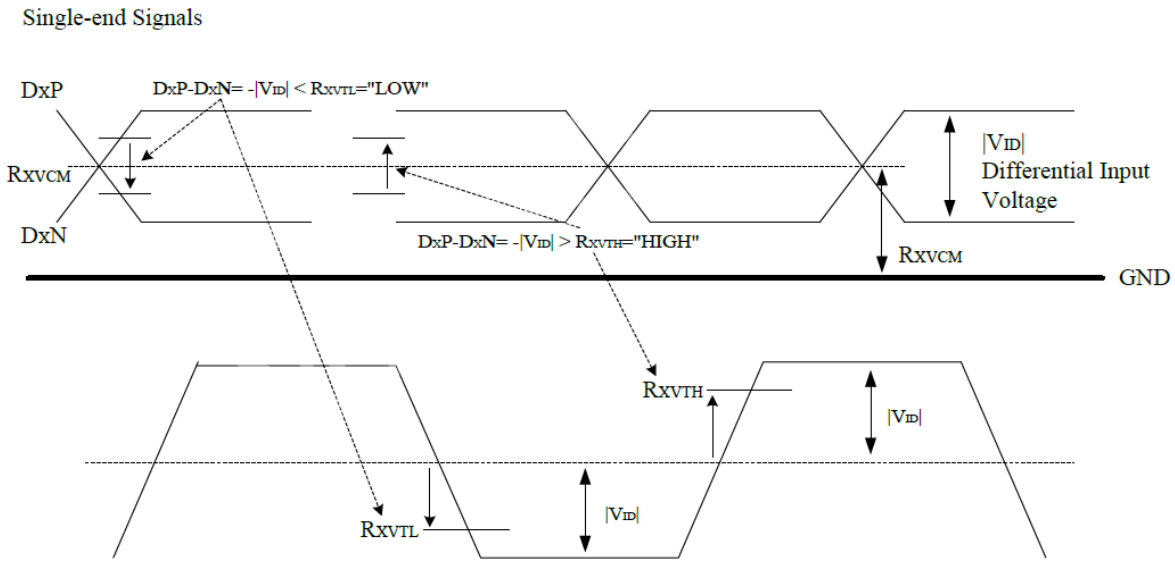


IF=30mA*4=120mA , VF=3.2V*9=28.8V

6.3 LVDS DC electrical characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Differential input high threshold voltage	R_{XVTH}	-	-	+0.1	V	R_{XVCM}=1.2V
Differential input low threshold voltage	R_{XVTL}	-0.1	-	-	V	R_{XVCM}=1.2V
Input voltage range (Singled-end)	R_{XVIN}	0.7	-	1.7	V	
Differential input common mode voltage	R_{XVCM}	1	1.2	1.4	V	$\|V_{ID}\|$=0.2V
Differential input Voltage	$\|V_{ID}\|$	0.2	-	0.6	V	

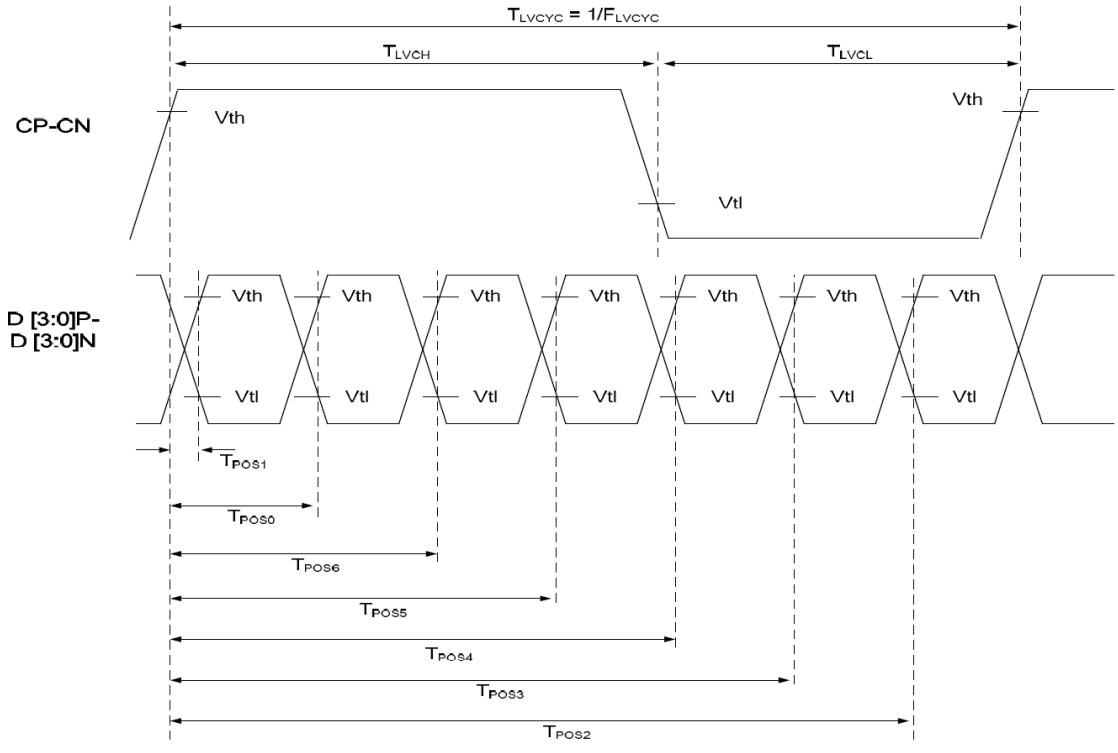
Note: The LVDS signal is measured at the land part of the terminating resistor (R1-R5: No Mount) on the FPC.

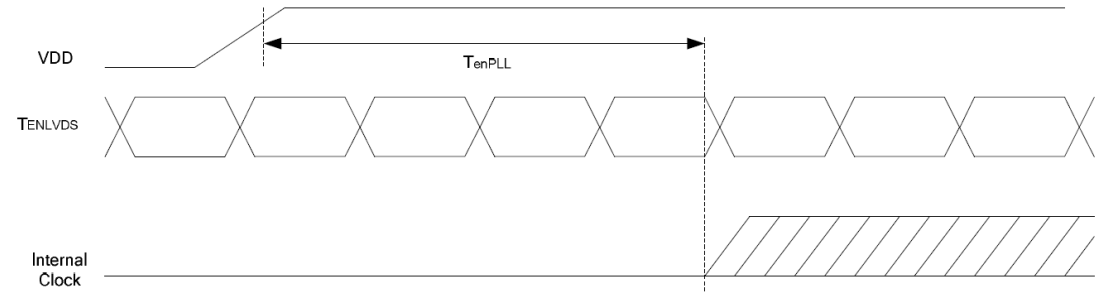


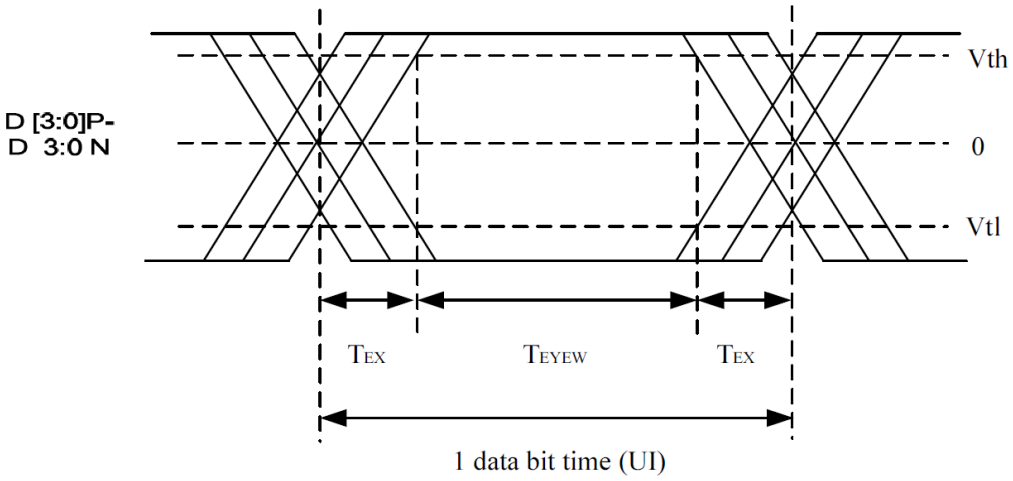
6.4 LVDS AC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	F_{LVCYC}	68.2		78.5	MHz
Clock period	T_{LVCYC}	12.74		14.66	ps
1 data bit time	UI	-	1/7	-	T_{LVCYC}
Clock high time	T_{LVCH}	3.9	4	4.1	UI
Clock low time	T_{LVCL}	2.9	3	3.1	UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6	-	-	UI
Input eye border	T_{EX}	-	-	0.2	UI
LVDS wake up time	TenPLL	-	-	150	us

Note: The LVDS signal is measured at the land part of the terminating resistor (R1-R5: No Mount) on the FPC.

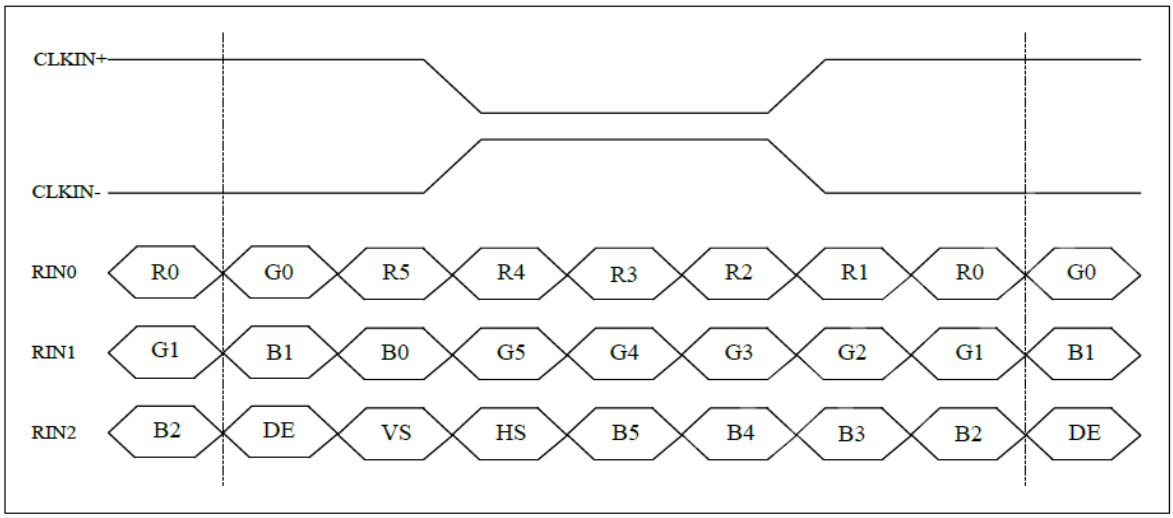




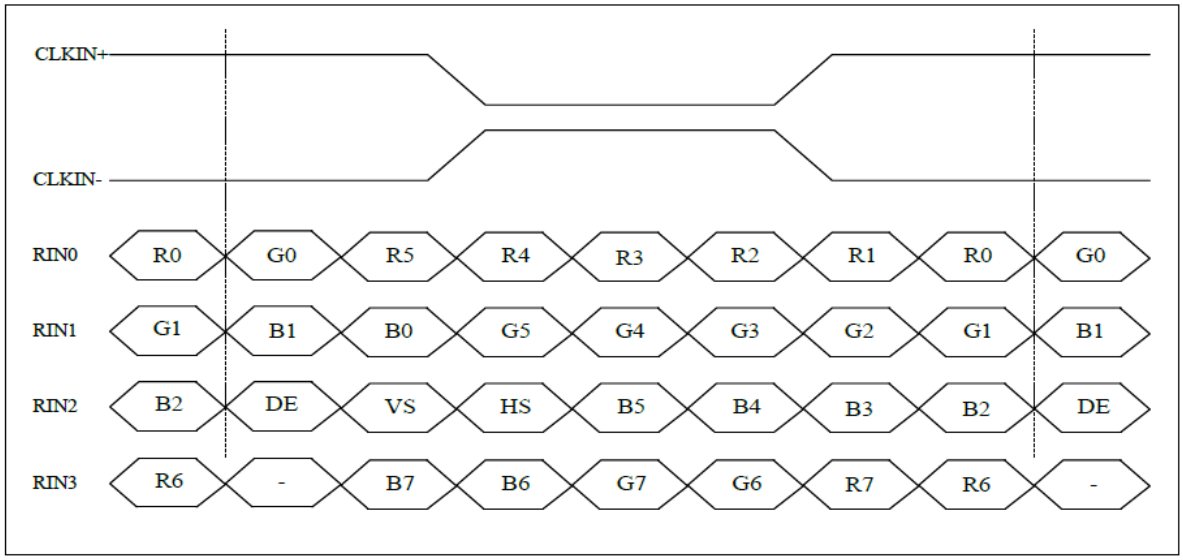


6.5 Data input format for LVDS

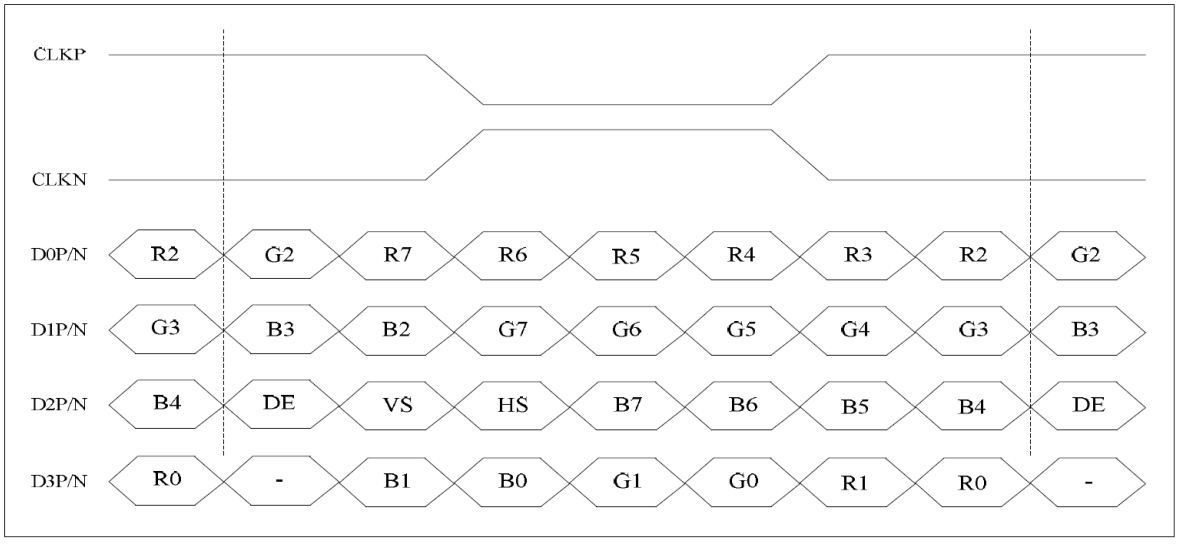
6.5.1 6-bit LVDS



6.5.2 8-bit LVDS (VESA format)



6.5.3 8-bit LVDS (JEIDA format)



6.6 Interface Timing

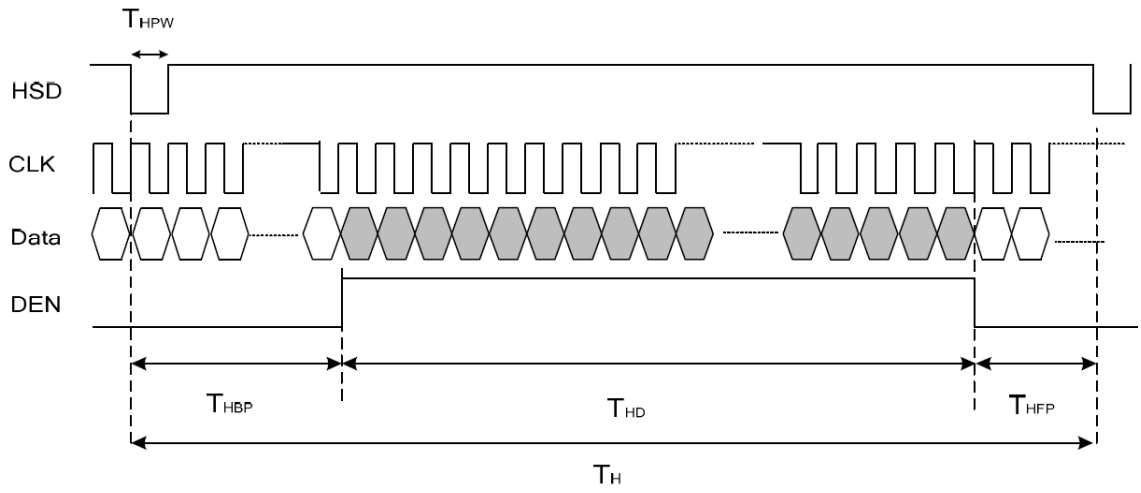
6.6.1 DE mode

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)	F_{DCLK}	68.2	72.4	78.5	MHz
Horizontal display area	T_{HD}		1280		DCLK
Horizontal total time	T_H	1380	1440	1500	DCLK
Horizontal blanking time	$T_{HBP}+T_{HFP}$	100	160	220	DCLK
Vertical display area	T_{VD}		800		H
Vertical total time	T_V	824	838	872	H
Vertical blanking time	$T_{VBP}+T_{VFP}$	24	38	72	H

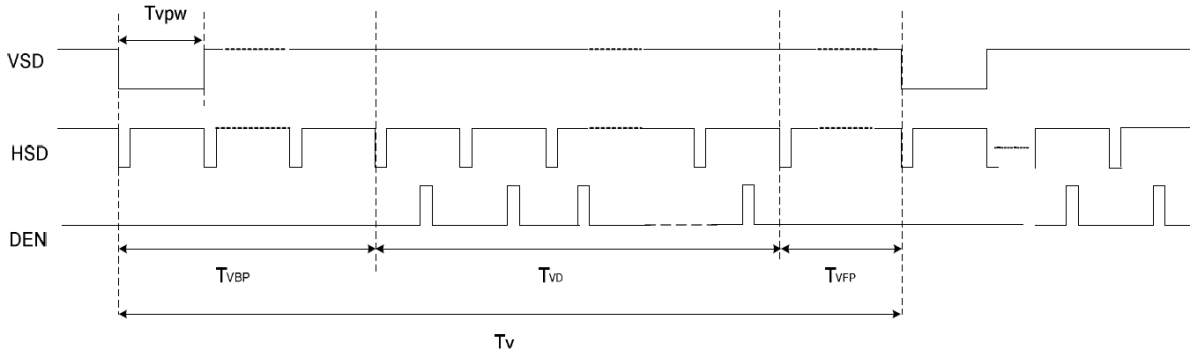
6.6.2 SYNC mode

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
DCLK frequency @Frame rate=60Hz (LVDS)		F_{DCLK}	68.2	72.4	78.5	MHz
Horizontal total time		T_H	1380	1440	1500	DCLK
Horizontal display area		T_{HD}		1280		DCLK
HSYNC pulse width	Min.	T_{HPW}		2		
	Typ.			-		
	Max.			40		
HSYNC back porch(with pulse width)		T_{HBP}	88	88	88	DCLK
HSYNC front porch		T_{HFP}	12	72	132	DCLK
Vertical total time		T_V	824	838	872	H
Vertical display area		T_{VD}		800		H
VSYNC pulse width	Min.	T_{VPW}		2		H
	Typ.			-		
	Max.			20		
VSYNC back porch(with pulse width)		T_{VBP}	23	23	23	H
VSYNC front porch		T_{VFP}	1	15	49	H

Horizontal timing

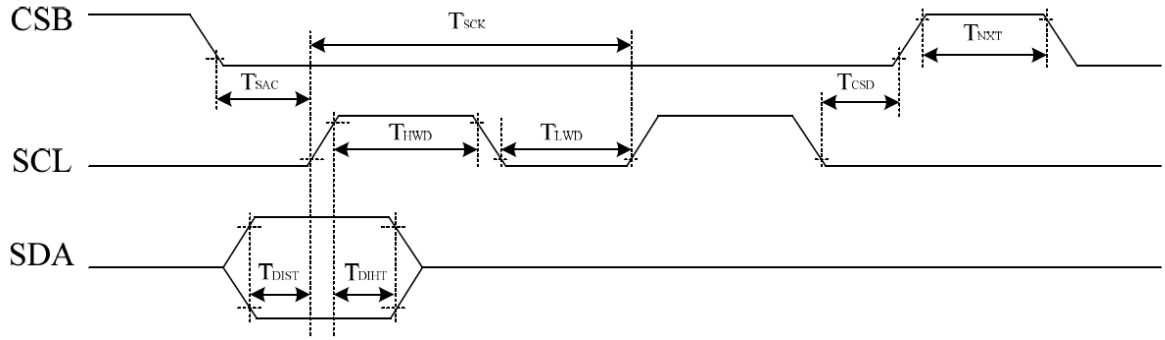


Vertical timing



6.7 Serial communication (SPI/I2C) format

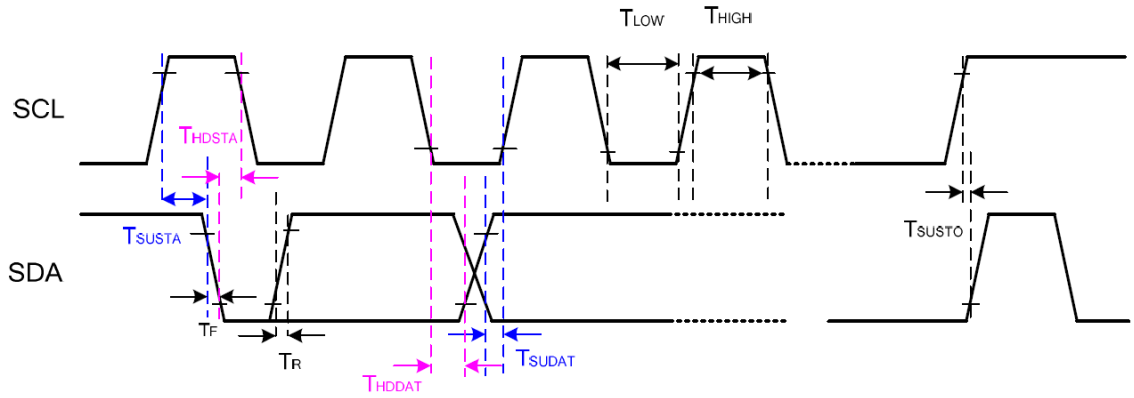
6.7.1 Timing Characteristics of SPI



Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
CSB assertion to first clock edge	T_{SAC}		120	-	-	ns
CSB de-assertion from last clock edge	T_{CSD}		120	-	-	ns
CSB next control enable	T_{NXT}		200	-	-	ns
SCL period time	T_{SCK}		200	-	-	ns
SCL high period time	T_{HWD}		100	-	-	ns
SCL low period time	T_{LWD}		100	-	-	ns
SDA input data setup time	T_{DIST}		50	-	-	ns
SDA input data hold time	T_{DIHT}		50	-	-	ns

Note: Measure the SPI signal with the pins of the FPC connector (U5).

6.7.2 Timing Characteristics of I2C



Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
SCL clock frequency	f_{SCL}		-	-	400	kHz
STOP setup time	T_{SUSTO}		0.60	-	-	uS
START setup time	T_{SUSTA}		0.60	-	-	uS
START hold time	T_{HDSTA}		0.60	-	-	uS
SCL clock pulse width low	T_{LOW}		1.20	-	-	uS
SCL clock pulse width high	T_{HIGH}		0.60	-	-	uS
Data hold time	T_{HDDAT}		0	-	-	uS
Data setup time	T_{SUDAT}		100	-	-	nS
IIC bus rise time	T_R		-	-	300	nS
IIC bus fall time	T_F		-	-	300	nS

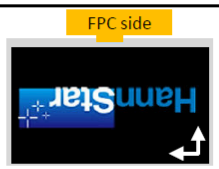
Note: Measure the I2C signal with the pins of the FPC connector (U5).

6.8 User Command

Address HEX	Parameter Index	D7	D6	D5	D4	D3	D2	D1	D0	Default
32	00	-	-	UPDN	DIR	-	-	-	-	32
35	00	-	-	-	LVFMT	LVBIT	MODE	-	-	24
4D	00	fiti_cmd[7:0]								AA

Description

UPDN and DIR: scanning direction control.

UPDN	DIR	Funtion	Display image
1	1	positive scan (Default)	
0	0	Reverse scan (Note)	

Note: if use Reverse scan, need to add the command R52h and R59h for GOA timing.
R52h={{13,13,13,13,13,13,12,13,10,11,04,05,06,07,08,09,0A,0B,03,0C,13,13}}
R59h={{13,13,13,13,13,13,12,13,10,11,04,05,06,07,08,09,0A,0B,03,0C,13,13}}

LVFMT: 8-bit input format select.

LVFMT	Funtion
0	VESA format (Default)
1	JEIDA mode

LVBIT: 6-bit / 8-bit input select.

SEL68=H

LVBIT	Funtion
0	8bits (Default)
1	6bits

SEL68=L

LVBIT	Funtion
0	6bits (Default)
1	8bits

MODE: DE/HV mode select.

MODE	Funtion
1	DE mode (Default)
0	HV mode (Note)

Note: if use HV mode, need to add the command R71h=C3h for GOA timing.

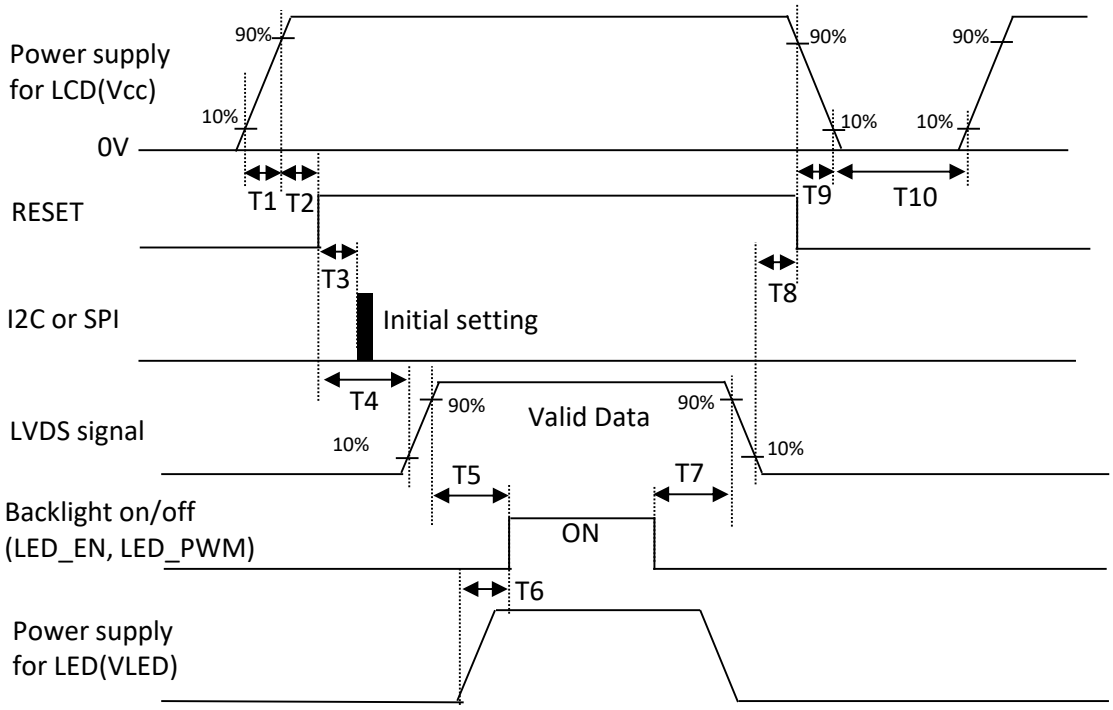
fiti_cmd[7:0]: the password "AA" to enter engineering mode.

6.9 Power Sequence

Power On Sequence: Vcc -> Reset -> LVDS signal -> B/L

Power Off Sequence: B/L-> LVDS signal -> Reset, VCC

STBYB can be directly connected with Vcc, or be turned on after Vcc is ready.



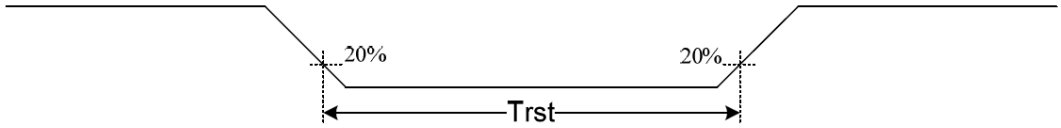
Item	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	1	-	-	ms
T3	50	-	-	ms
T4	0	-	-	ms
T5	200	-	-	ms
T6	10	-	-	ms
T7	200	-	-	ms
T8	0	-	-	ms
T9	0	-	10	ms
T10	500	-	-	ms

6.10 Timing requirements for RESET

When RESET of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set. However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max	
Reset low pulse width	Trst		20	-	-	μs



7.0 RELIABILTY TEST ITEMS

No.	Item	Conditions	Remark
1	High Temperature Storage	Ta=+80℃, 240hrs	
2	Low Temperature Storage	Ta=-30℃, 240hrs	
3	High Temperature Operation	Ta=+70℃, 240hrs	
4	Low Temperature Operation	Ta=-20℃, 240hrs	
5	High Temperature and High Humidity (operation)	Ta=+60ºC, 90%RH, 240hrs	
6	Thermal Cycling Test (non operation)	-20℃(30min)→+70℃(30min),100 cycles	
7	Vibration	Sine Wave: 1.5G, 5~500Hz, XYZ 30min/each direction Random: 1.04G, 5~500Hz, XYZ 30min/each direction	
8	Shock (Non OP)	Half-Sine, 100G, 6ms, ±XYZ, 3times	

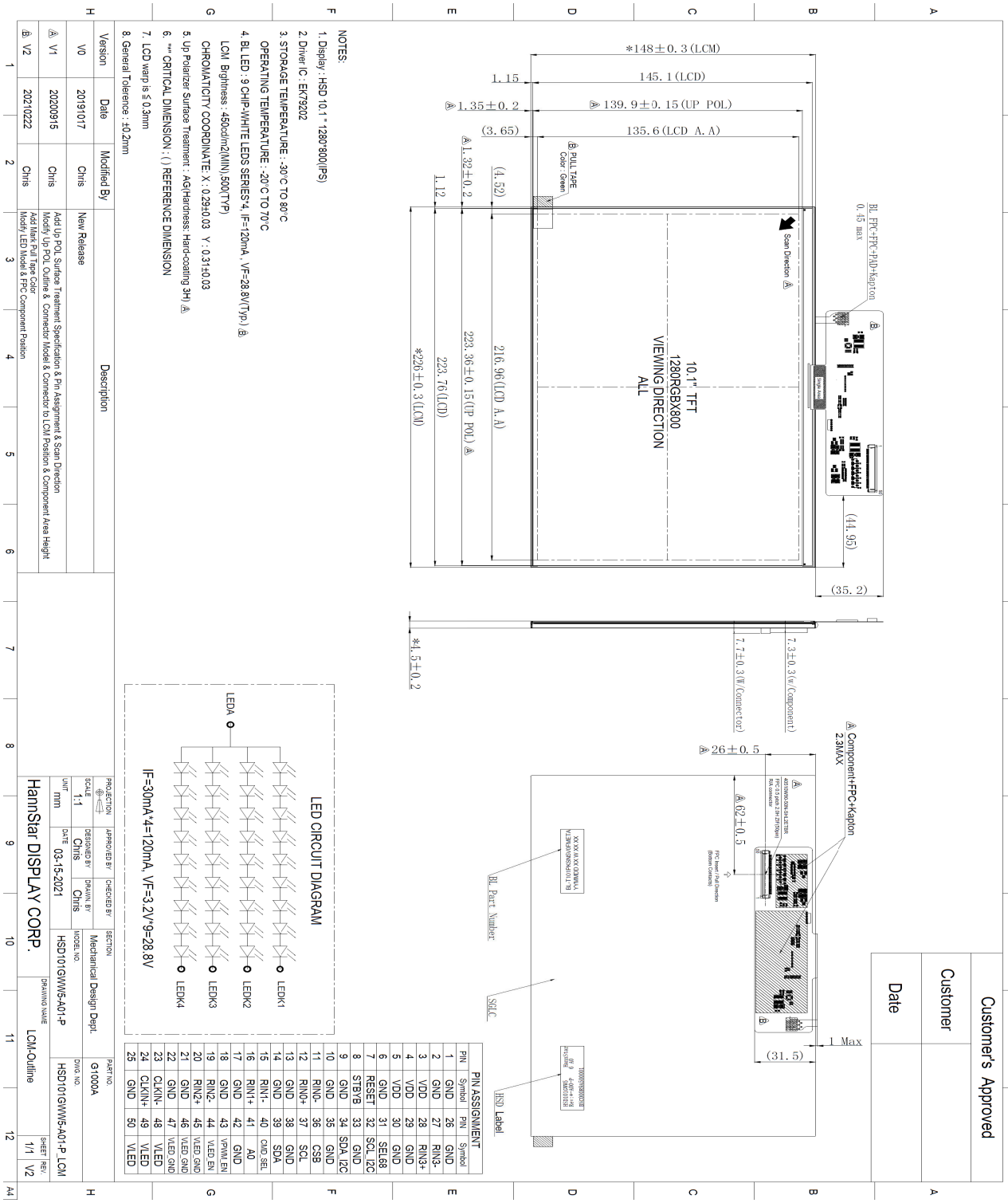
Note1: There is no display function NG issue occurred, all the cosmetic specification is judged before the reliability stress.

Note2: All of the function & cosmetic Judgment basis base on room temperature. (The tested module must have enough recovery time at least 2 hours at room temperature.)

Note3: The test condition definition panel's surface temperature.

8.0 OUTLINE DIMENSION

Unit : mm



NOTES:

1. Display : HSD 10.1" 1280*800(IPS)
2. Driver IC : EK79202
3. STORAGE TEMPERATURE : -30°C TO 80°C
   OPERATING TEMPERATURE : -20°C TO 70°C
4. BL LED : 9 CHIP-WHITE LEDS SERIES*4, IF=120mA , VF=28.8V(Typ.) Ⓑ
   LCM Brightness : 450cd/m2(MIN),500(TYP)
   CHROMATICITY COORDINATE: X : 0.29±0.03 Y : 0.31±0.03
5. Up Polarizer Surface Treatment : AG/Hardness: Hard-coating 3H) Ⓐ
6. "*" CRITICAL DIMENSION ; ( ) REFERENCE DIMENSION
7. LCD warp is ≤ 0.3mm
8. General Tolerence : ±0.2mm

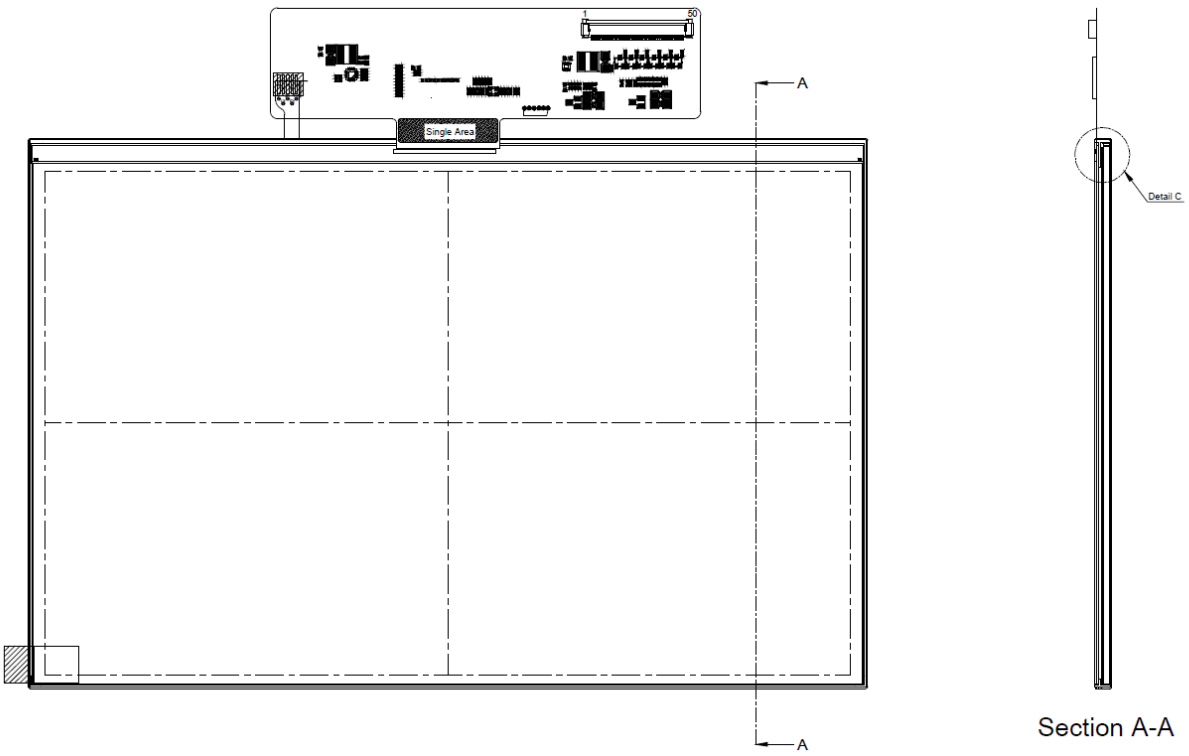
Version	Date	Modified By	Description
V0	20191017	Chris	New Release
Ⓐ V1	20200915	Chris	Add Up POL Surface Treatment Specification & Pin Assignment & Scan Direction Modify Up POL Outline & Connector Model & Connector to LCM Position & Component Area Height
Ⓑ V2	20210222	Chris	Add Main Pull Tape Color Modify LED Model & FPC Component Position

LED CIRCUIT DIAGRAM

IF=30mA*4=120mA, VF=3.2V*9=28.8V

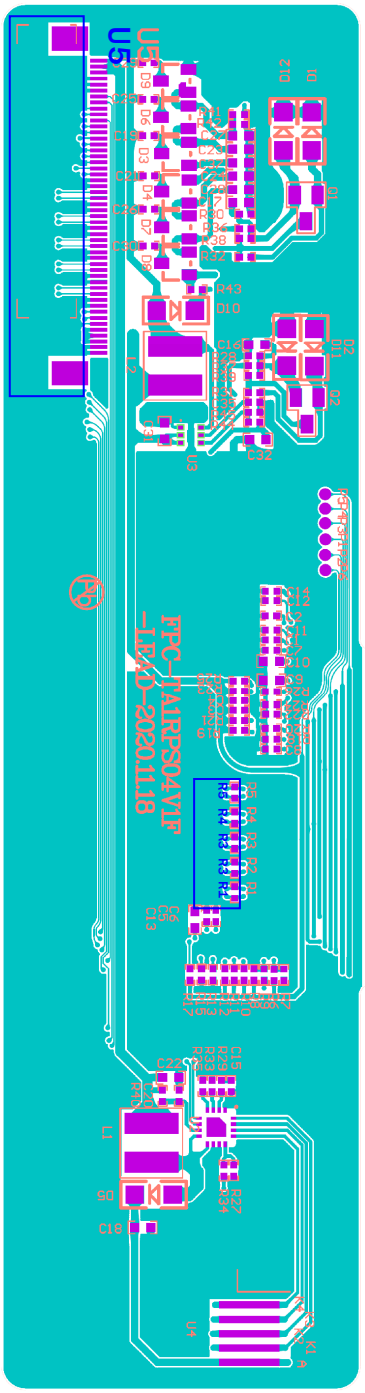
PIN	Symbol	PIN	Symbol
1	GND	26	GND
2	GND	27	RIN3-
3	VDD	28	RIN3+
4	VDD	29	GND
5	VDD	30	GND
6	GND	31	SELB8
7	RESET	32	SCL_I2C
8	STBYB	33	GND
9	GND	34	SDA_I2C
10	GND	35	GND
11	RIN0-	36	CSB
12	RIN0+	37	SCL
13	GND	38	GND
14	GND	39	SDA
15	RIN1-	40	CMD_SEL
16	RIN1+	41	A0
17	GND	42	GND
18	GND	43	VPWM_EN
19	RIN2-	44	VLED_GND
20	RIN2+	45	VLED_GND
21	GND	46	VLED_GND
22	GND	47	VLED_GND
23	CLKIN-	48	VLED
24	CLKIN+	49	VLED
25	GND	50	VLED

PROJECTION	APPROVED BY	CHECKED BY	SECTION
SCALE 1:1	DESIGNED BY Chris	DRAWN BY Chris	Mechanical Design Dept.
UNIT mm	DATE 03-15-2021	MODEL NO. HSD101GWW5-A01-P	PART NO. G1000A
HannStar DISPLAY CORP.		DRAWING NAME LCM-Outline	DWG NO. HSD101GWW5-A01-P_LCM
			SHEET 1/1 REV. V2

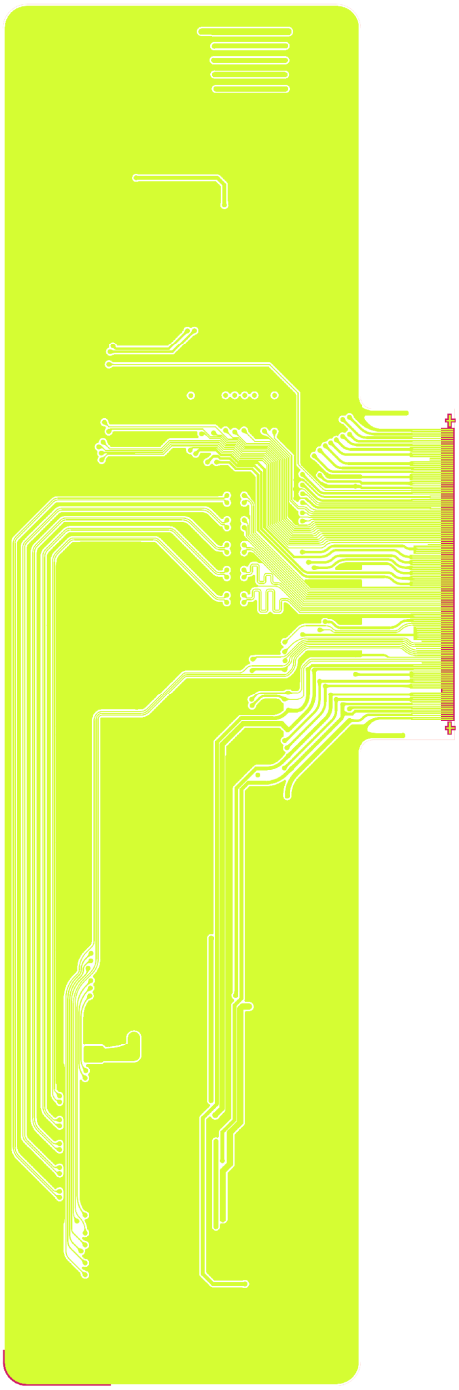


Section A-A

FPCA TOP view



FPCA Bottom view



Note:

- R1-R5: Measurement point of ELECTRICAL CHARACTERISTIC for LVDS
- U5: Measurement point of ELECTRICAL CHARACTERISTIC except LVDS

9.0 LOT MARK

9.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Code 1,2,3,4,5,6: HannStar internal flow control code.
Code 7: production location.
Code 8: production year.
Code 9: production month.
Code 10,11,12,13,14,15: serial number.

Note (1) Production Year: Code 8 is defined by the last number of the year, for example

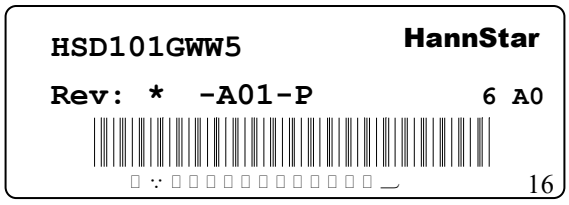
Year	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Mark	6	7	8	9	0	1	2	3	4	5	6

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

9.2 Detail of Lot Mark

(1) Below label is attached on the backside of the LCD module. See Section 8.0: Outline Dimension.
(2) The detail of Lot Mark is attached as below.
(3) This is subject to change without prior notice.

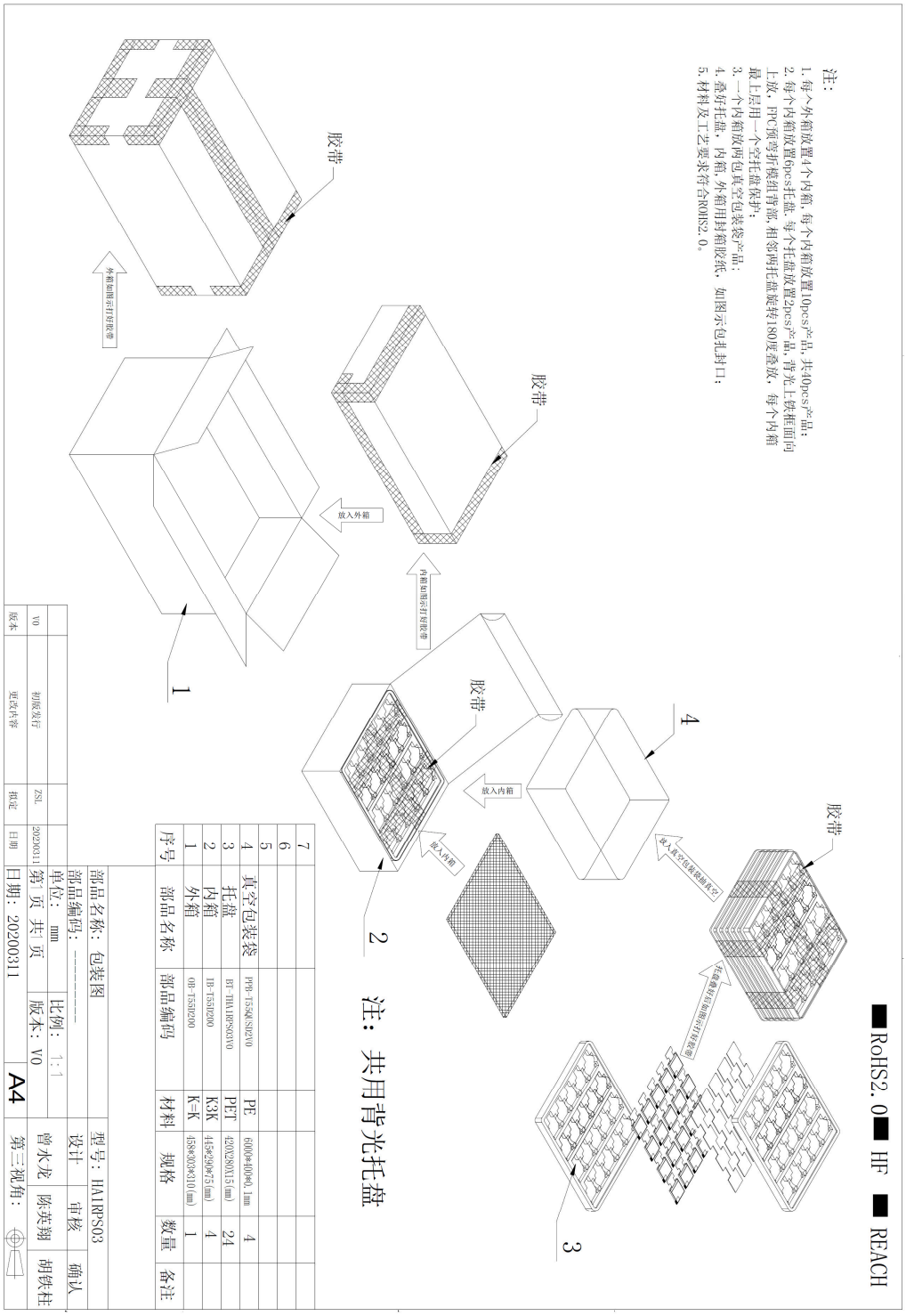


10.0 PACKAGE SPECIFICATION

10.1 Packing form

Packing name	Material	Specification	Quantity	Notice
Outer box	OB-T55D200 K=K	458*303*310(mm)	1	
Inner box	IB-T55D200 K3K	445*290*75(mm)	4	
Tray	BT-TA1RPS03V0	420*280*15(mm)	24	
vacuum bag	PPB-T55QUSD2V0	600*400*0.1(mm)	4	
Module	101GWW5-A01-P	-		

10.2 Packing Drawing



11.0 GENERAL PRECAUTION

11.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

11.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HannStar does not warrant the module, if customers disassemble or modify the module.

11.3 Breakage of LCD Panel

11.3.1. If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

11.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

11.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

11.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

11.4 Electric Shock

11.4.1. Disconnect power supply before handling LCD module.

11.4.2. Do not pull or fold the LED cable.

11.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

11.5 Absolute Maximum Ratings and Power Protection Circuit

11.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

11.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

11.5.3. It's recommended to employ protection circuit for power supply.

11.6 Operation

11.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

11.6.2 Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

11.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

11.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

11.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

11.7 Static Electricity

11.7.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

11.7.2 Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

11.8 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

11.9 Disposal

When disposing LCD module, obey the local environmental regulations.

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