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**TITLE : MV270QUM-NM0**

**Product Specification**

**Ver.O**

BEIJING BOE Display TECHNOLOGY CO. LTD

SPEC. NUMBER

S8-64-8A-301

PRODUCT GROUP

TFT-LCD

Ver.O

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PRODUCT GROUP

REV

ISSUE DATE

TFT- LCD PRODUCT

Ver.O

2020.11.10

### REVISION HISTORY

- ( ) Preliminary specification
- (●) Final specification

Revision No.	Page	Description of changes	Date	Prepared
Ver. O		Initial Release	2020.11.10	Wang Juan

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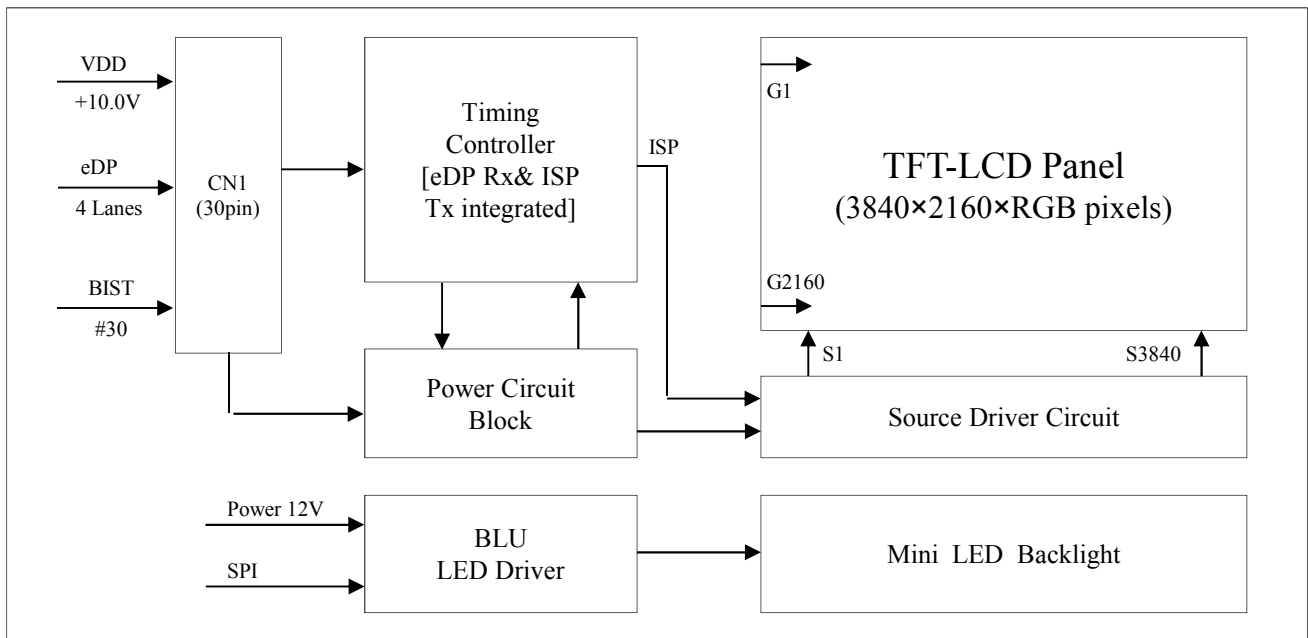
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### 1.0 GENERAL DESCRIPTION

#### 1.1 Introduction

MV270QUM-NM0 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 27 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 1.07B colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



#### 1.2 Features

- 4 lane eDP Interface with 5.4Gbps Link Rates
- High-speed response
- 10bit (8bit+A-FRC) color depth, display 1.07B colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only
- RoHS/Halogen Free
- Gamma Correction
- Reverse type
- Mini LED direct type back-light , Support HDR1000, Peak Luminance 1200nit Typ.
- Compatible with DCI-P3 Typ. 99.5%, Min. 98% & sRGB Typ. 100% @CIE1931

### 1.3 Application

- Desktop Type of PC & Workstation Use
- Slim-Size Display for Stand-alone Monitor
- Display Terminals for Control System
- Monitors for Process Controller

### 1.4 General Specification

The followings are general specifications at the model MV270QUM-NM0.

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	596.736(H) × 335.664(V)	mm	
Number of pixels	3840(H) × 2160(V)	pixels	
Pixel pitch	0.1554 (H) × 0.1554(V)	mm	
Pixel arrangement	RGB Vertical stripe		
Display colors	1.07 B(8bit+A-FRC)	colors	
Display mode	Normally Black		
Dimensional outline	608.8(H) × 354.1 (V) × 8.9 (D) Typ.	mm	Detail refer to drawing
Weight	3910 Typ.	g	
Bezel width (L/R/U/D)	6.032/6.032/5.968/12.468	mm	
Surface Treatment	Haze 25%, 3H		
Back-light	Mini LED direct back-light type with 1152 local dimming blocks		

### 2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

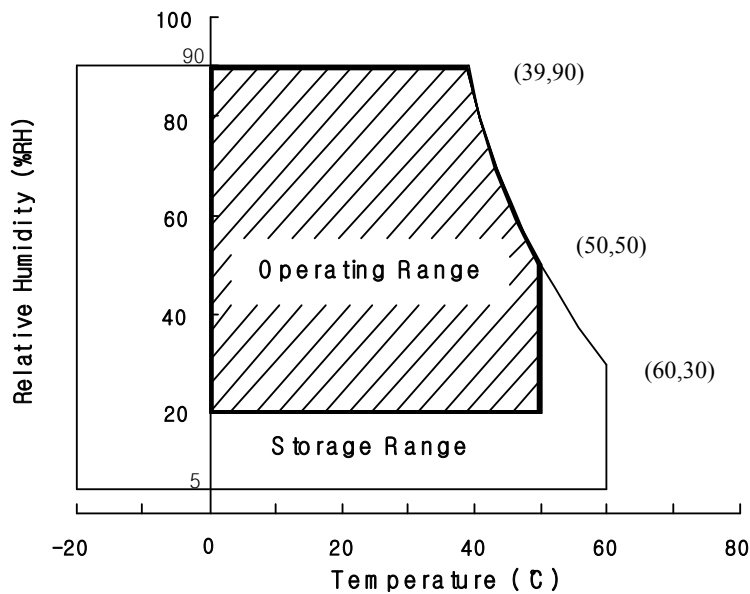
< Table 2. Absolute Maximum Ratings >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	$V_{DD}$	GND-0.3	12	V	Ta = 25 °C
Logic Supply Voltage	$V_{IN}$	VSS-0.3	$V_{DD}+0.3$	V	
Operating Temperature	$T_{OP}$	0	+50	°C	1)
Storage Temperature	$T_{ST}$	-20	+60	°C	1)

Note : 1) Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39 °C max. and no condensation of water.



### 3.0 ELECTRICAL SPECIFICATIONS

#### 3.1 Electrical Specifications

< Table 3. Electrical specifications >

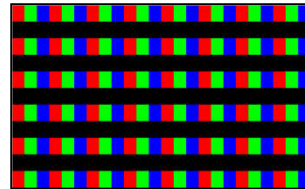
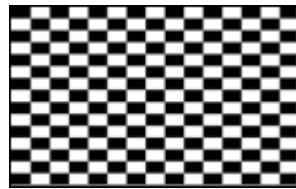
[Ta =25 ± 2 °C]

Parameter.		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V <sub>DD</sub>	9	10.0	12	V	Note1
Power Supply Current	I <sub>DD</sub>	-	600	900	mA	
In-Rush Current	I <sub>RUSH</sub>	-	2.0	3.0	A	Note 2
Permissible Input Ripple Voltage	V <sub>RF</sub>	-	-	400	mV	Note1,3
High Level Differential Input Threshold Voltage	V <sub>IH</sub>	-	-	+100	mV	
Low Level Differential Input Threshold Voltage	V <sub>IL</sub>	-100	-	-	mV	
Differential input voltage	V <sub>ID</sub>	100	-	600	mV	
Differential input common mode voltage	V <sub>cm</sub>	0	-	2		V <sub>IH</sub> =100mV, V <sub>IL</sub> =-100mV
Power Consumption	P <sub>D</sub>	-	6.0	9.0	W	
	P <sub>BL</sub>	-	73.2	80.52	W	Note 4
	P <sub>total</sub>	-	79.2	89.52	W	

Note : 1. The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=10.0V, Frame rate=60Hz

Test Pattern of power supply current



a) Typ : Mosaic Pattern

b) Max : 1 line Inversion

2. Duration of rush current is about 2 ms and rising time of VDD is 520 μs ± 20 %

3. Ripple Voltage should be covered by Input voltage Spec.

4. Calculated value for reference (Input pins\*VPIN × IPIN) excluding inverter loss.

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### 3.2 LED Driver Electrical Specifications

< Table 4. LED Driver Electrical Specifications >

Parameter		Min.	Typ.	Max.	Unit	Remarks
Input Voltage	VBL	10.8	12	13.5	V	
Input Current	IBL	/	6.1	/	A	Duty=50%
Input Current @Peak Luminance	IBL	/	12.2	/	A	Duty Max
In Rush current	Irush	/	/	12	A	
Power Consumption	PBL	/	73.2	80.52	W	Duty=50%
Power Consumption @Peak Luminance	PBL	/	146.4	161	W	Duty Max
SYS_BL_EN, SYS_LD_EN, SYS_VSYNC, SYS_CS, SYS_SCK, SYS_MISO, SYS_MOSI	High	2.4	3.3	3.6	V	
	Low	0	/	0.7	V	
SYS_VSYNC	Vsync	/	60	/	Hz	
LED Life-Time	-	30,000	-		Hrs	Note2

Note :

1. One BLU contains 1152 blocks, one block consists of 9 LEDs in serial.

$$IBL(Typ.) = Vled * 9 * Iled * Blocks * Duty / 4 / Efficiency / VBL$$

$$Vled = 3V; Iled = 16mA; Efficiency = 85\%;$$

2. The lifetime is determined as the time at which luminance of LED become 50% of the initial brightness or not normal lighting at Iled=16mA & Duty=50% on condition of continuous operating at 25 ± 2 °C.



## 4.0 OPTICAL SPECIFICATION

### 4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance  $\leq 1$  lux and temperature =  $25 \pm 2^\circ\text{C}$ ) with the equipment of Luminance meter system (Goniometer system and TOPCONE PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of  $\theta$  and  $\Phi$  equal to  $0^\circ$ . We refer to  $\theta_{\theta=0}$  ( $=\theta_3$ ) as the 3 o'clock direction (the "right"),  $\theta_{\theta=90}$  ( $=\theta_{12}$ ) as the 12 o'clock direction ("upward"),  $\theta_{\theta=180}$  ( $=\theta_9$ ) as the 9 o'clock direction ("left") and  $\theta_{\theta=270}$  ( $=\theta_6$ ) as the 6 o'clock direction ("bottom"). While scanning  $\theta$  and/or  $\Phi$ , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 5.0V +/-10% at  $25^\circ\text{C}$ . Optimum viewing angle direction is 6 o'clock.

### 4.2 Optical Specifications

[VDD = 10.0V, Frame rate = 60Hz, Clock = 74.25MHz,  $V_{BL} = 12\text{V}$ ,  $I_{BL} = 6.1\text{ A}$ , duty=50%,  $T_a = 25 \pm 2^\circ\text{C}$ ]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	$\Theta_3$	CR > 10	85	89	-	Deg.	Note 1
		$\Theta_9$		85	89	-	Deg.	
	Vertical	$\Theta_{12}$		85	89	-	Deg.	
		$\Theta_6$		85	89	-	Deg.	
Static Luminance Contrast ratio		CR	$\Theta = 0^\circ$ (Center) Normal Viewing Angle	900	1100			Note 2
Dynamic Luminance Contrast ratio		CR		-	1000,000	-		Note 3
Luminance of White		$Y_w$		600	720	-	cd/m <sup>2</sup>	Note 4
White luminance uniformity		$\Delta Y$		85	90	-	%	Note 5
Reproduction of color	White	$W_x$		0.283	0.313	0.343	-	Note 6
		$W_y$	0.299	0.329	0.359	-		
	Red	$R_x$	0.644	0.674	0.704	-		
		$R_y$	0.293	0.323	0.353	-		
	Green	$G_x$	0.230	0.260	0.290	-		
		$G_y$	0.668	0.698	0.728	-		
	Blue	$B_x$	0.125	0.155	0.185	-		
		$B_y$	0.023	0.053	0.083	-		
Response Time	GTG	$T_g$		14	20	ms	Note 7	

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**Note :**

- Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
- Static Contrast measurements shall be made at viewing angle of  $\theta = 0^\circ$  and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

- Dynamic Contrast measurements shall be made at viewing angle of  $\theta = 0^\circ$  and at the center of the LCD surface. The white luminance shall be measured with 10% center patch set to white at black state. The dark luminance shall be measured with 2.5% screen area of each corner set to white at black state. (See FIGURE 2 shown in Appendix) Dyanmic CR is defined as follows. Wheres DCR is measured matching with BOE algorithm..

$$DCR = \frac{\text{Luminance when displaying 10\% center white patch at black state}}{\text{Luminance when displaying a black raster with 2.5\% corner area set to white}}$$

- Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 1 for a total of the measurements per display.
- The White luminance uniformity on LCD surface is then expressed as :  
 $\Delta Y = (\text{Minimum Luminance of 9points} / \text{Maximum Luminance of 9points}) * 100$  (See FIGURE 3 shown in Appendix).
- The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
- Response time Tg is the average time required for display transition by switching the input signal as below table and is based on F rame rate fV =60Hz to optimize.  
Each time in below t able is defined as appendix Figure4 and shall be measured by switching the input signal for “any level of gray(bright)”and “any level of gray(dark)”

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### 5.0 INTERFACE CONNECTION.

#### 5.1 LED Driver Board

- Input connector(CN1& CN2 ) : CI0114M1HR0-NH manufactured by Cvilux or equivalent.
- SPI connector(U3): CI4410M1HR0-NH manufactured by Cvilux or equivalent.

< Table 6. Input Connector Pin Configuration CN1&CN2>

**CN1&CN2**

Pin No	Symbol	Description
1	VCC	Power supply 12V
2	VCC	Power supply 12V
3	VCC	Power supply 12V
4	VCC	Power supply 12V
5	VCC	Power supply 12V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	NC	NC
12	SYS_BL_EN	Back Light_EN
13	SYS_BL_PWM	BL Global PWM dimming
14	NC	NC

**U3**

Pin No	Symbol	Description
1	SYS_LD_EN	Local Dimming_EN
2	SYS_BL_EN	Back Light_EN
3	SYS_CS	SPI CS
4	SYS_SCK	SPI Clock
5	SYS_MISO	Driver output
6	SYS_MOSI	Driver input
7	SYS_VSYNC	VSYNC
8	NC	NC
9	NC	NC
10	GND	Ground

## 5.0 INTERFACE CONNECTION.

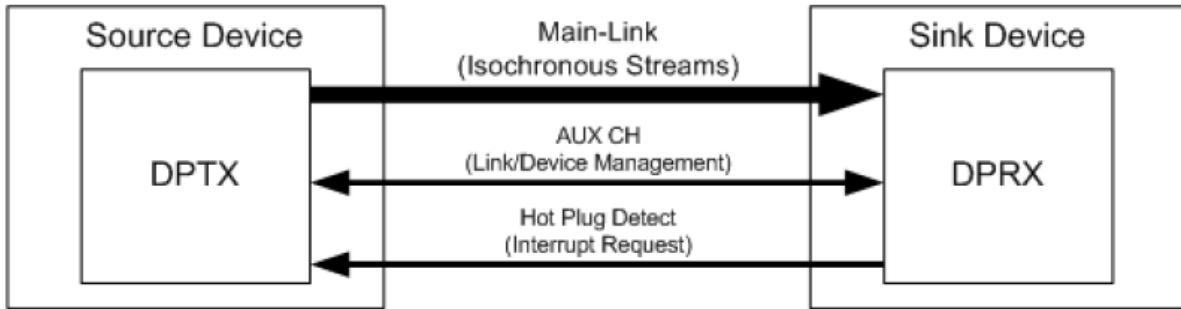
### 5.2 Electrical Interface Connection

- CN1 Module Side Connector : STM MSAK24025P30 or Equivalent

Pin No	Symbol	Function	Remark
30	VDD	Power Supply (10.0V)	
29	VDD	Power Supply (10.0V)	
28	VDD	Power Supply (10.0V)	
27	VDD	Power Supply (10.0V)	
26	VDD	Power Supply (10.0V)	
25	GND	Ground	
24	GND	Ground	
23	NC	No connection	
22	NC	No connection	
21	GND	Ground	
20	HPD	Hot Plug Detection Signal	
19	GND	Ground	
18	DAUXN	Negative Signal for Auxiliary Chanel	
17	DAUXP	Positive Signal for Auxiliary Chanel	
16	GND	Ground	
15	DRX0P	Positive Signal For eDP Lane0	
14	DRX0N	Negative Signal For eDP Lane0	
13	GND	Ground	
12	DRX1P	Positive Signal For eDP Lane1	
11	DRX1N	Negative Signal For eDP Lane1	
10	GND	Ground	
9	DRX2P	Positive Signal For eDP Lane2	
8	DRX2N	Negative Signal For eDP Lane2	
7	GND	Ground	
6	DRX3P	Positive Signal For eDP Lane3	
5	DRX3N	Negative Signal For eDP Lane3	
4	GND	Ground	
3	GND	Ground	
2	NC	No connection	
1	BIST	BIST Function	BIST

### 5.3 eDP Interface

- eDP Data Transport Channels



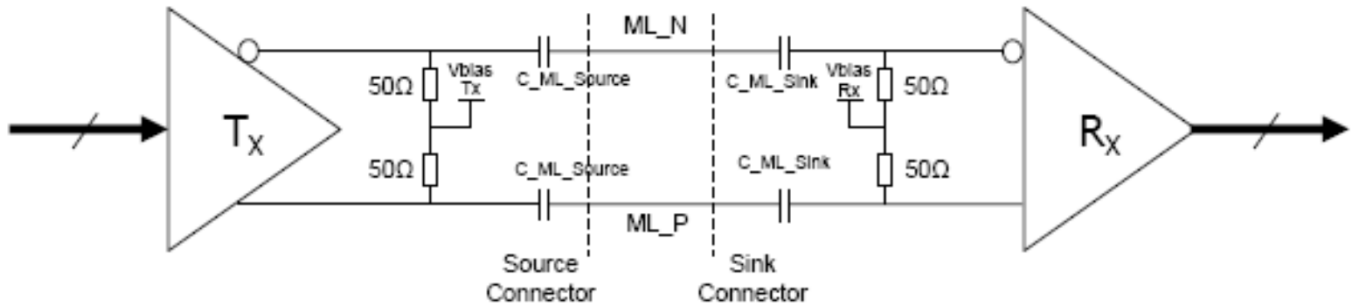
#### eDP Data Transport Channels

- The TCON supports 4 lane 8 bit input eDP architecture. The data mapping is shown as below:

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

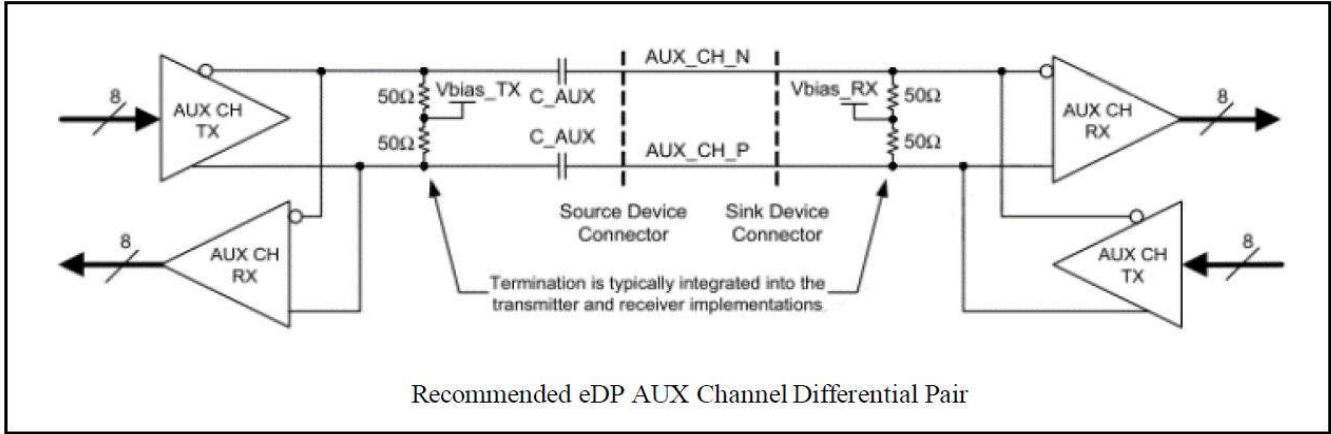
#### 8bit RGB to a 4-Lane Main-Link Mapping

### 5.3.1 eDP Main Link Signal



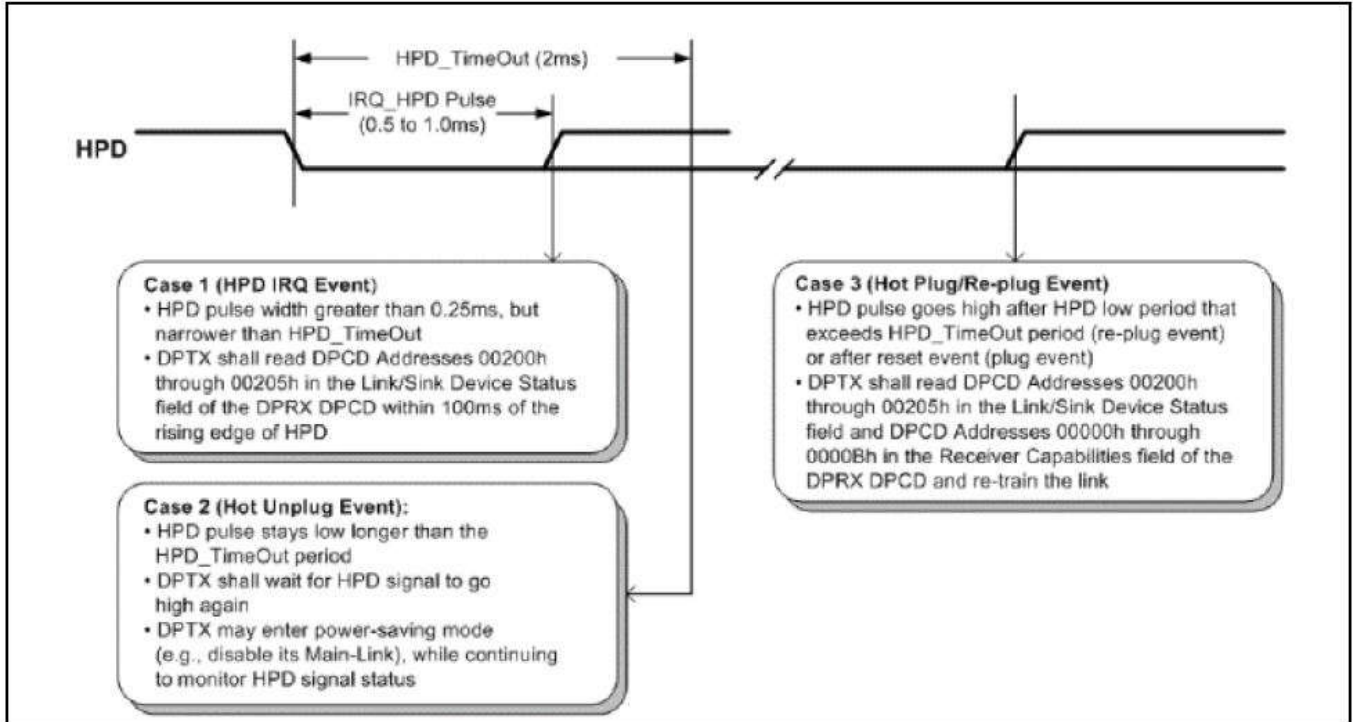
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate2(5.4Gbps/lane)	UI-HBR2	-	185	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30	-	33	kHz	TBD
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	-	-	1.38	V	
EYE width at Sink side connector	$T_{RX-EYE-CONN}$	0.25	-	-	UI	TBD
Lane-to-Lane skew	$L_{RX-SKEWINTER\_PAIR}$	-	-	1250	-	TBD
Lane intra-pair skew	$L_{RX-SKEWINTER\_PAIR}$	-	-	50	ps	
AC Coupling Capacitor	$C_{SOURCE\_ML}$	75	-	265	nF	Source side

### 5.3.2 eDP AUX Channel Signal



Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	μs	
AUX Jitter at Tx IC Package Pins	$T_{jitter}$	-	-	0.04	UI	
AUX Jitter at Rx IC Package Pins		-	-	0.05	UI	
AUX Peak-to-peak voltage at Connector Pins of Receiving	$V_{AUX-DIFFP-P}$	0.27	-	1.36	V	
AUX Peak-to-peak voltage at Connector Pins of Transmitting		0.29	-	1.38	V	
AUX DC common mode voltage	$V_{AUX-CM_RX}$	0	-	2.0	V	
	$V_{AUX-CM_TX}$	0	-	2.0	V	
AUX AC Coupling Capacitor	$C_{SOURCE\_ML}$	75	-	200	nF	

### 5.3.3 eDP HPD Signal



Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
HOT Plug Detection Threshold		2.0	-	-	V	Source side Detecting
HOT Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut	-	2.0	-	-	ms	HPD Unplug Event



**6.0 SIGNAL TIMING SPECIFICATION**

6.1 The MV270QUM-NM0 is operated by the DE only.

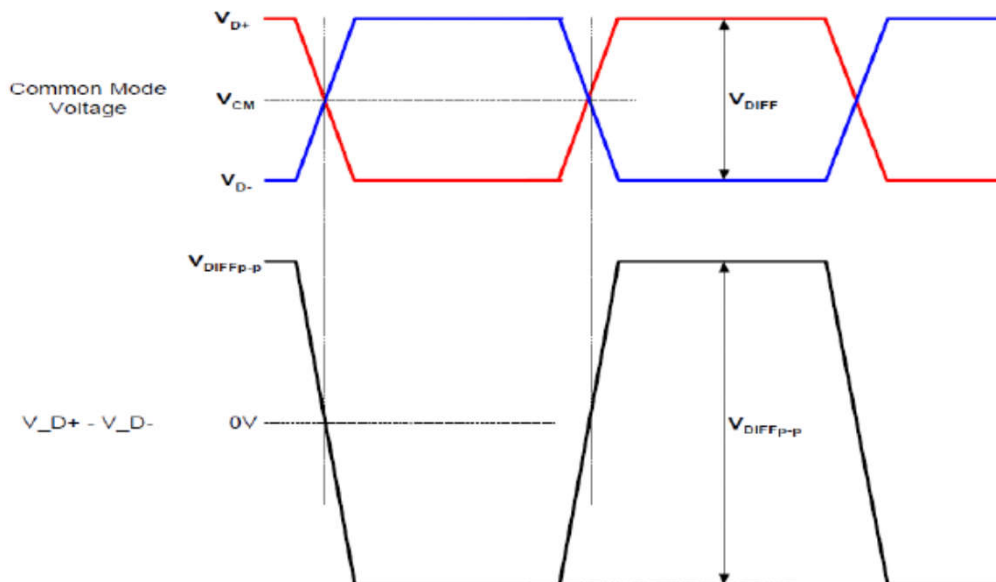
Item		Symbol	Min	Typ	Max	Unit	Note
DCLK	Period	tCLK	1.8	1.9	2.2	ns	
	Frequency	fCLK	444	533	551	MHz	
Hsync	Period	tHP	3950	4000	4088	tCLK	
	Width-Active	tWH	18	28	36		
Vsync	Period	tVP	2213	2222	2290	tHP	
	Frequency	fv	50	60	62	HZ	
	Width-Active	tWV	6	8	12	tHP	
Data Eenlabe	Horizontal valld	tHV	3840	3840	3840	tCLK	
	Horizontal Back P orch	tHBP	32	54	112		
	Horizontal Front P orch	tHFP	60	78	100		
	Horizontal Blank	-	110	160	248		tWH+tHBP +tHFP
	Vertial valld	tVV	2160	2160	2160	tHP	
	Vertial Back Porch	tVBP	5	7	18		
	Vertial Front Porch	tVFP	42	47	100		
	Vertial Blank	-	53	62	130		tWV+tVBP +tVFP

### 6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 7.

<Table 7. eDP Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock	ssc	0	-	0.5	%	
Differential peak-to-peak input voltage at package pins	VRX-DIFFp-p	120	-	-	mV	
Rx input DC common mode voltage	VRX_DC_CM	-	GND	-	V	
Differential termination resistance	RRX-DIFF	80	-	100	$\Omega$	
Single-ended termination resistance	RRX-SE	40	-	60	$\Omega$	
Rx short circuit current limit	IRX_SHORT	-	-	20	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	LRX_SKEW_ INTRA_PAIR	-	-	150	ps	

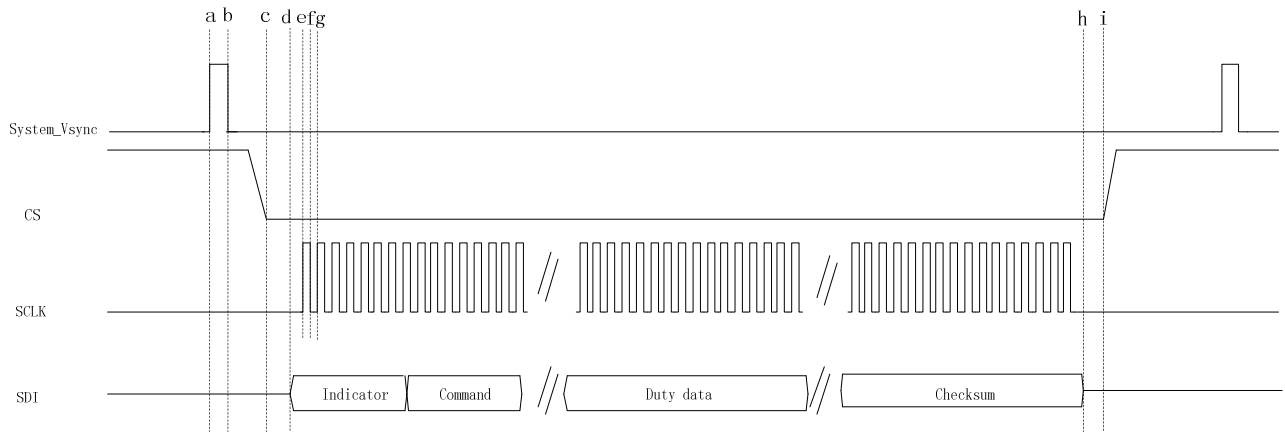


\*  $V_{diff} = (RXZ+) - (RXZ-), \dots, (RXCLK+) - (RXCLK-)$

### 6.3 LED Driver Interface SPI Parameter

The specification of the LED Driver SPI parameter is shown in Table 8.

<Table 8. LED Driver SPI parameter Specification>



Parameter	Value			Units	Note
	Min	Typ	Max		
Tab	20	--	--	us	
Tbc	--	100	--	us	
Tcd	--	100	--	us	
Tef	0.0625	--	0.125	us	
Teg	0.125	--	0.25	us	

**Note:** SCLK Rising edge validity

### 6.3 LED Driver Interface SPI Parameter

**SPI Data Format:**

Indicator	Command	Data1	Data2	...	DataN	Checksum
-----------	---------	-------	-------	-----	-------	----------

**Definition:**

**1. Indicator (1Byte)**

0xAA : 8bit

**2. Command (1Byte)**

Bit0 : Local dimming enable ( "1" : Enable ; "0" : Disable )

Bit1 : Light Water select ( "1" : Enable ; "0" : Disable )

Bit2 : Reserved

Bit3 : Reserved

Bit4 : Reserved

Bit5 : Reserved

Bit6 : Reserved

Bit7 : Frame frequency select ( "1" : 60Hz ; "0" : 120Hz )

**3. Data1~DataN: 2Byte per data,**

12bits local dimming gray value

**4. Checksum: 1Byte 8bits XOR**

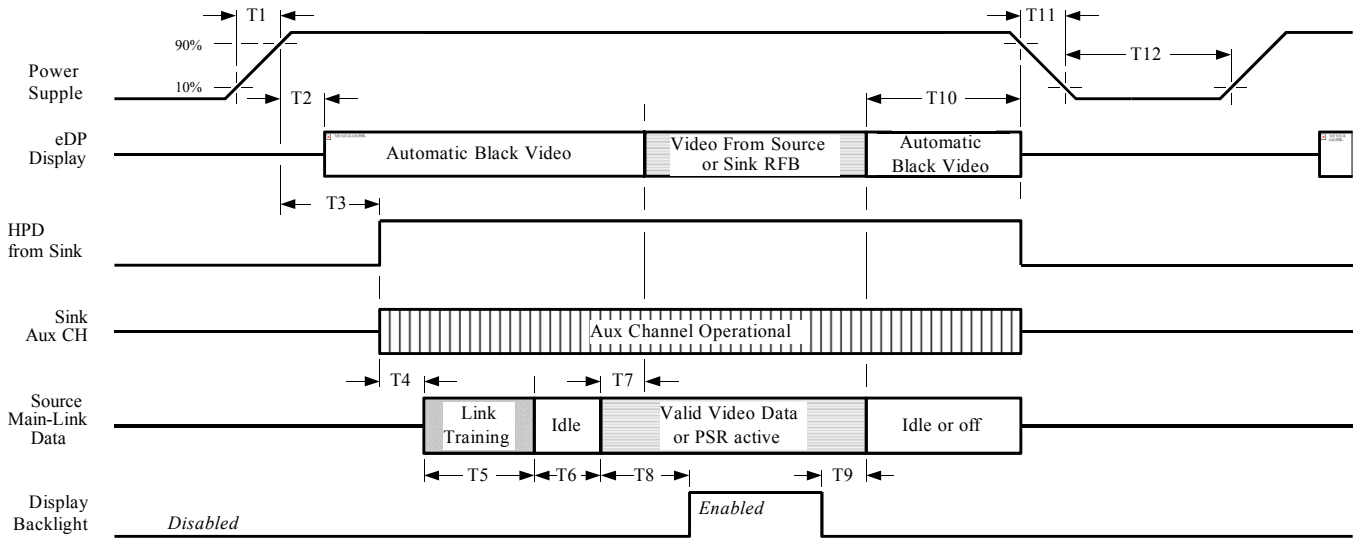
ID^Command^Data1^Data2^...DataN(^:Exclusive OR)



### 8.0 POWER SEQUENCE

#### 8.1 Panel Power sequence

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below



Timing Parameter	Description	Required By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	
T2	Delay from Power Supply to automatic Black Video generation	Sink	0ms	200ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source
T3	Delay from Power Supply to HPD high	Sink	0ms	200ms	Sink AUX Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for the Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on the Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle Pattern. Max allows for Source frame synchronization.

## 8.0 POWER SEQUENCE

### 8.1 Panel Power sequence

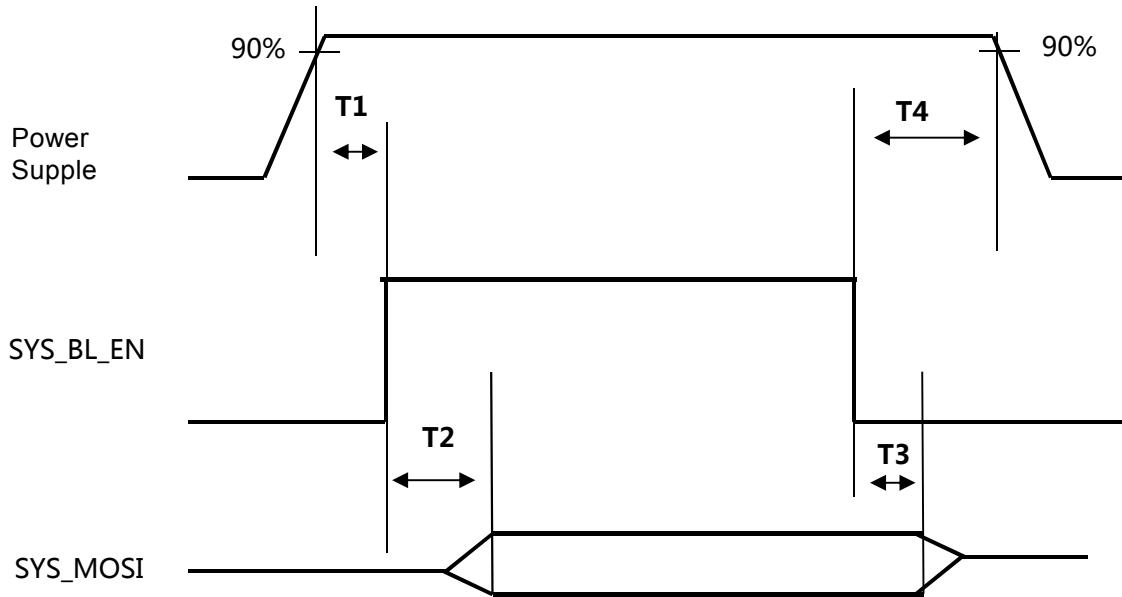
T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max value allows for the Sink to validate video data and timing. At the end of T7, the Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and the Sink will no longer generate automatic Black Video.
T8	Delay from valid video data from Source to backlight enable	Source	-	-	The Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	The Source must assure backlight is no longer illuminated. At the end of T9, the Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and the Sink will automatically display Black Video.
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T11	Power rail fall time, 90% to 10%	Source	-	-	T11 decrease smoothly, there is none re-bouncing voltage
T12	Power off time	Source	500ms	-	

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.

## 8.0 POWER SEQUENCE

### 8.2 LED Driver Power sequence



Parameter	Values			Units
	Min	Typ	Max	
T1	200	-	-	ms
T2	200	-	-	ms
T3	20	-	-	ms
T4	20	-	-	ms



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## 9.0 MECHANICAL CHARACTERISTICS

### 9.1 Dimensional Requirements

FIGURE 6 (located in Appendix) shows mechanical outlines for the model MV270QUM-NM0. Other parameters are shown in Table 9.

<Table 9. Dimensional Parameters>

Parameter	Specification	Unit
Dimensional outline	608.8(H) × 354.1 (V) × 8.9 (D) Typ.	mm
Weight	3910 Typ.	gram
Active area	596.736(H) × 335.664 (V)	mm
Pixel pitch	0.1554 (H) × 0.1554(V)	mm
Number of pixels	3840(H) × 2160 (V) (1 pixel = R + G + B dots)	pixels
Back-light	Direct type, Mini LED, 1152 blocks	

### 9.2 Mounting

See FIGURE 7. (shown in Appendix)

### 9.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an anti-glare coating to minimize reflection and a coating to reduce scratching.

### 9.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

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### 10.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

<Table 10. Reliability Test Parameters >

No	Test Items	Conditions	
1	High temperature storage test	Ta = 60 °C, 240 hrs	
2	Low temperature storage test	Ta = -20 °C, 240 hrs	
3	High temperature & high humidity operation test	Ta = 50 °C, 80%RH, 240hrs	
4	High temperature operation test	Ta = 50 °C, 240hrs	
5	Low temperature operation test	Ta = 0°C, 240hrs	
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle	
7	Vibration test (non-operating)	Frequency	Random, 10 ~ 300 Hz, 30 min/Axis
		Gravity\AMP	1.5 Grms
		Period	X, Y, Z 30 min
8	Shock test (non-operating)	Gravity	50G
		Pulse width	11msec, sine wave
		Direction	± X, ± Y, ± Z Once for each
9	Electro-static discharge test	Air : 150 pF, 330Ω, 15 KV Contact : 150 pF, 330Ω, 8 KV	

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## 11.0 HANDLING & CAUTIONS

### (1) Cautions when taking out the module

- Pick the pouch only, when taking out module from a shipping package.

### (2) Cautions for handling the module

- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

### (3) Cautions for the operation

- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.
- Ultra-violet ray filter is necessary for outdoor operation
- If the product will be used in extreme conditions such as high temperature, humidity, display patterns, operation time, etc., it is strongly recommended to contact BOE for application engineering device. Otherwise, the reliability and function of the module may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stocks, markets, and controlling systems.

### (4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

### (5) Cautions for the module characteristics

- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

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## 11.0 HANDLING & CAUTIONS

### (6) Other cautions

- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.
- When this reverse model is used as a forward-type model (PCB on top side), BOE can not guarantee any defects of LCM.
- If LCD module containing system is out of BOE 's operating or storing condition, BOE can not guarantee LCD module operating properly.

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## 12.0 PRODUCT SERIAL NUMBER

MV270QUM-NM0 B4



XXXX XXXXXXXXXXXXXXXXXXXX

P/N: XXXXXXXXXXXX FRU: XXXXXXXXXXXX

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XXXXXXXXXXXXXXXXXXXXXXXXXXXX





MADE IN CHINA

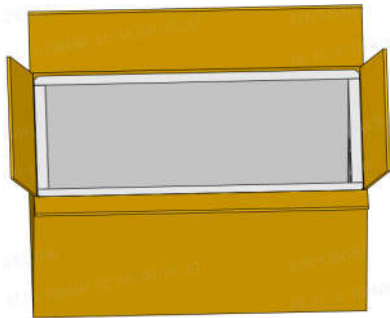
Digit	1		2		3		4		5		6				7				
Code	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Des.	1. Control Number 2. Rank/Grade 3. Line Classification 4. Year(2001:01, 2002:02, ...) 5. Month(1, 2, 3, ..., 9, X, Y, Z) 6. Internal Use 7. Serial Number																		

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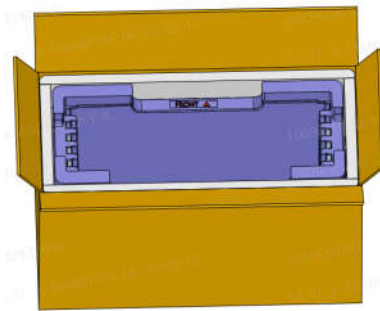
## 13.0 Packing

### 13.1 Packing Order

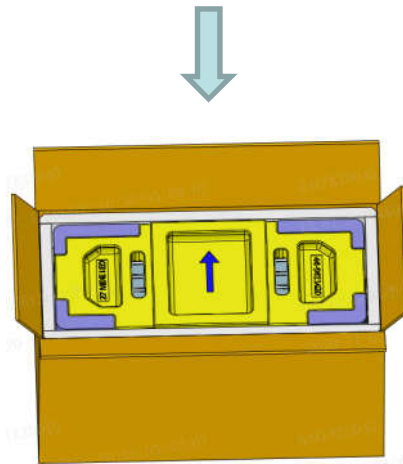
Put EPE bottom into the inner box.



Put EPO bottom into the EPE Bottom  
Put each module into a PE bag.  
Insert 6 Pcs MDL into each box



Place paper corners and wrap film around the boxes.  
Pack with 4 packing belts.



Put 1 EPO cover in and seal the box.

### 13.2 Packing Note

- Box Dimension : 744mm(W) × 2346mm(L) × 488mm(H)
- Package Quantity in one Box : 6 pcs

### 13.3 Box label

- Label Size : 108 mm (L) × 56 mm (W)

- Contents

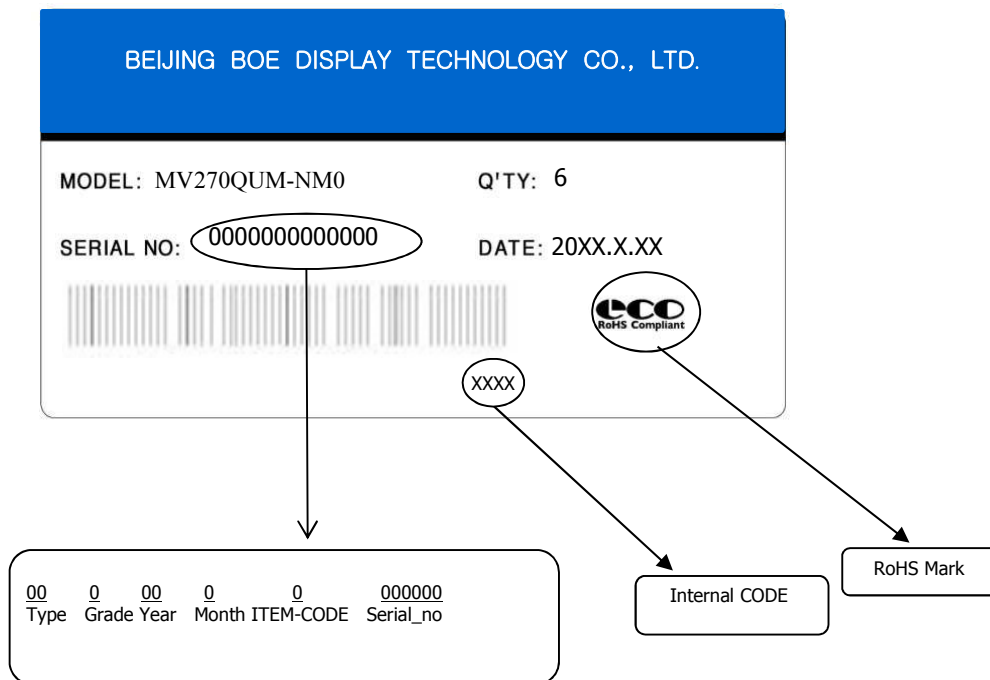
Model : MV270QUM-NM0

Q`ty : Module 6 Q`ty in one box

Serial No. : Box Serial No. See next page for detail description.

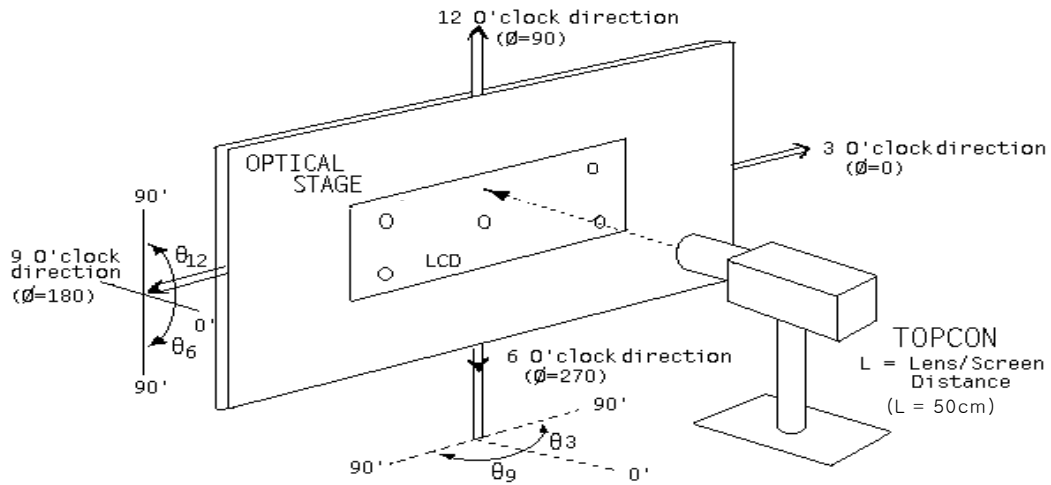
Date : Packing Date

FG Code : FG Code of Product

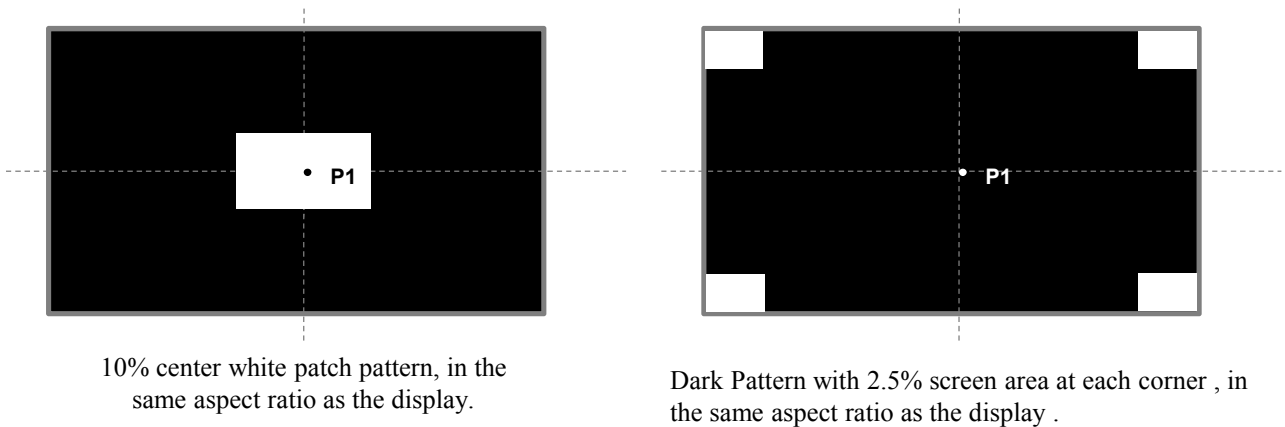


## 14.0 APPENDIX

**Figure 1. Measurement Set Up**

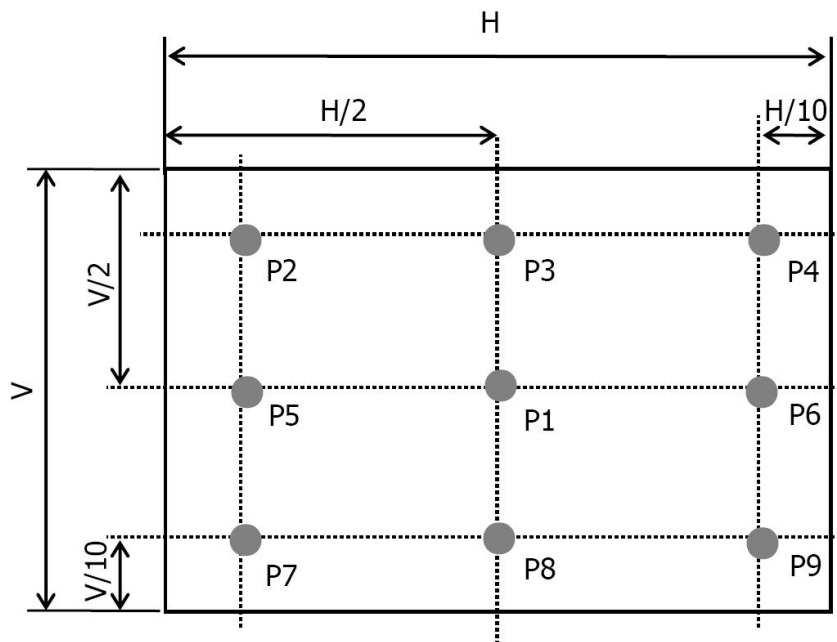


**Figure 2. DYNAMIC CR TEST PATTERN**

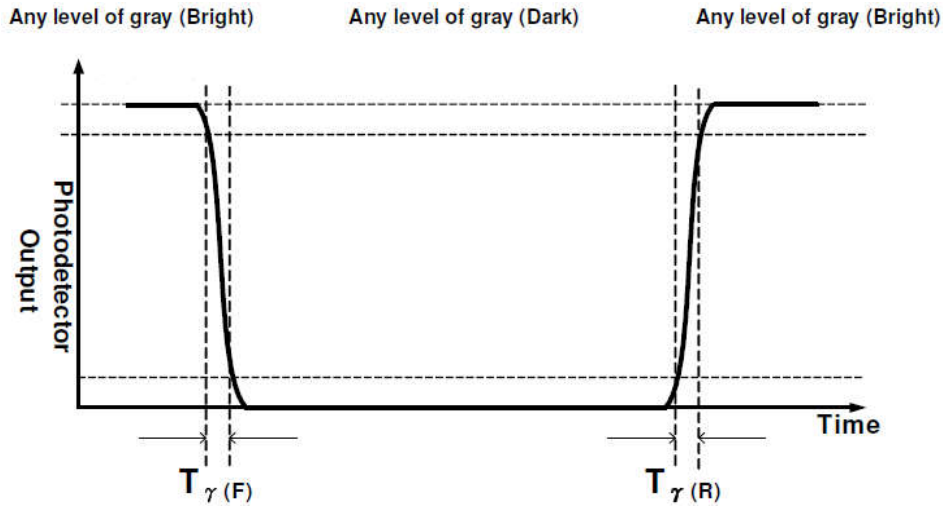




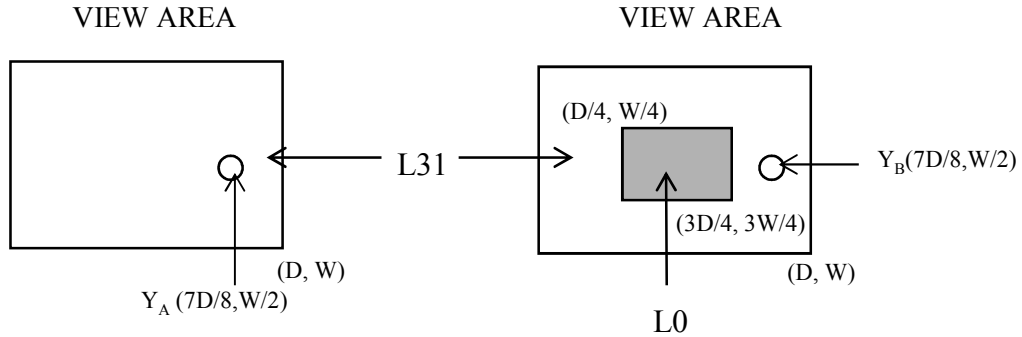
**Figure 3. White Luminance and Uniformity Measurement Locations (9 points)**



**Figure 4. Response Time Testing**



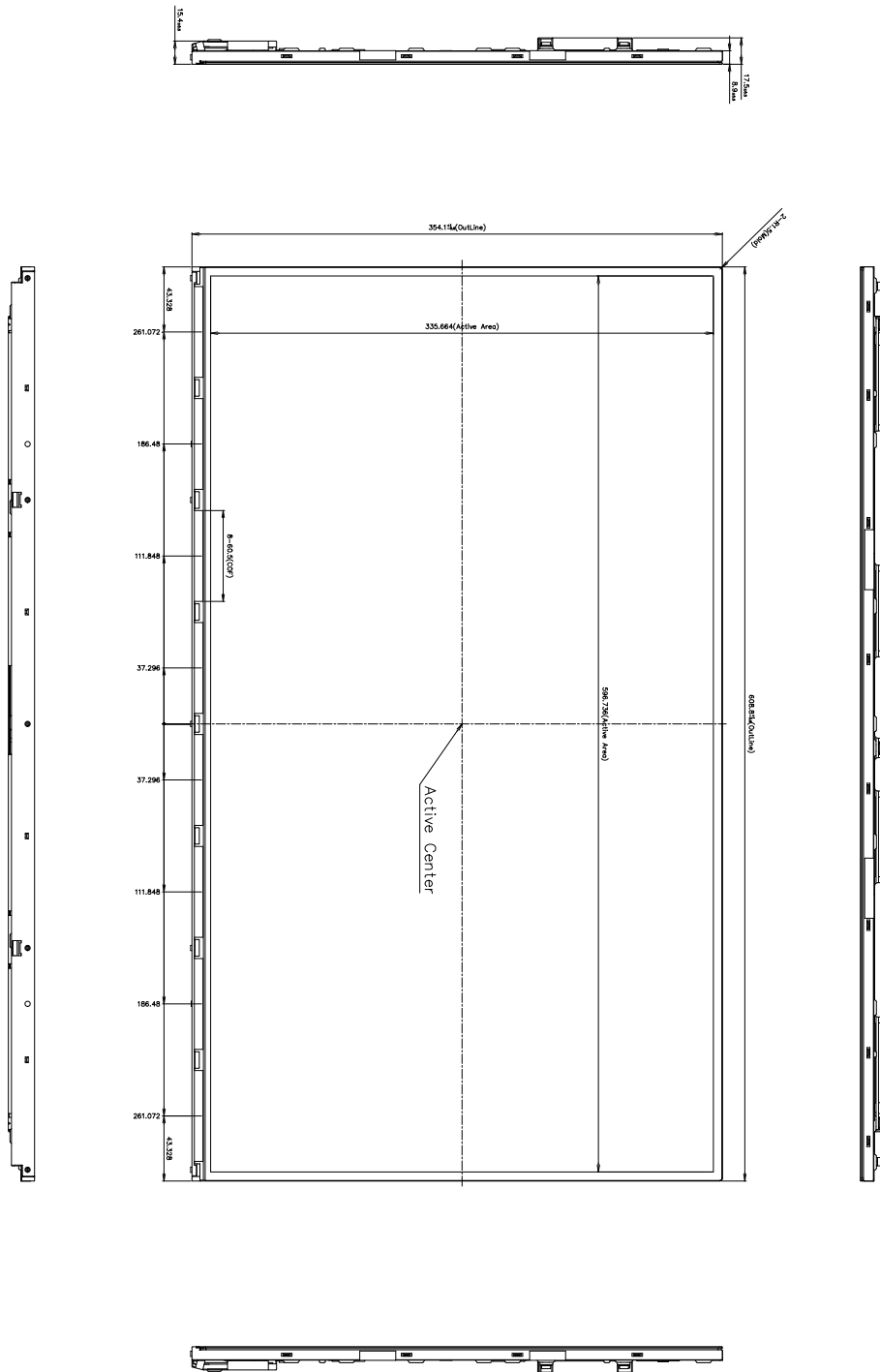
**Figure 5. Cross Modulation Test Description**



$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where:  $Y_A$  = Initial luminance of measured area (cd/m<sup>2</sup>)  
 $Y_B$  = Subsequent luminance of measured area (cd/m<sup>2</sup>)  
 The location measured will be exactly the same in both patterns

**Figure 6. TFT-LCD Module Outline Dimensions (Front view)**



### Figure 7. TFT-LCD Module Outline Dimensions (Rear view)

- NOTE:
1. I/F CONNECTOR SPECIFICATION  
CN1:MSAK240ZSP30 or EQUIVALENT CN5:C14603S or EQUIVALENT
  2. BLU PCB CONNECTOR SPECIFICATION  
CN2:C10114M1HRO-NH CN3:C14410M1HRO-NH CN4:C14610M1HRO-NH
  3. USER MOUNTING TORQUE SPEC : 3 ~ 4 kgf-cm  
Tilt and portial disposition tolerance of display area as following  
(1)Y-direction  $-0.45 \leq A \leq 0.45$ ,  $-0.45 \leq B \leq 0.45$   
(2)X-direction  $-0.45 \leq C \leq 0.45$ ,  $-0.45 \leq D \leq 0.45$
- 4.The COF area is weak & sensitive, so please don't press the COF Area

