DATA MODUL

SPECIFICATION

KOE
JDI Group

TX26D203VM2BAA

10.4” TFT - XGA - LVDS

Version: 7B64LTD-2478-1
Date: 17.04.2015

Note: This specification is subject to change without prior notice

KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

TENTATIVE

FOR MESSRS :_____ DATE : Apr. 17th ,2015

TECHNICAL DATA

TX26D203VM2BAA

Contents

ACCEPTED BY:_____ PROPOSED BY: Ken Chen

2. RECORD OF REVISION

ATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 10.4” XGA format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R(red), G(green), B(blue) sequentially. This display is RoHS compliant, and COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX26D203VM2BAA
Module Dimensions	235.0(W) mm x 180.2(H) mm x 9.5(D) mm
LCD Active Area	211.2(W) mm x 158.4(H) mm
Dot Pitch	0.20625(W) mm x 0.20625(H) mm
Resolution	1024 x 3(RGB)(W) x 768(H) Dots
Color Pixel Arrangement	R, G, B Vertical Stripe
LCD Type	Transmissive Color TFT; Normally White
Display Type	Active Matrix
Number of Colors	262K (6-bit) / 16.7M (8-bit RGB)
Backlight	Light Emitting Diode (LED)
Weight	370g
Interface	LVDS; 20 pins
Power Supply Voltage	3.3V for LCD; 30V for Backlight
Power Consumption	0.825W for LCD; (6.6)W for Backlight
Viewing Direction	12 O’clock (without image inversion and least brightness change) 6 O’clock (contrast peak located at)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	3.96	V	-
Input Voltage of Logic	V_I	-0.3	V_{DD}+0.3	V	Note 1
Operating Temperature	T_{op}	-30	80	˚C	Note 2
Storage Temperature	T_{st}	-30	80	˚C	Note 2
LED Forward Current	I_F	-	150	mA	-

Note 1: The rating is defined for the signal voltages of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25˚C.
- Operating under high temperature will shorten LED lifetime.

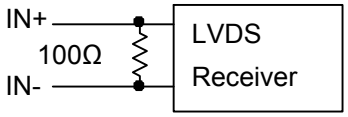
5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

$T_a = 25\ ^{\circ}C,\ \text{Vss} = 0\text{V}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	V_I	"H" level	-	-	+100	mV	Note 1
		"L" level	-100	-	-		
Power Supply Current	I_{DD}	V_{DD}-V_{SS} =3.3V	-	TBD	250	mA	Note 2
Frame Frequency	f_{Frame}	-	-	60	65	Hz	-
CLK Frequency	f_{CLK}	-	52	65	71	MHz	

Note 1: VCM 1.2V is common mode voltage of LVDS transmitter and receiver. The input terminal of LVDS receiver is terminated with 100Ω.



Note 2: An all black check pattern is used when measuring I_{DD}. f_{Frame} is set to 60Hz. Moreover, 1.0A fuse is applied in the module for I_{DD}. For display activation and protection purpose, power supply is recommended larger than 2.5A to start the display and break fuse once any short circuit occurred.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	I_{LED}=55mA	-	30	34	V	Note 1
LED Forward Current (per serial)	I_{LED}	-	-	55	-	mA	
LED Lifetime	-	I_{LED}=55mA	-	70K	-	hrs	Note 2

Note 1: Fig. 5.1 shows the LED backlight circuit.

Note 2: The estimated lifetime is specified as the time to reduce 50% brightness by applying 55 mA at 25°C.

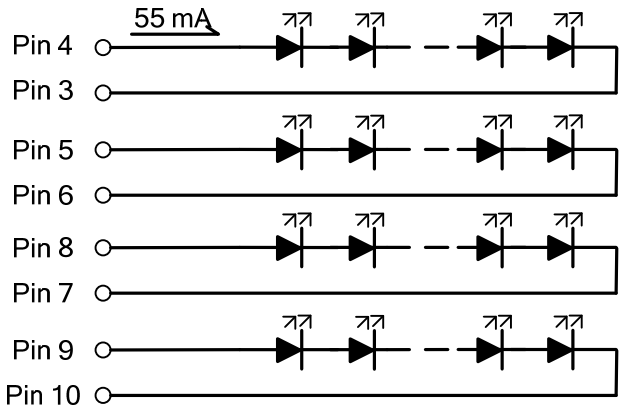


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^\circ C$, $f_{Frame} = 60$ Hz, $V_{DD} = 3.3V$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^\circ, \theta = 0^\circ$, I_{LED}= 55 mA	960	1200	-	cd/m^2	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2
Contrast Ratio		CR		-	900	-	-	Note 3
Response Time		Tr + Tf	$\phi = 0^\circ, \theta = 0^\circ$	-	16	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^\circ, \theta = 0^\circ$	-	50	-	%	-
Viewing Angle		θ x	$\phi = 0^\circ$, CR $\geq$ 10	-	75	-	Degree	Note 5
		θ x′	$\phi = 180^\circ$, CR $\geq$ 10	-	75	-		
		θ y	$\phi = 90^\circ$, CR $\geq$ 10	-	75	-		
		θ y′	$\phi = 270^\circ$, CR $\geq$ 10	-	75	-		
Color Chromaticity	Red	X	$\phi = 0^\circ, \theta = 0^\circ$	-	TBD	-	-	Note 6
		Y		-	TBD	-		
	Green	X		-	TBD	-		
		Y		-	TBD	-		
	Blue	X		-	TBD	-		
		Y		-	TBD	-		
	White	X		-	TBD	-		
		Y		-	TBD	-		

Note 1: The brightness is measured from the center point of the panel, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \text{ X100\%}$$

which is based on the brightness values of the 9 points in active area measured by BM-5 as shown in Fig. 6.2.

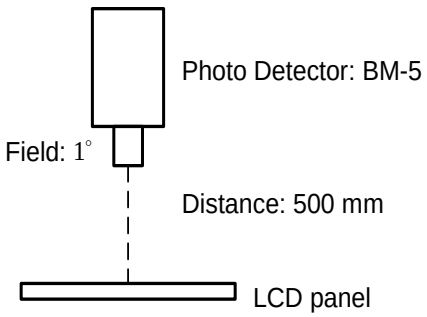


Fig 6.1

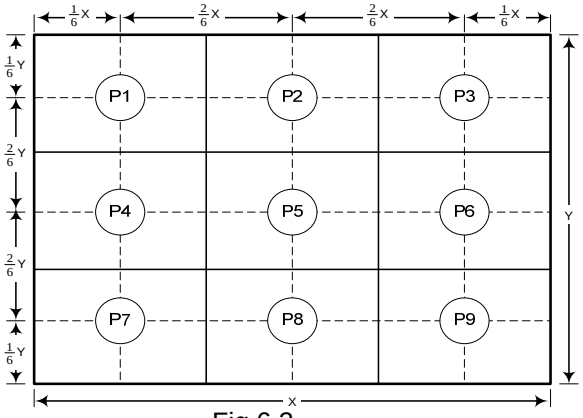


Fig 6.2

Note 3: The Contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 90% brightness to 10% brightness when the data is from white to black. Oppositely, Falling time is the period from 10% brightness rising to 90% brightness.

The viewing direction of this display is 12 o'clock, which means that a photograph with gray scale would not be reversed in color and the brightness change would be less from this direction. However, the best contrast peak would be located at 6 o'clock.

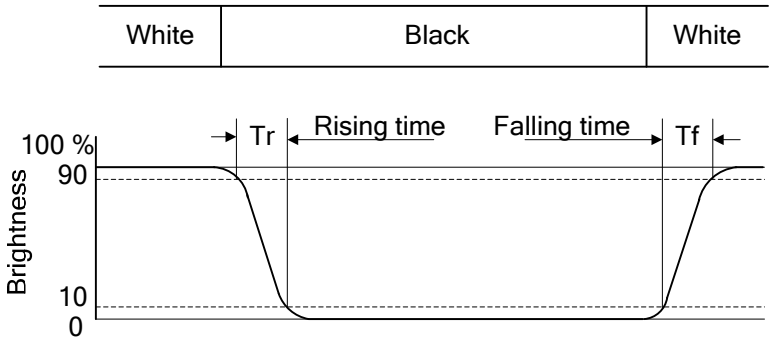


Fig 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

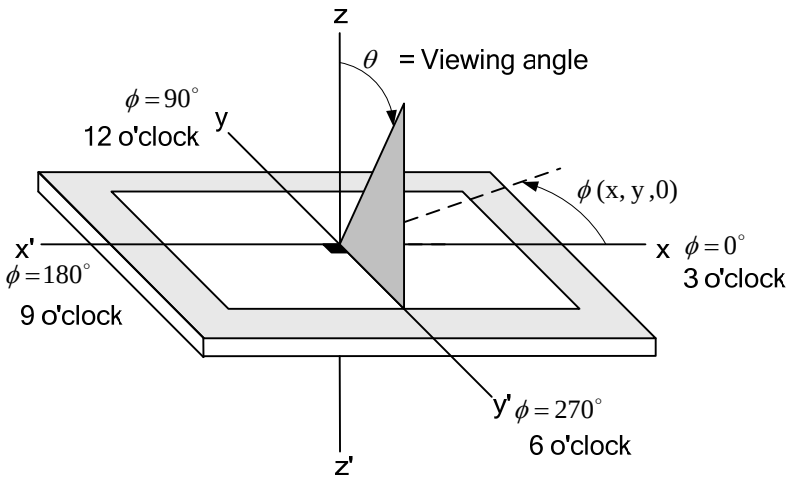
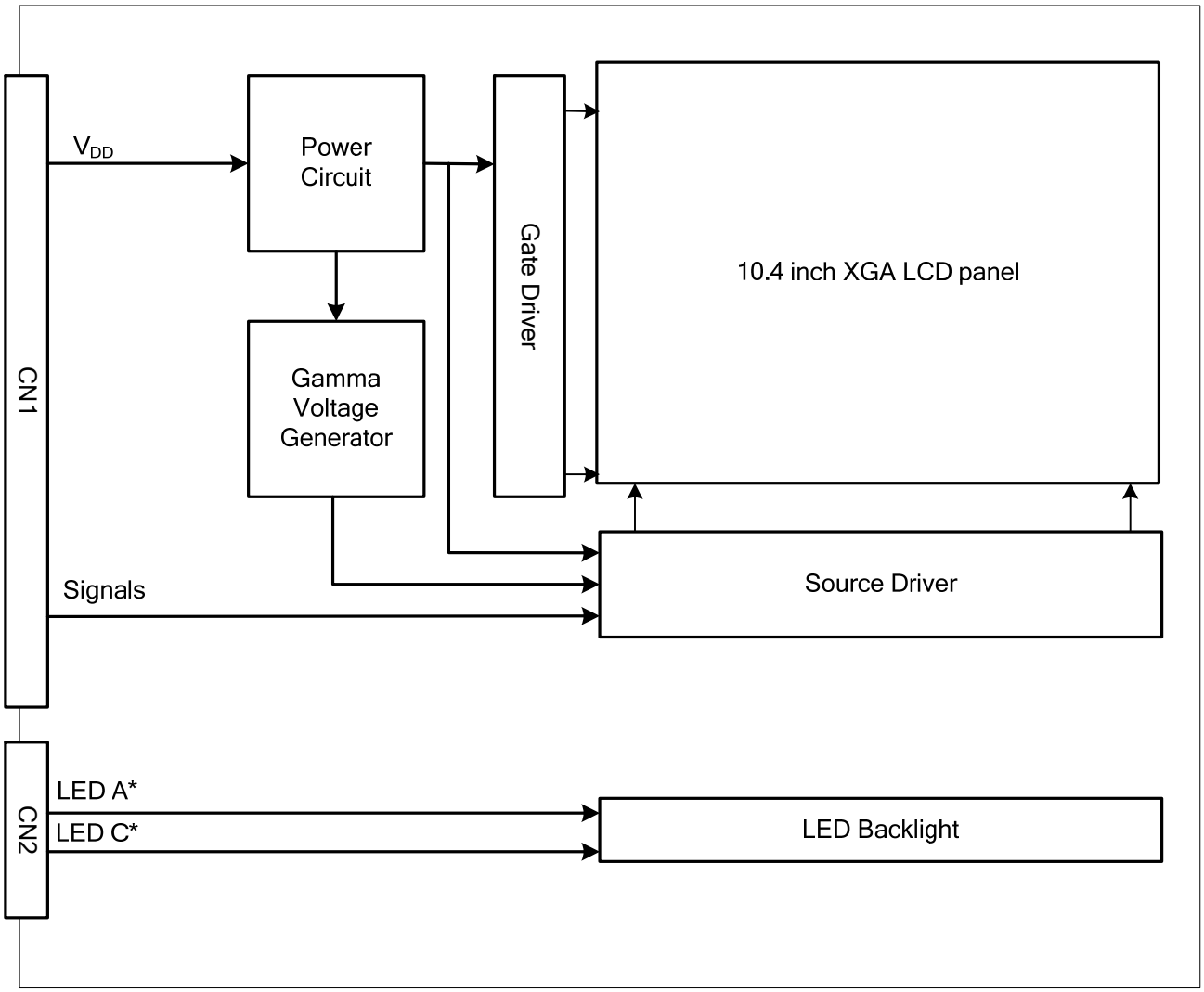


Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note : Signals are CLK and pixel data pairs.

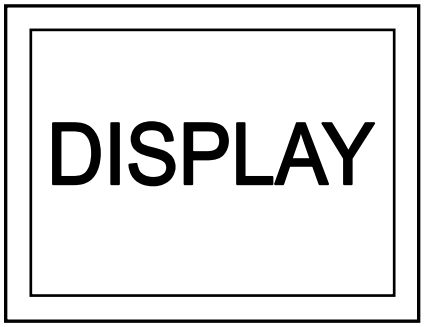
8. LCD INTERFACE

8.1 INTERFACE PIN CONNECTIONS

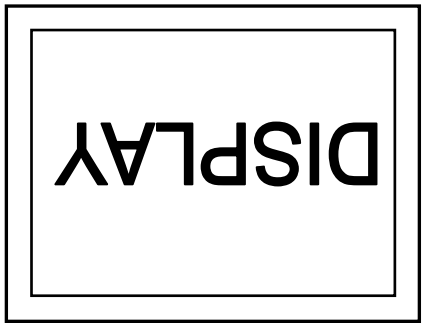
The display interface connector is CN1 MSB24013P20HA made by STM and pin assignment is as below:

Pin No.	Signal	Signal	Pin No.	Signal	Signal
1	V_{DD}	Power Supply for Logic	11	IN2-	B2~B5, DE
2	V_{DD}		12	IN2+	
3	V_{SS}	GND	13	V_{SS}	GND
4	SD	Scan Direction Control (Note 1)	14	CLK IN-	Pixel Clock
5	IN0-	R0~R5, G0	15	CLK IN+	
6	IN0+		16	V_{SS}	GND
7	V_{SS}	GND	17	IN3-	R6~R7, G6~G7, B6~B7
8	IN1-	G1~G5, B0~B1	18	IN3+	
9	IN1+		19	SEL	Data selection (H:8 bits L/NC:6bits)
10	V_{SS}	GND	20	NC	Test Pin

Note 1: Scan direction is available to be switched as below.



SD：Low or Open



SD：High

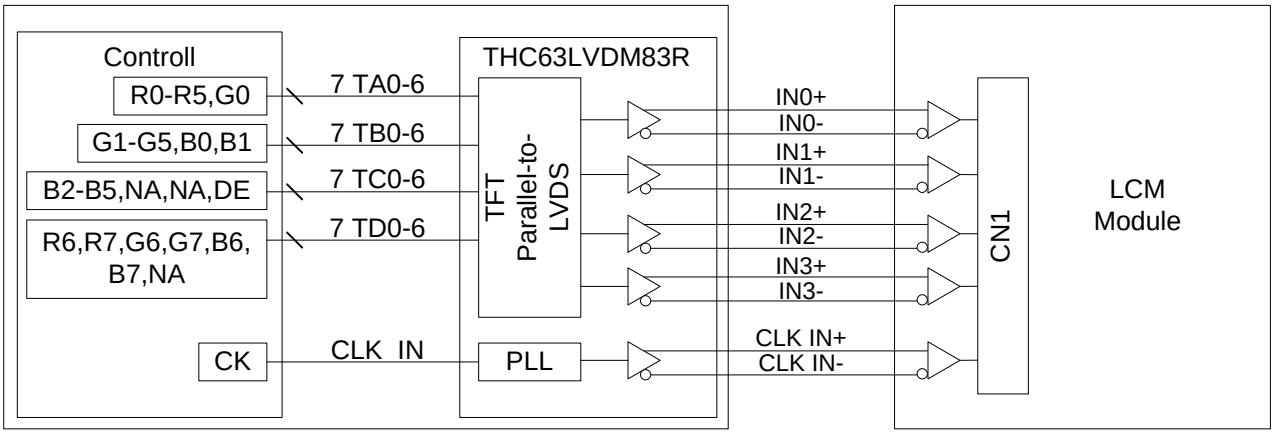
Note 2: INn- and INn+ (n=0,1,2,3), CLK IN- and CLK IN+ should be wired by twist-pairs or side-by-side FPC patterns, respectively.

The backlight interface connector CN2 is SM10B-SHLS-TS made by JST, and pin assignment as below:

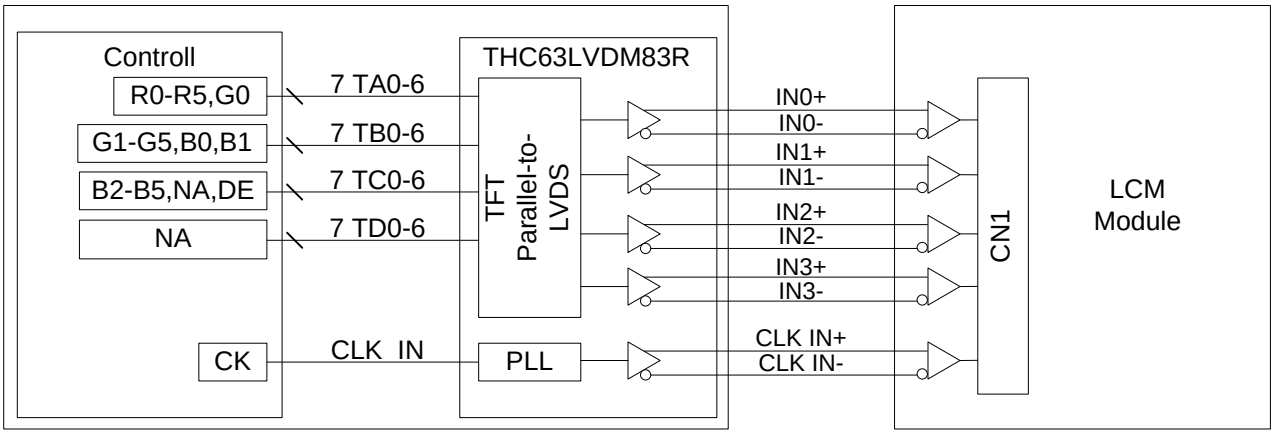
Pin No.	Signal	Level	Function
1	NC	-	This pin should be open
2	NC	-	
3	LED C1	-	LED Cathode1
4	LED A1	-	LED Anode1
5	LED A2	-	LED Anode2
6	LED C2	-	LED Cathode2
7	LED C3	-	LED Cathode3
8	LED A3	-	LED Anode3
9	LED A4	-	LED Anode4
10	LED C4	-	LED Cathode4

8.2 LVDS INTERFACE

(1) 8Bit Mode (SEL = H)



(2) 6Bit Mode (SEL = L)



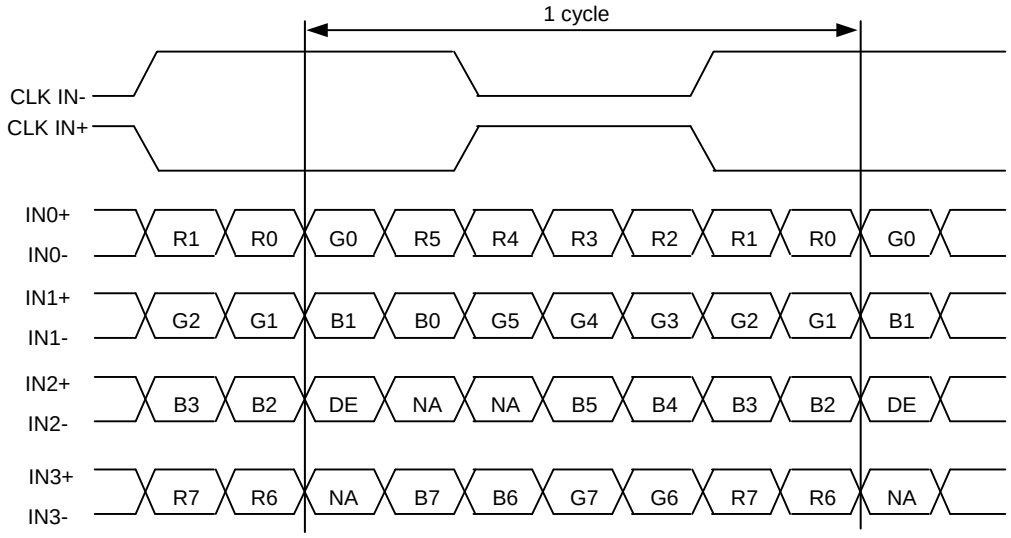
Note 1: LVDS cable impedance should be 100 ohms per signal line when each 2-lines (+,-) is used in differential mode.

Note 2: The recommended transmitter, THC63LVDM83R, is made by Thine or equivalent, which is not contained in the module.

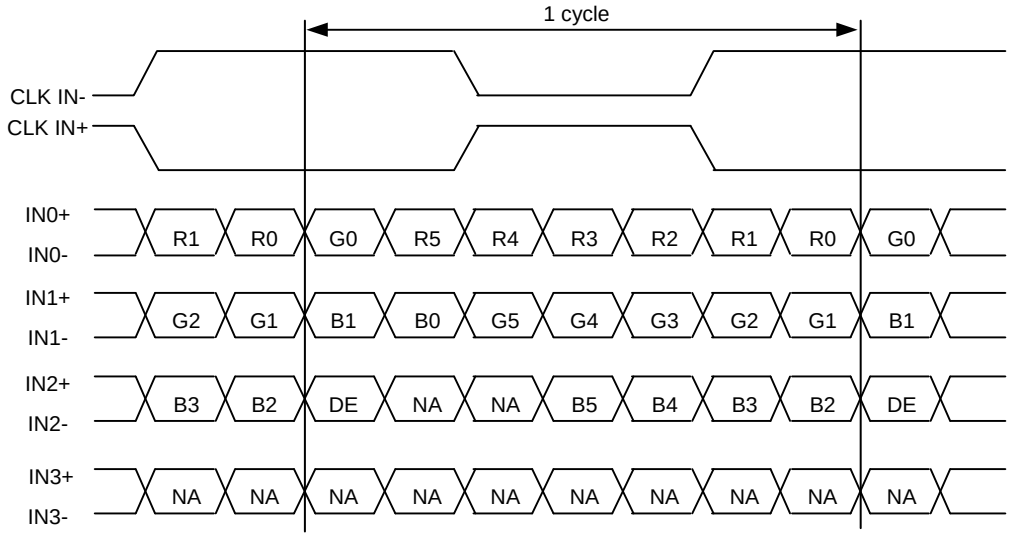
8.3 DATA MAPPING

Transmitter		8Bit Mode	6Bit Mode
Pin No.	Pin name	SEL	
		HIGH	LOW
51	TA0	R0(LSB)	R0(LSB)
52	TA1	R1	R1
54	TA2	R2	R2
55	TA3	R3	R3
56	TA4	R4	R4
3	TA5	R5	R5(MSB)
4	TA6	G0(LSB)	G0(LSB)
6	TB0	G1	G1
7	TB1	G2	G2
11	TB2	G3	G3
12	TB3	G4	G4
14	TB4	G5	G5(MSB)
15	TB5	B0(LSB)	B0(LSB)
19	TB6	B1	B1
20	TC0	B2	B2
22	TC1	B3	B3
23	TC2	B4	B4
24	TC3	B5	B5(MSB)
27	TC4	(NA)	(NA)
28	TC5	(NA)	(NA)
30	TC6	DE	DE
50	TD0	R6	(NA)
2	TD1	R7(MSB)	(NA)
8	TD2	G6	(NA)
10	TD3	G7(MSB)	(NA)
16	TD4	B6	(NA)
18	TD5	B7(MSB)	(NA)
25	TD6	(NA)	(NA)

(1) 8Bit Mode (SEL = H)



(2) 6Bit Mode (SEL = L)



DE : Display Enable

NA : Not Available

8.4 TIMING CHART

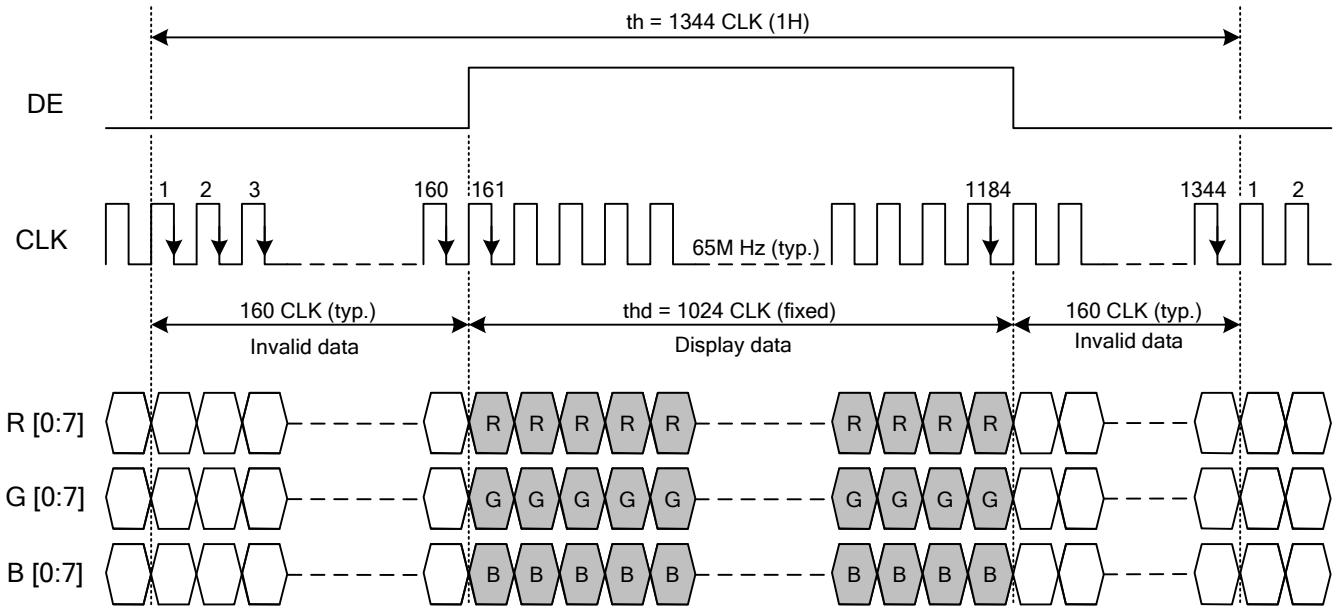


Fig. 8.1 Horizontal Timing

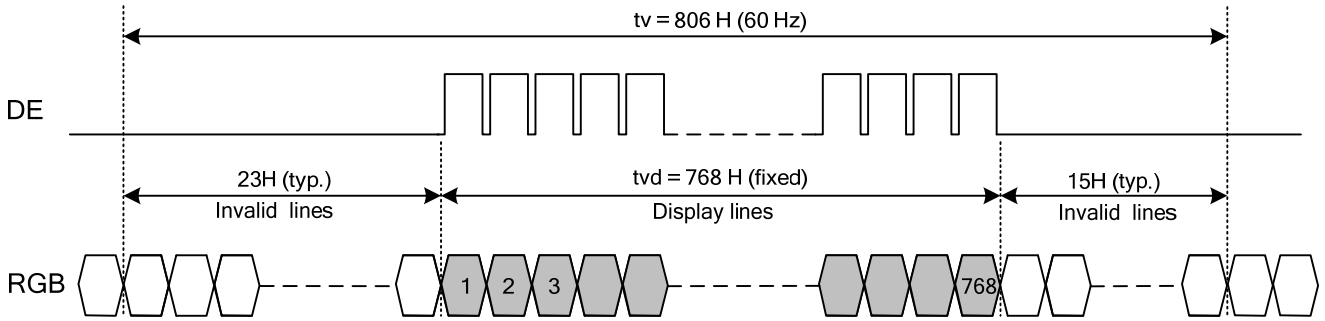


Fig. 8.2 Vertical Timing

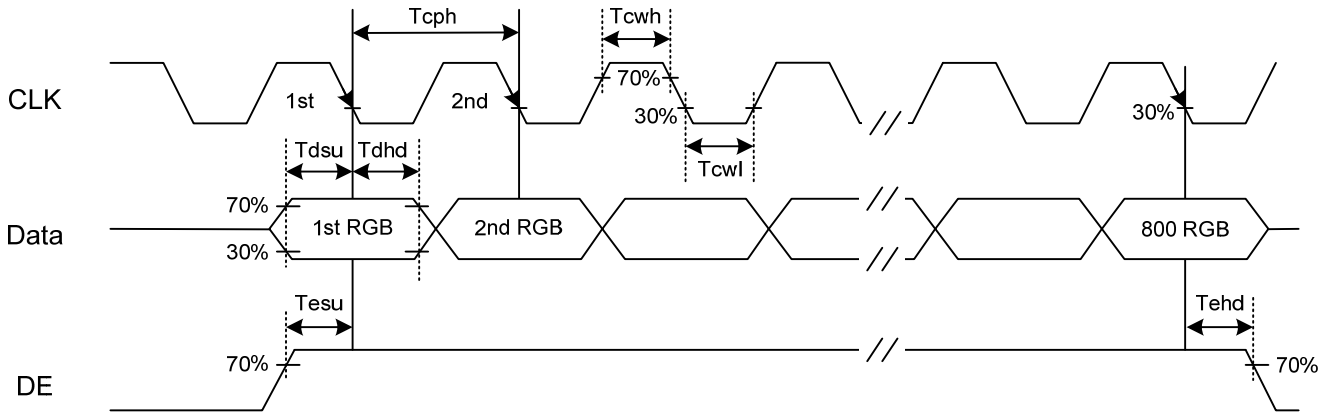


Fig. 8.3 Setup & Hold Time

8.5 TIME TABLE

The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (f_{Frame}) = 60 Hz to define. If 60 Hz is not the aim to set, less than 66 Hz for Vsync is recommended to apply for better performance by other parameter combination as the definitions in section 5.1.

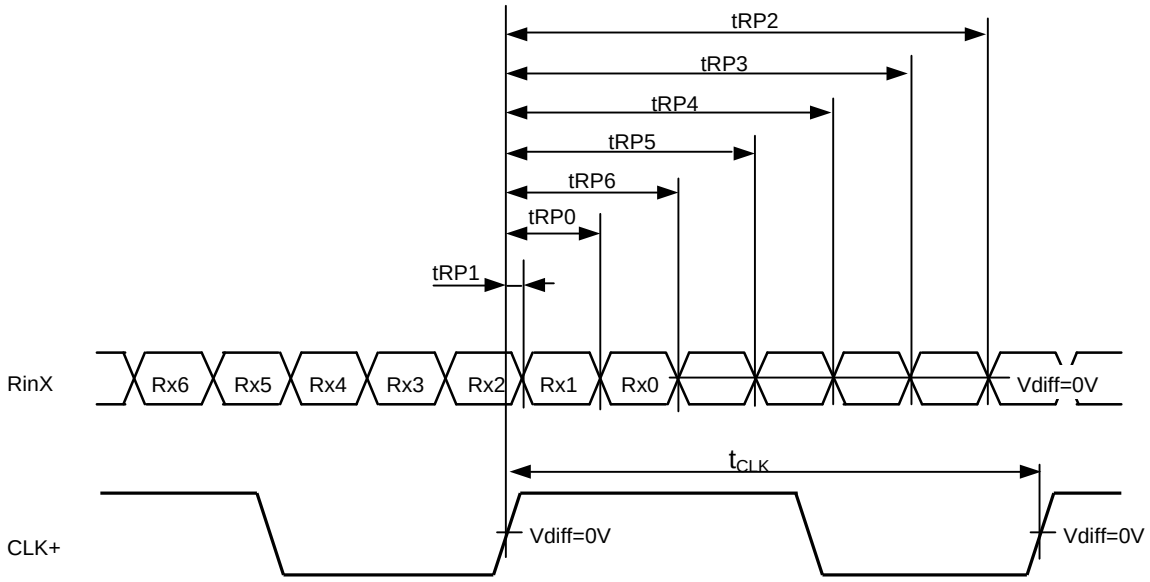
A. Horizontal and Vertical Timing

Item		Symbol	Min.	Typ.	Max.	Unit
Horizontal	CLK Frequency	fclk	52	65	71	M Hz
	Display Data	thd		1024		CLK
	Cycle Time	th	1114	1344	1400	
Vertical	Display Data	tvd		768		H
	Cycle Time	tv	778	806	845	

B. Setup and Hold Time

Item		Symbol	Min.	Typ.	Max.	Unit
CLK	Duty	Tcwh	40	50	60	%
	Cycle Time	Tcph	14	15.38	-	ns
Data	Setup Time	Tdsu	5	-	-	
	Hold Time	Tdhd	5	-	-	
DE	Setup Time	Tesu	5	-	-	
	Hold Time	Tehd	5	-	-	

8.6 LVDS RECEIVER TIMING



RinX= (RinX+)-(RinX-) (X=0, 1, 2, 3)

Item		Symbol	Min.	Typ.	Max.	Unit
CLK	Cycle frequency	1/tcLK	52	65	71	MHz
RinX (X=0,1,2,3)	0 data position	tRP0	1/7* t_{CLK} -0.49	1/7* t_{CLK}	1/7* t_{CLK} +0.49	ns
	1st data position	tRP1	-0.49	0	+0.49	
	2nd data position	tRP2	6/7* t_{CLK} -0.49	6/7* t_{CLK}	6/7* t_{CLK} +0.49	
	3rd data position	tRP3	5/7* t_{CLK} -0.49	5/7* t_{CLK}	5/7* t_{CLK} +0.49	
	4th data position	tRP4	4/7* t_{CLK} -0.49	4/7* t_{CLK}	4/7* t_{CLK} +0.49	
	5th data position	tRP5	3/7* t_{CLK} -0.49	3/7* t_{CLK}	3/7* t_{CLK} +0.49	
	6th data position	tRP6	2/7* t_{CLK} -0.49	2/7* t_{CLK}	2/7* t_{CLK} +0.49	

8.7 DATA INPUT for DISPLAY COLOR(8BIT MODE)

Input color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

Note 2: Data Signal : 1 : High, 0 : Low

(6BIT MODE)

Input		Red Data						Green Data						Blue Data					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
color		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

Note 2: Data Signal : 1 : High, 0 : Low

8.8 POWER SEQUENCE

Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD voltage is off.

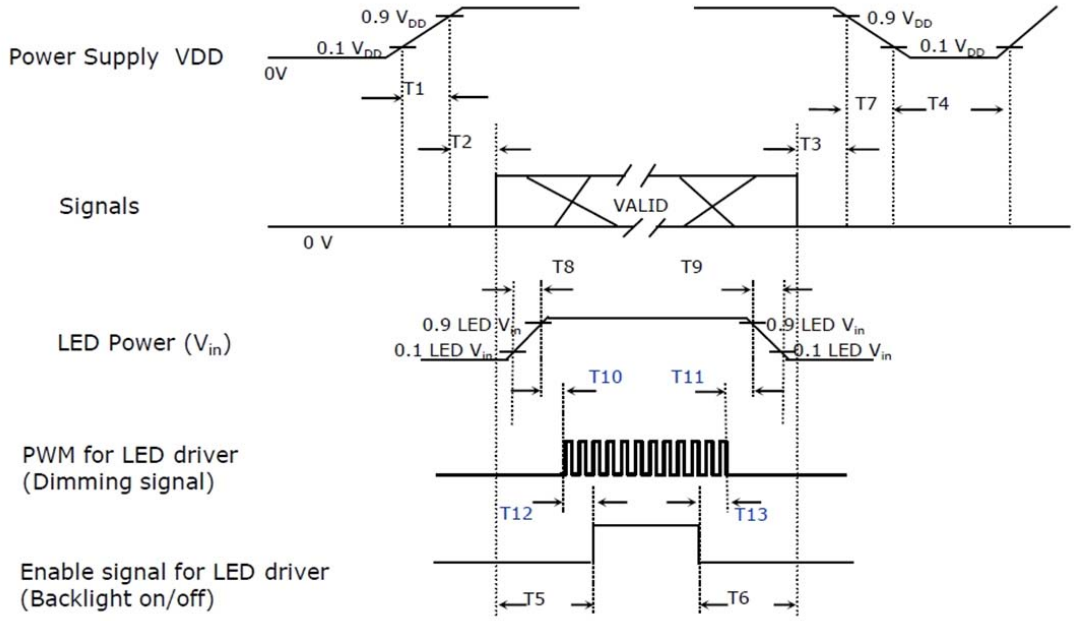
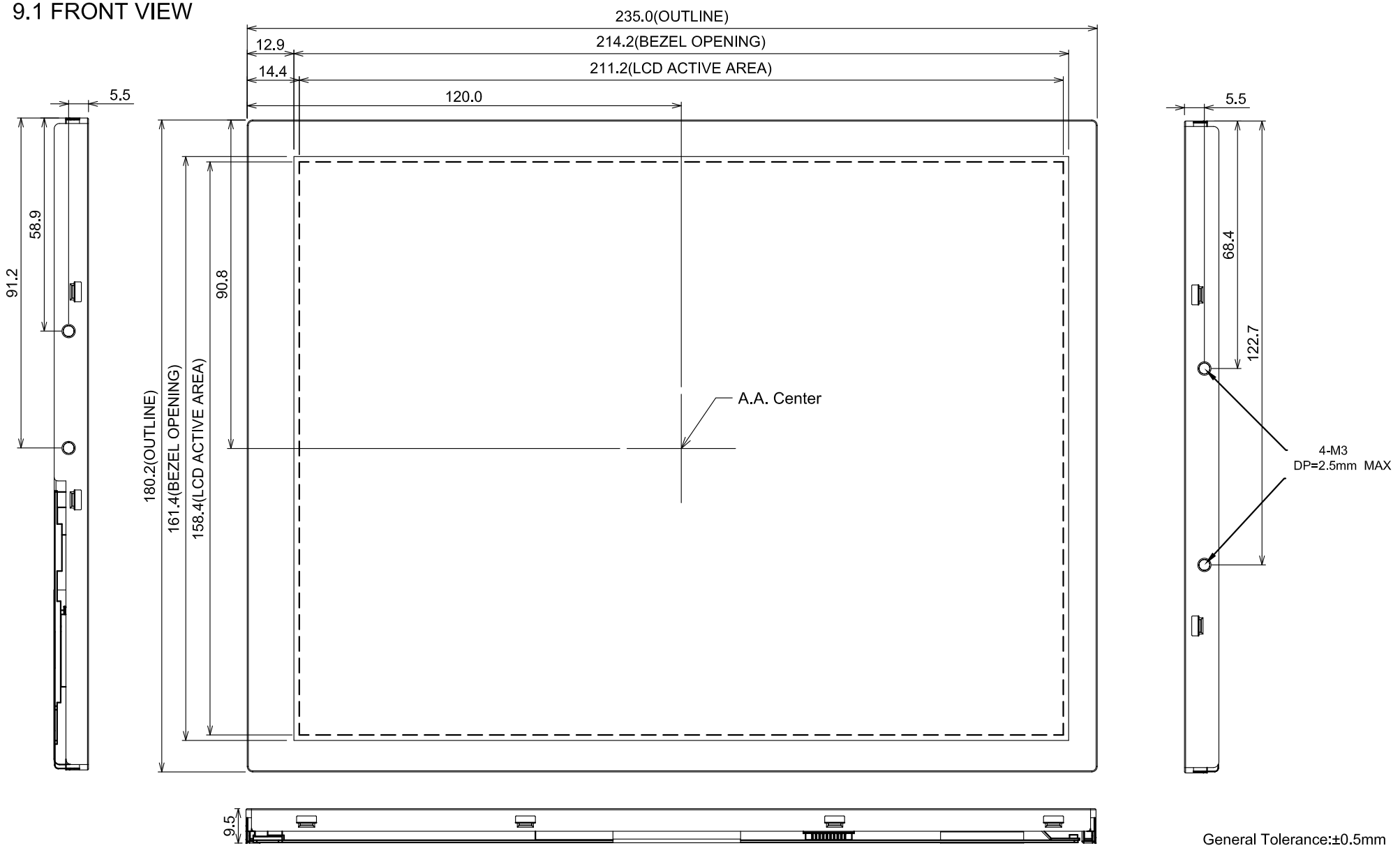


Fig 8.4 Power Sequence

Parameter	Symbol	Min.	Typ.	Max.	Unit
VDD rising time from 10% to 90%	T1	0.5	-	10	ms
Delay from VDD to valid data at power ON	T2	30	-	50	ms
Delay from valid data OFF to VDD OFF at power OFF	T3	0	-	50	ms
VDD OFF time for windows restart	T4	500	-	-	ms
Delay from valid data to B/L enable at power ON	T5	200	-	-	ms
Delay from valid data off to B/L disable at power Off	T6	200	-	-	ms
VDD falling time from 90% to 10%	T7	0.5	-	10	ms
LED Vin rising time from 10% to 90%	T8	0.5	-	10	ms
LED Vin falling time from 90% to 10%	T9	0.5	-	10	ms
Delay from LED driver Vin rising time 90% to PWM ON	T10	0	-	-	ms
Delay from PWM Off to LED driver Vin falling time 10%,Must keep rule	T11	0	-	-	ms

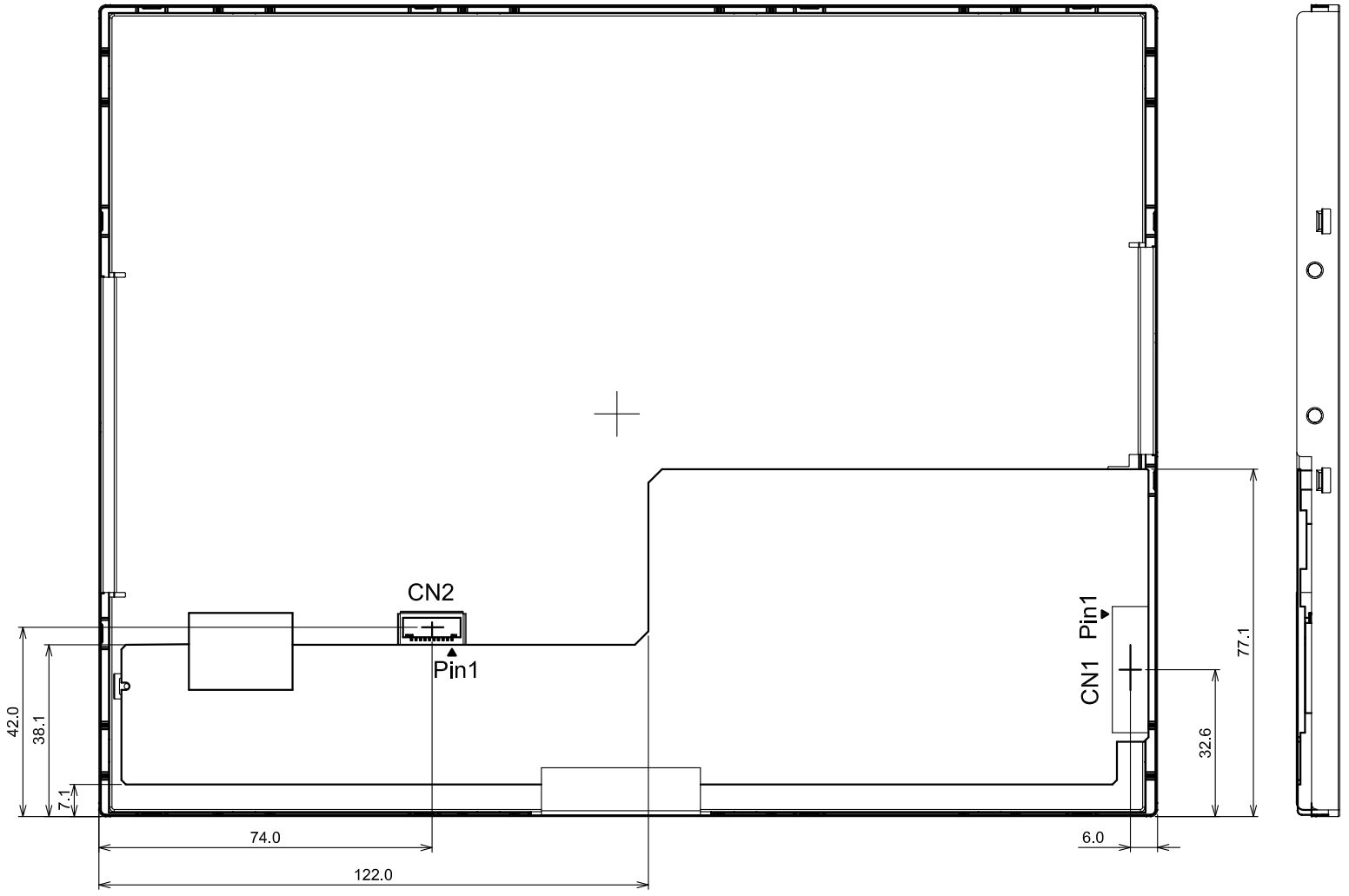
9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

9.2 REAR VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

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