



SPECIFICATION

KOE
JDI Group

TX26D206VM0BAA

10.25" TFT - LTPS - LVDS

Version: 1.0

Date: 31.08.2018

Note: This specification is subject to change without prior notice

KOE

JDI Group

TENTATIVE

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____

DATE : Aug. 31st, 2018

TECHNICAL DATA

TX26D206VM0BAA(ES)

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ACCEPTED BY : _____

PROPOSED BY : Oblack Tsai

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY																	
Aug.31,'18	7B64LTD-2562-2 Page 3-1/1	3.1 DISPLAY FEATURES Revised : amorphous silicon → LTPS Power Consumption : (TBD) → 0.46W for LCD , 8.2W for Backlight																	
	7B64LTD-2562-2 Page 5-1/2~2/2	5.1 OPERATING CONDITIONS Revised : Power Supply Current : TYP.=610mA → TYP.=138mA , MAX.=210mA 5.2 BACKLIGHT CHARACTERISTICS Revised : LED Forward Current : TYP.630mA → TYP.680mA																	
	7B64LTD-2562-2 Page 6-1/2	6. OPTICAL CHARACTERISTICS Revised : Brightness of White=TYP.1000 cd/m ² → TYP. 1200 cd/m ² <table border="1" data-bbox="580 779 1485 1003"> <thead> <tr> <th colspan="2">Item</th> <th>X</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td rowspan="4">Color Chromaticity</td> <td>Red</td> <td>0.64 → 0.63</td> <td>0.32 → 0.33</td> </tr> <tr> <td>Green</td> <td>0.31 → 0.34</td> <td>0.61 → 0.62</td> </tr> <tr> <td>Blue</td> <td>-</td> <td>0.06 → 0.05</td> </tr> <tr> <td>White</td> <td>-</td> <td>0.36 → 0.34</td> </tr> </tbody> </table>	Item		X	Y	Color Chromaticity	Red	0.64 → 0.63	0.32 → 0.33	Green	0.31 → 0.34	0.61 → 0.62	Blue	-	0.06 → 0.05	White	-	0.36 → 0.34
	Item		X	Y															
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		White	-	0.36 → 0.34															
7B64LTD-2562-2 Page 7-1/1	7. BLOCK DIAGRAM All Page Change																		
7B64LTD-2562-2 Page 8-2/8	8.1 INTERFACE PIN CONNECTIONS All Page Change																		
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7B64LTD-2562-2 Page 9-2/2	9.2 REAR VIEW All Page Change																		

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 10.25" HD of 8:3 format LTPS TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX26D206VM0BAA
Module Dimensions	259.0(W) mm x 111.4(H) mm x 14.2 (D) mm
LCD Active Area	243.7(W) mm x 91.4(H) mm
Pixel Pitch	0.1269(W) mm x 0.1269 (H) mm
Resolution	1920 x 3(RGB)(W) x 720(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally Black
Display Type	Active Matrix
Number of Colors	16.7M Colors (8-bit RGB)
Backlight	Light Emitting Diode (LED)
Weight	430g
Interface	2ch-LVDS; 50 pins
Power Supply Voltage	3.3V for LCD; 12V for Backlight
Power Consumption	0.46W for LCD , 8.2W for Backlight
Viewing Direction	Super Wide Version (In-Plane Switching)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	4.0	V	-
Input Voltage of Logic	V_I	-0.3	$V_{DD} + 0.3$	V	Note 1
Operating Temperature	T_{op}	-40	85	°C	Note 2
Storage Temperature	T_{st}	-40	90	°C	Note 2
Backlight Input Voltage	V_{LED}	6	21	V	-
Backlight Voltage for PWM	V_{PWM}	-0.3	6	V	-
Backlight Voltage for VDC	V_{DC}	0	3.3	V	-
Backlight Voltage for EN	V_{EN}	-0.3	6	V	-

Note 1: The rating is defined for the signal voltages of the interface such as CLK and data pairs.

Note 2: The maximum rating is defined as above based on the chamber temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.

5. ELECTRICAL CHARACTERISTICS

5.1 OPERATING CONDITIONS

$T_a = 25\text{ }^\circ\text{C}$, $V_{SS} = 0\text{V}$

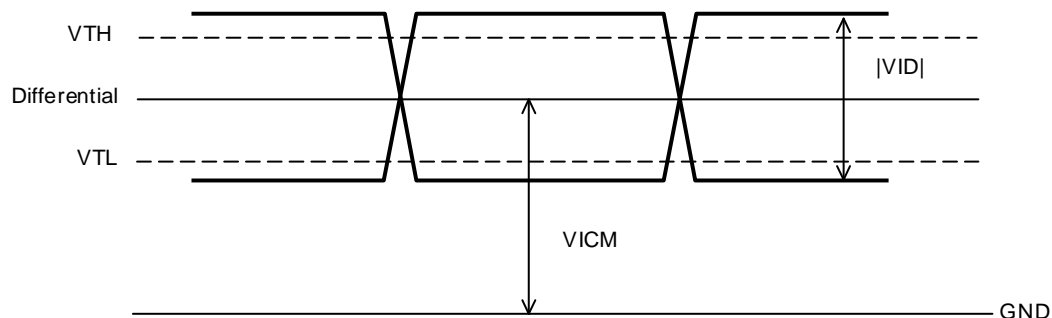
Item	Symbol	Condition	Standard Value			Unit	Remarks
			Min.	Typ.	Max.		
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Power Supply Current	I_{DD}	Note 1	-	138	210	mA	Note 1,4
Input Signal Voltage (CMOS)	V_{IH1}	-	$0.8V_{DD}$	-	V_{DD}	V	Note 2
	V_{IL1}	-	V_{SS}	-	$0.2V_{DD}$	V	
Allowable Ripple Voltage	VRP	-	-	-	100	mV (p-p)	-
Differential Input High Threshold	VTH	$V_{ICM}=1.2\text{V}$	-	-	100	mV	Note 3
Differential Input Low Threshold	VTL	$V_{ICM}=1.2\text{V}$	-100	-	-	mV	
Input Differential Voltage	VID	-	100	-	600	mV	
Differential Input Common Mode Voltage	V_{ICM}	-	1.125	1.2	1.375	V	

Note 1: Measurement pattern: All white.

Power supply voltage: Typ. voltage.

Note 2: Signals of interest is UL / DR.

Note 3: Signal of interest is LVDS.



Note 4: (TBD) fuse is applied in the module for I_{DD} . For display activation and protection purpose, power supply is recommended larger than (TBD) to start the display and break fuse once any short circuit occurred.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25^\circ\text{C}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	$I_{LED}=680\text{mA}$	11.5	12	12.5	V	Note 1
LED Forward Current	I_{LED}	3.3V _{DC} ; 100% duty	(TBD)	680	(TBD)	mA	Note 2
		0.2 V _{DC} ; 0% duty	(TBD)	60	(TBD)		
PWM Signal Voltage	-	High	2.5	3.3	5	V	-
		Low	-	-	0.9		
		Range	0	-	100	%	
EN Voltage	V_{EN}	-	2.5	3.3	5.0	V	-
LED Lifetime	-	$I_{LED}=680\text{mA}$	-	70K	-	hrs	Note 3

Note 1: Fig. 5.1 shows the LED backlight circuit.

Note 2: Dimming function can be obtained by applying PWM signal from the display interface CN2. The recommended PWM signal is 1K ~ 10KHz with 3.3 V amplitude.

Note 3: The estimated lifetime is specified as the time to reduce 50% brightness by applying 680mA at 25°C.

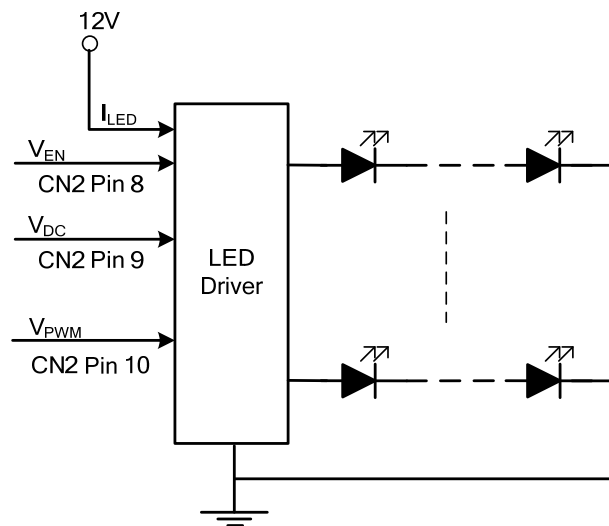


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25 °C .
- In the dark room around 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$$T_a = 25 \text{ }^\circ\text{C}, f_{Frame} = 60 \text{ Hz}, V_{DD} = 3.3\text{V}$$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White	-	$\phi = 0^\circ, \theta = 0^\circ,$ $I_{LED} = 680 \text{ mA}$	950	1200	-	cd/m ²	Note 1
Brightness Uniformity	-		70	-	-	%	Note 2
Contrast Ratio	CR		500	1000	-	-	Note 3
Response Time	$T_r + T_f$	$\phi = 0^\circ, \theta = 0^\circ$	-	20	-	ms	Note 4
NTSC Ratio	-	$\phi = 0^\circ, \theta = 0^\circ$	-	70	-	%	-
Viewing Angle	θ_x	$\phi = 0^\circ, CR \geq 10$	-	85	-	Degree	Note 5
	$\theta_{x'}$	$\phi = 180^\circ, CR \geq 10$	-	85	-		
	θ_y	$\phi = 90^\circ, CR \geq 10$	-	85	-		
	$\theta_{y'}$	$\phi = 270^\circ, CR \geq 10$	-	85	-		
Color Chromaticity	Red	X	-	0.63	-	-	Note 6
		Y	-	0.33	-		
	Green	X	-	0.34	-		
		Y	-	0.62	-		
	Blue	X	-	0.14	-		
		Y	-	0.05	-		
White	X	-	0.32	-			
	Y	-	0.34	-			

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

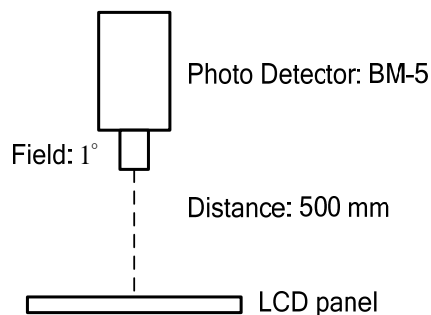


Fig. 6.1

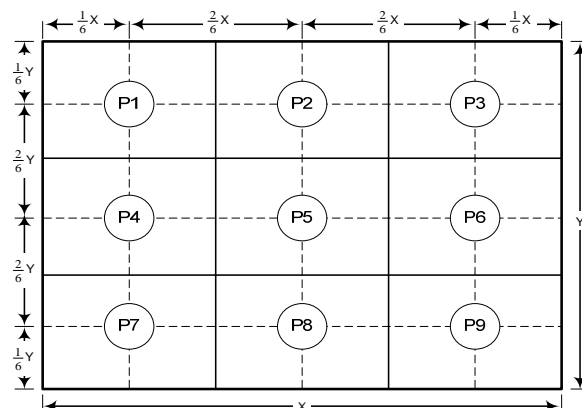


Fig. 6.2

Note 3: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness falling to 10% brightness.

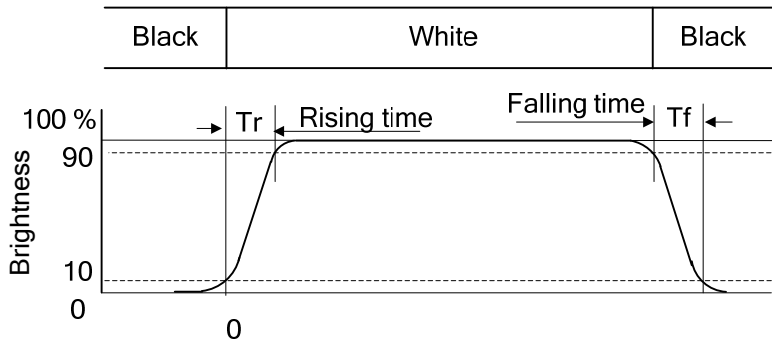


Fig 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version; 85° viewing angle can be obtained from each viewing direction.

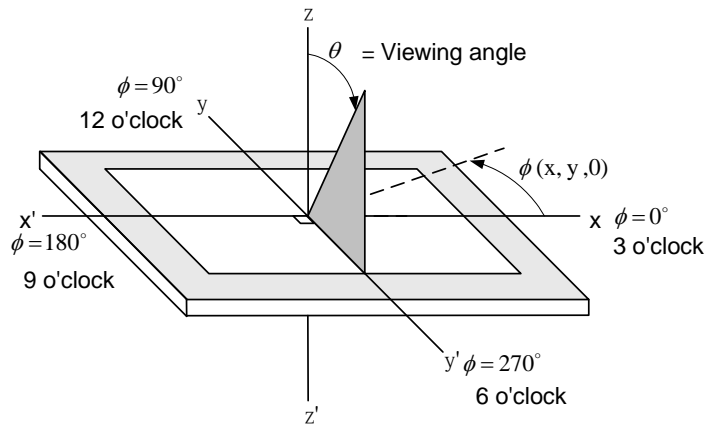
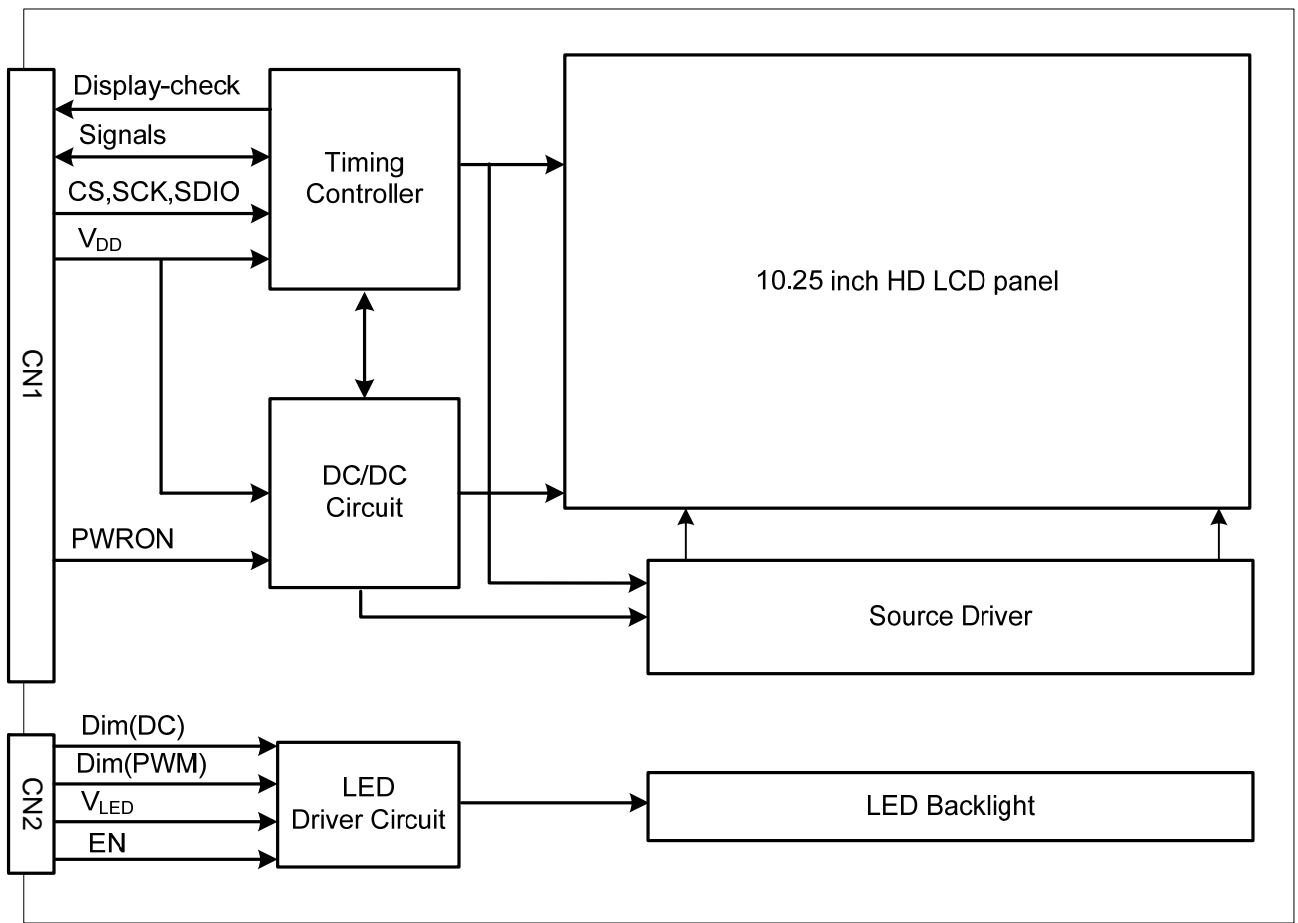


Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



8. LCD INTERFACE

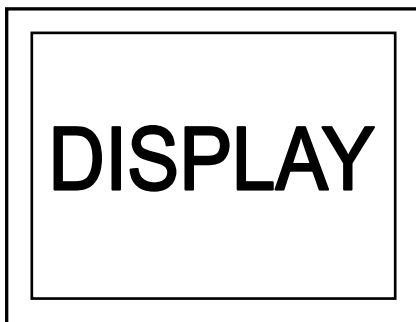
8.1 INTERFACE PIN CONNECTIONS

The display interface connector CN1 is FH28-50S-0.5SH (Hirose), and Pin assignment is as below:

No	Symbol	Function	I/O
1	GND	GND (0V)	I
2	GND	GND (0V)	I
3	GND	GND (0V)	I
4	GND	GND (0V)	I
5	NC	Not connected	-
6	NC	Not connected	-
7	GND	GND (0V)	I
8	GND	GND (0V)	I
9	GND	GND (0V)	I
10	GND	GND (0V)	I
11	NC	Not connected	-
12	VDD	+3.3V	I
13	VDD	+3.3V	I
14	VDD	+3.3V	I
15	VDD	+3.3V	I
16	NC	Not connected	-
17	UL/DR	Up & Left / Down & Right switching terminal (Note1)	I
18	GND	GND (0V)	I
19	NC	Not connected	-
20	GND	GND (0V)	I
21	RO0-	-LVDS differential data input, Chan 0-odd	I
22	RO0+	+LVDS differential data input, Chan 0-odd	I
23	GND	GND (0V)	I
24	RO1-	-LVDS differential data input, Chan 1-odd	I
25	RO1+	+LVDS differential data input, Chan 1-odd	I
26	GND	GND (0V)	I
27	RO2-	-LVDS differential data input, Chan 2-odd	I
28	RO2+	+LVDS differential data input, Chan 2-odd	I
29	GND	GND (0V)	I
30	CLKO-	-LVDS clock input(odd)	I

No	Symbol	Function	I/O
31	CLKO+	+LVDS clock input(odd)	I
32	GND	GND (0V)	I
33	RO3-	-LVDS differential data input, Chan 3-odd	I
34	RO3+	+LVDS differential data input, Chan 3-odd	I
35	GND	GND (0V)	I
36	RE0-	-LVDS differential data input, Chan 0-Even	I
37	RE0+	+LVDS differential data input, Chan 0-Even	I
38	GND	GND (0V)	I
39	RE1-	-LVDS differential data input, Chan 1-Even	I
40	RE1+	+LVDS differential data input, Chan 1-Even	I
41	GND	GND (0V)	I
42	RE2-	-LVDS differential data input, Chan 2-Even	I
43	RE2+	+LVDS differential data input, Chan 2-Even	I
44	GND	GND (0V)	I
45	CLKE-	-LVDS clock input(Even)	I
46	CLKE+	+LVDS clock input(Even)	I
47	GND	GND (0V)	I
48	RE3-	-LVDS differential data input, Chan 3-Even	I
49	RE3+	+LVDS differential data input, Chan 3-Even	I
50	GND	GND (0V)	I

Note 1: The scanning direction in is defined as below.



U/L/DR: Low or Open

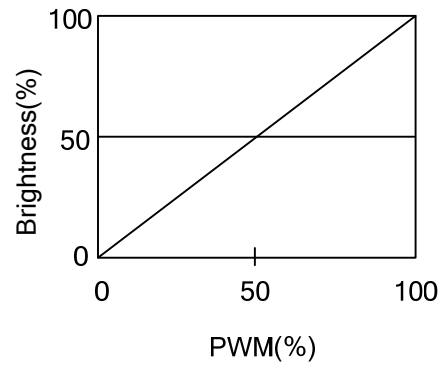
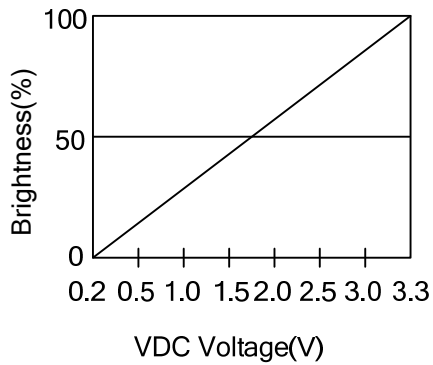


UL/DR : High

The interface CN2 is SM10B-SRSS-TB(LF)(SN) made by JST and pin assignment is as below:

Connector Name	Pin No.	Symbol	Function
SM10B-SRSS-TB(LF)(SN)	1	$V_{LED(+)}$	Power Supply for LED
	2	$V_{LED(+)}$	Power Supply for LED
	3	$V_{LED(+)}$	Power Supply for LED
	4	NC	No Connected
	5	$V_{LED(-)}$	GND
	6	$V_{LED(-)}$	GND
	7	$V_{LED(-)}$	GND
	8	V_{EN}	Backlight On/Off
	9	V_{DC}	Brightness dimming
	10	V_{PWM}	Brightness dimming

Note 1: The relationship of brightness and Dim control are shown as below.



8.2 TIMING CHART

Horizontal timing

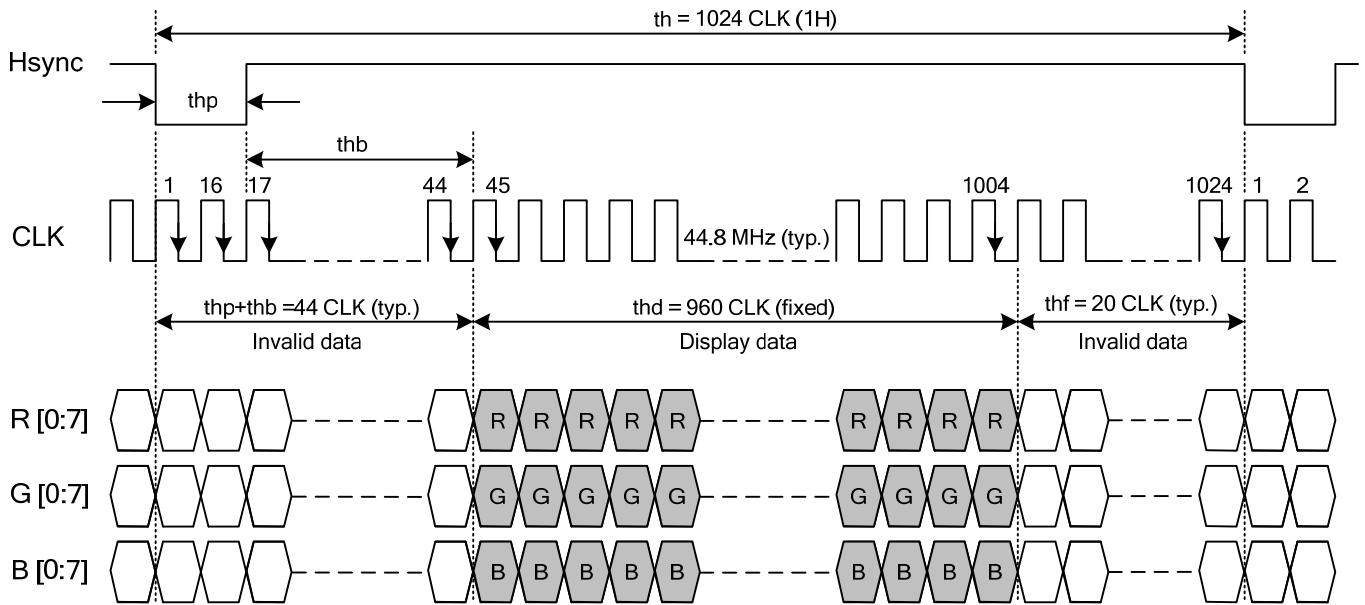


Fig. 9.1 Horizontal Timing of Synchronous Mode

Note 1: CLK's falling edge is the time to latch data and count ($thp + thb$), therefore, data sending and Hsync's falling edge should start when CLK's rise edge.

Vertical timing

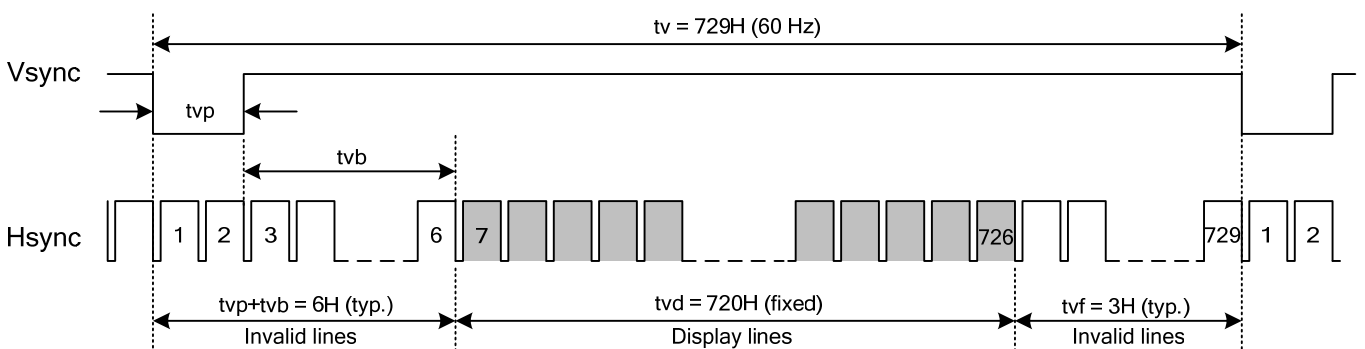


Fig. 9.2 Vertical Timing of Synchronous Mode

Note 2: Vsync's falling edge needs to start with Hsync's falling edge simultaneously to count ($tvp + tvb$)

8.2 TIMING TABLE

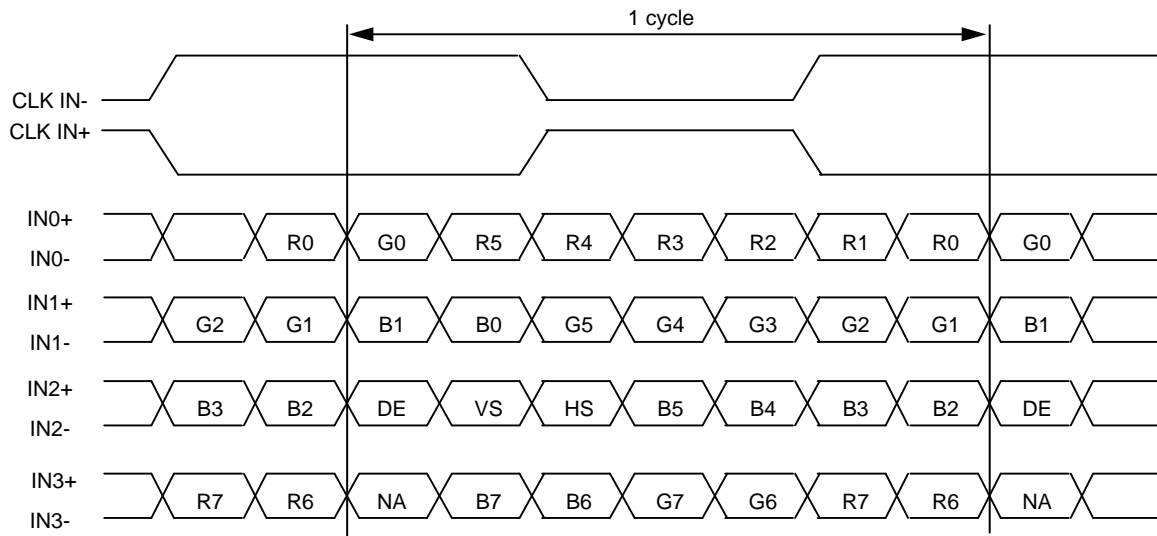
The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (f_{Frame}) = 60 Hz to define.

Item		Symbol	Min.	Typ.	Max.	Unit
Clock	CLK Frequency	fclk	44.4	44.8	45.25	M Hz
		-	22.1	22.3	22.5	ns
Hsync	Cycle Time	th	(TBD)	1024	1074	DCLK
	Display Data	thd	960	960	960	
	Pulse Width	thp	5	16	46	
	Pulse Width	thb	2	28	43	
	Front Porch	thf	16	20	25	
	Horizontal "L" width +back porch	thd+thp	39	44	48	
	Horizontal total porch	thd+thp+thf	64	64	64	
Vsync	Cycle Time	tv	728	729	735	Line
	Display Line	tvd	720	720	720	
	Pulse Width	tvp	1	2	5	
	Pulse Width	tvb	1	4	5	
	Front Porch	tvf	3	3	5	
	Vertical "L" period +back porch	tvp+tvb	4	6	5	
	Vertical active area	tvp+tvb+tvf	9	9	9	
	Frame Frequency	f_{Frame}	56.2	60	60.69	Hz

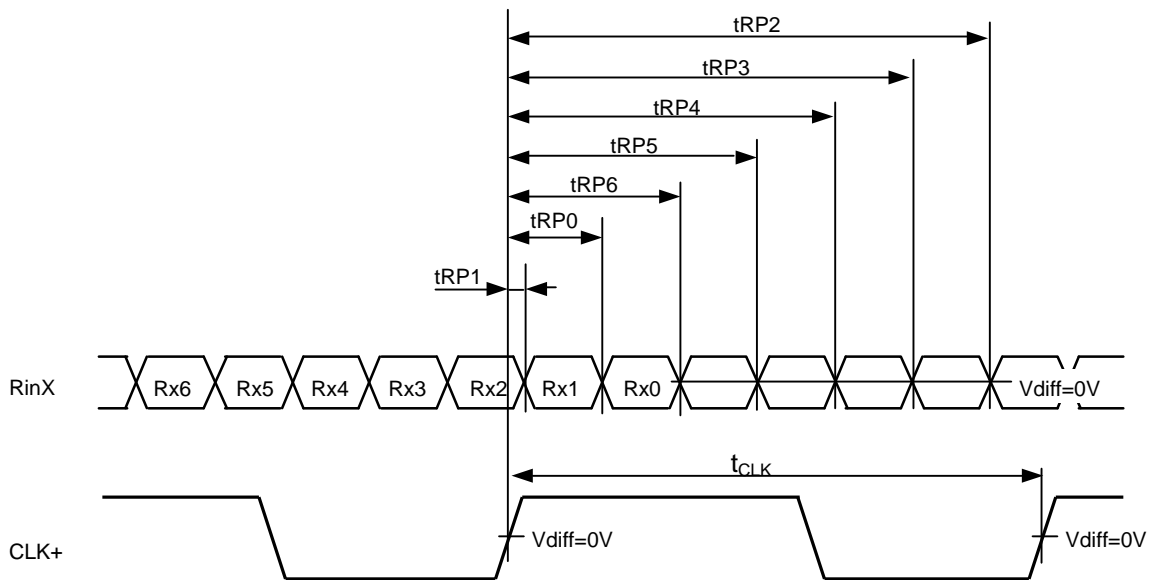
Note 1: For 2-port input, horizontal display period has the notation of the half of 1920.

8.3 LVDS Sequence

LVDS data format



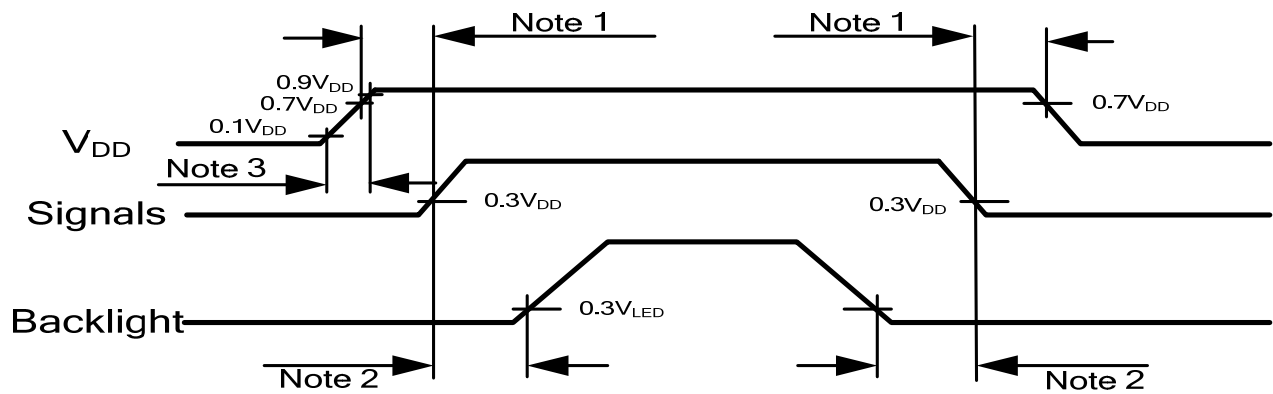
DE: Display Enable, VS: Vertical Signal, HS: Horizontal Signal, NA: Not Available



$$R_{inX} = (R_{inX+}) - (R_{inX-}) \quad (X=0, 1, 2, 3)$$

Item	Symbol	Min.	Typ.	Max.	Unit	
CLK	Cycle frequency	$1/t_{CLK}$	44.4	44.8	45.2	MHz
RinX (X=0,1,2,3)	0 data position	t_{RP0}	$1/7 * t_{CLK} - 0.3$	$1/7 * t_{CLK}$	$1/7 * t_{CLK} + 0.3$	ns
	1st data position	t_{RP1}	-0.3	0	+0.3	
	2nd data position	t_{RP2}	$6/7 * t_{CLK} - 0.3$	$6/7 * t_{CLK}$	$6/7 * t_{CLK} + 0.3$	
	3rd data position	t_{RP3}	$5/7 * t_{CLK} - 0.3$	$5/7 * t_{CLK}$	$5/7 * t_{CLK} + 0.3$	
	4th data position	t_{RP4}	$4/7 * t_{CLK} - 0.3$	$4/7 * t_{CLK}$	$4/7 * t_{CLK} + 0.3$	
	5th data position	t_{RP5}	$3/7 * t_{CLK} - 0.3$	$3/7 * t_{CLK}$	$3/7 * t_{CLK} + 0.3$	
	6th data position	t_{RP6}	$2/7 * t_{CLK} - 0.3$	$2/7 * t_{CLK}$	$2/7 * t_{CLK} + 0.3$	

8.4 Power ON/OFF sequence



Note 1: In order to avoid any damages, V_{DD} has to be applied before all other signals. The opposite is true for power off where V_{DD} has to be remained on until all other signals have been switch off. The recommended time period is 1 second.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

Note 3: In order to avoid high Inrush current, V_{DD} rising time need to set more than 0.5ms.

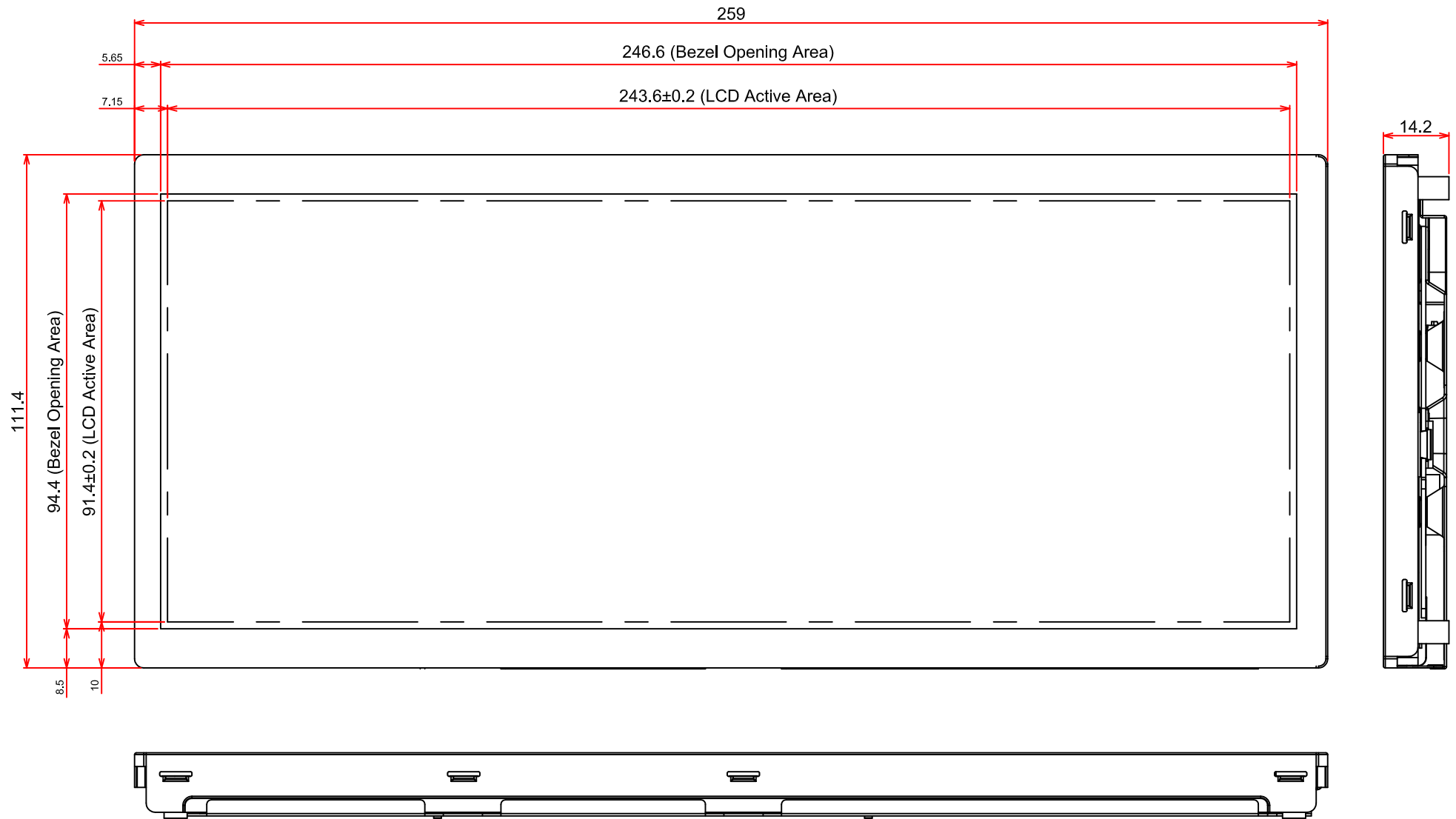
8.5 DATA INPUT for DISPLAY COLOR

Input color		Red Data								Green Data								Blue Data													
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0						
		MSB								LSB								MSB								LSB					
Basic Color	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Red(255)	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Green(255)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L						
	Blue(255)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H						
	Cyan	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H						
	Magenta	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H						
	Yellow	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L						
	White	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H						
Red	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Red(1)	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Red(2)	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	Red(253)	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Red(254)	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Red(255)	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
Green	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Green(1)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L						
	Green(2)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L						
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	Green(253)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L						
	Green(254)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L						
	Green(255)	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L						
Blue	Black	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L						
	Blue(1)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H						
	Blue(2)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L						
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:						
	Blue(253)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	H						
	Blue(254)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L						
	Blue(255)	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H						

Note 1: Color (n) --- 'n' indicates gray scale step.

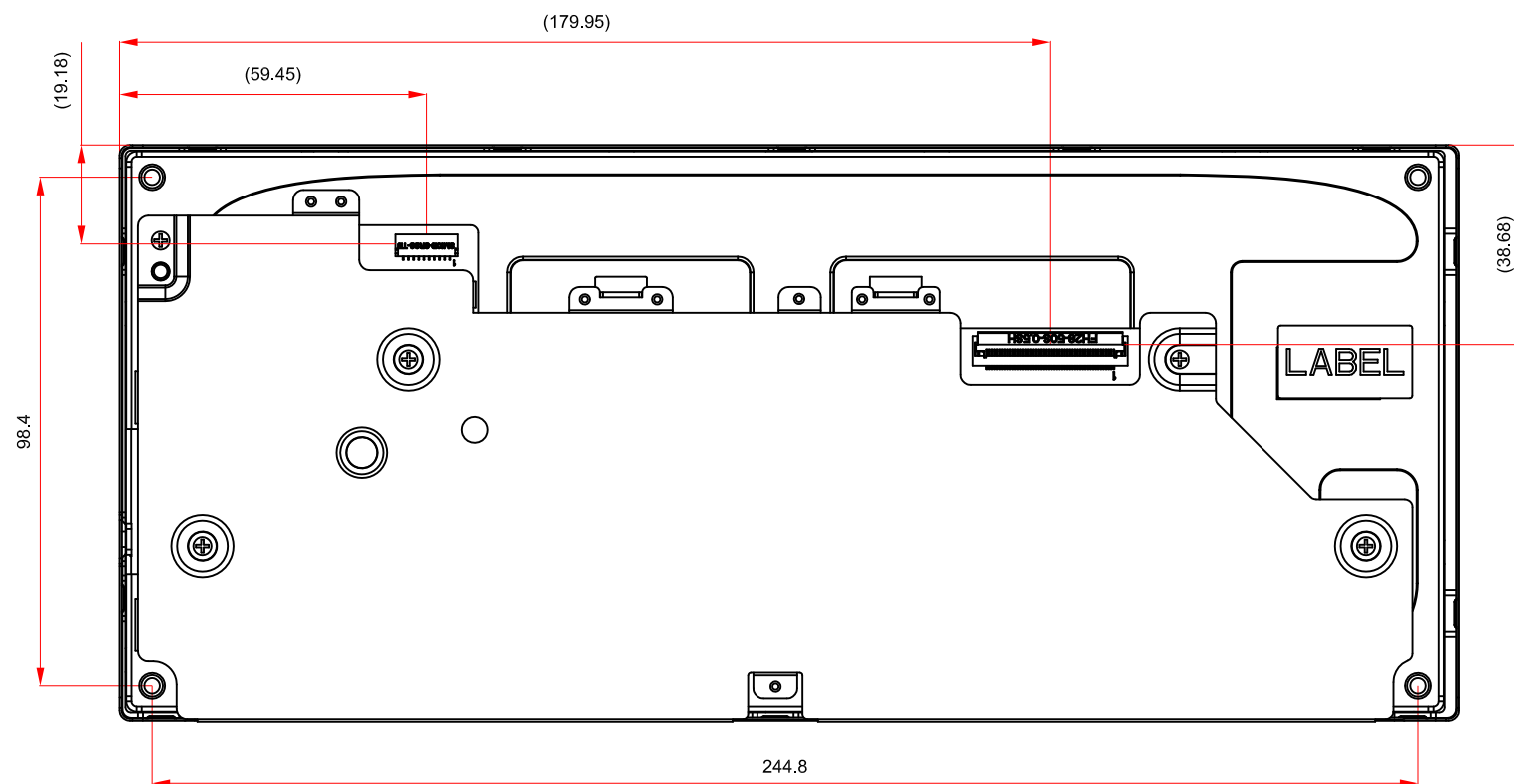
9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



General Tolerance ±0.5mm
Scale : NTS
Unit : mm

9.2 REAR VIEW



General Tolerance ± 0.5
Scale : NTS
Unit : mm

10. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.10.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.

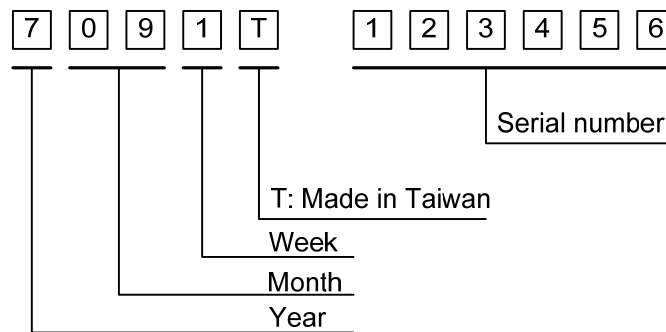


Fig. 10.1

2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark
2017	7
2018	8
2019	9
2020	0
2021	1

Month	Lot Mark	Month	Lot Mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week	Lot Mark
1~7 days	1
8~14 days	2
15~21 days	3
22~28 days	4
29~31 days	5

3) The location of the lot mark is on the back of the display shown in Fig. 10.2

Label example:

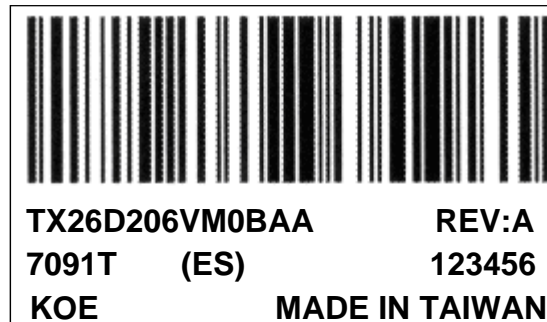


Fig. 10.2

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DATA MODUL AG
Landsberger Straße 322
DE-80687 Munich
Phone: +49-89-56017-0

DATA MODUL WEIKERSHEIM GMBH
Lindenstraße 8
DE-97990 Weikersheim
Phone: +49-7934-101-0



More information and worldwide locations can be found at

www.data-modul.com