DATA MODUL

SPECIFICATION

ED100UC1 VB3300-KOA

10”, 1200x1600

Version: 1.0
Date: 29.04.2020

Note: This specification is subject to change without prior notice

www.data-modul.com

Version: 1.0

Technical Specification

MODEL NO: VB3300-KOA (ED100UC1)

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

Approved By _____

Confirmed By _____

Prepared By _____

Revision History

Rev.	Issued Date	Revised Contents
0.1	2020-03-20	Tentative SPEC V0.1
0.2	2020-03-27	Revised typo and RA criteria(Package Drop Impact)
1.0	2020-04-29	Formal SPEC(Update the formats and contents)

TECHNICAL SPECIFICATION

CONTENTS

1. General Description

VB3300-KOA(ED100UC1) is a reflective electrophoretic E Ink® and Glass-type display module based on active matrix TFT substrate. It has 10” active area with 1200 x 1600 pixels, the display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

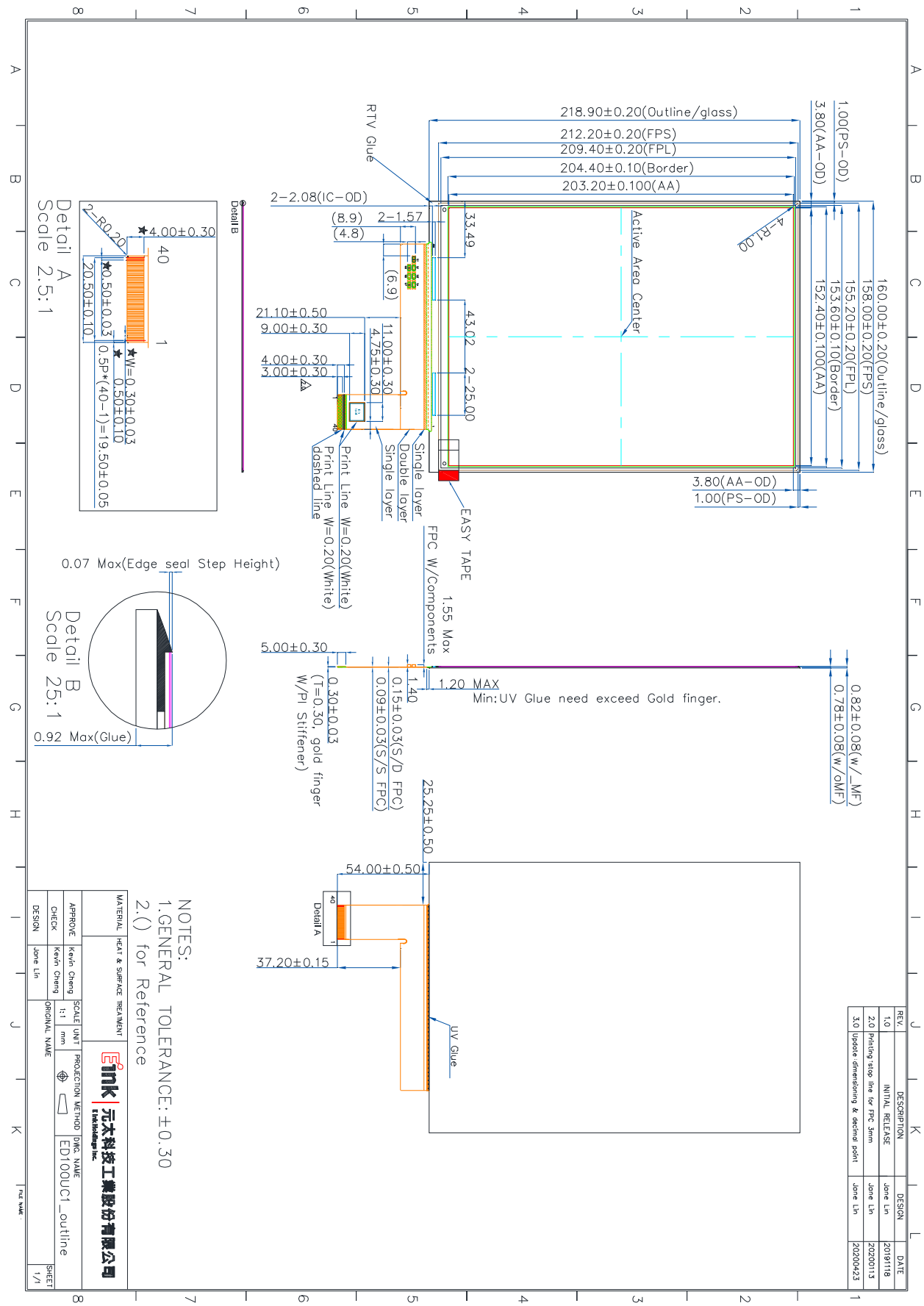
2. Feature

- High contrast reflective/electrophoretic technology
- Glass-type display
- EPD module only, no other structure
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Portrait(Landscape) mode

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	10 (3 : 4)	Inch	
Display Resolution	1200(H) x 1600(V)	Pixel	
Active Area	152.4(H) x 203.2(V)	mm	
Pixel Pitch	0.127(H) x 0.127(V)	mm	Square
Outline Dimension	160 (H) x 218.9(V) x 0.78(D)	mm	
Module Weight	55	g	±7%
Number of Gray	16 Gray Level (monochrome)		

4. Mechanical Drawing of EPD Module



5. Input/Output Interface

5-1) Recommended Connector Type of Panel

P-TWO 196033-40041

5-2) Pin Assignment of Panel

Pin #	Signal	I/O	Description	Remark
1	VGL	P	Negative voltage of gate driver	Note2
2	NC	-	NO Connection	
3	VGH	P	Positive voltage of gate driver	Note2
4	NC	-	NO Connection	
5	VDD	P	Digital voltage of source driver and gate driver	Note2
6	OEV	I	Output enable of gate driver	
7	CKV	I	Clock of gate driver	
8	SPV	I	Start pulse of gate driver	
9	VSS	P	Ground	Note2
10	VCOM	P	Common voltage	Note2
11	VDD	P	Digital power supply drivers	Note2
12	VSS	P	Ground	Note2
13	CKH	I	Clock of source driver	
14	D0	I	Data signal source driver	
15	D1	I	Data signal source driver	
16	D2	I	Data signal source driver	
17	D3	I	Data signal source driver	
18	D4	I	Data signal source driver	
19	D5	I	Data signal source driver	
20	D6	I	Data signal source driver	
21	D7	I	Data signal source driver	
22	VSS	P	Ground	Note2
23	D8	I	Data signal source driver	
24	D9	I	Data signal source driver	
25	D10	I	Data signal source driver	
26	D11	I	Data signal source driver	
27	D12	I	Data signal source driver	
28	D13	I	Data signal source driver	
29	D14	I	Data signal source driver	
30	D15	I	Data signal source driver	
31	SPH	I	Start pulse of source driver	
32	LEH	I	Latch enable of source driver	
33	OEH	I	Output enable of source driver	

34	TEST	-	Test pin of E Ink	Note1
35	NC	-	NO Connection	
36	VSH	P	Positive voltage of source driver	Note2
37	NC	-	NO Connection	
38	VSL	P	Negative voltage of source driver	Note2
39	NC	-	NO Connection	
40	Border	I	Border connection	

Note1: Please connect to VDD pin.
Note2: P → Power pin

5-3) Panel Scan Directions

5-4)The relationship of input data and output

Output	S1	S2	S3	S4	S5	S6	S7	S8
Data	D15	D13	D11	D9	D7	D5	D3	D1
	D14	D12	D10	D8	D6	D4	D2	D0

6. Electrical Characteristics

6-1) Absolute Maximum Ratings of panel only:

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5	V	--
Positive Supply Voltage	VSH	-0.3 to +18	V	--
Negative Supply Voltage	VSL	+0.3 to -18	V	--
Max .Drive Voltage Range	VSH – VSL	36	V	--
Supply Voltage	VGH	-0.3 to VGL+50	V	--
Supply Voltage	VGL	-25.0 to +0.3	V	--
Supply Range	VGH-VGL	10 to +45	V	--
Operating Temp. Range	TOTR	0 to +50	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

6-2) Panel DC Characteristics (Note. 1)

Parameter	Symbol	Conditions	Min	Typ**(Note 3)**	Max**(Note 2)**	Unit
Signal ground	VSS		-	0	-	V
Logic Voltage supply	VDD		1.7	1.8	2.1	V
	I_{VDD}	VDD=1.8V	-	6.32	8.36	mA
	VDD		3	3.3	3.6	V
	I_{VDD}	VDD=3.3V	-	6.32	8.36	mA
Gate Negative supply	VGL		-21	-20	-19	V
	I_{GL}	VGL = -20V	-	5.56	17.62	mA
Gate Positive supply	VGH		27	28	29	V
	I_{GH}	VGH = 28V	-	2.63	4.32	mA
Source Negative supply	VSL		-15.4	-15	-14.6	V
	I_{SL}	VSL = -15V	-	5.51	192.96	mA
Source Positive supply	VSH		14.6	15	15.4	V
	I_{SH}	VSH = 15V	-	5.32	202.56	mA
Border supply	V_{COM}		-4	Adjusted	-0.3	V
Asymmetry source	V_{Asym}	VSH+VSL	-800	0	800	mV
Common voltage	VCOM		-4	Adjusted	-0.3	V
	I_{COM}		-	6.74	7.87	mA
Panel Power	P		-	368.15	6616.4	mW
Standby power panel **(Note 4)**	P_{STBY}		-	-	10.68	mW

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents **(Note 5)**	I_{SH}	VSH = 15V	-		441.6	mA
	I_{SL}	VSL = -15V	-		451.2	mA
	I_{GH}	VGH = 28V	-		41.28	mA
	I_{GL}	VGL =-20V	-		211.2	mA
	I_{COM}	--	-		480	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input “H” voltage	VIH	--	0.8VDD		VDD	V
Digital Input “L” voltage	VIL	--	GND		0.2VDD	V

Note :

1. The power consumption in this field is provided for the purpose as the follows:

1-1. The selection of suitable PMIC in the market to drive EPD normally.

1-2. Estimation of voltage-drop at input side of PMIC for setting of threshold-voltage of battery.

2. The maximum average Currents for power consumption are measured using 85 Hz waveform with following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)

3. The Typical average current for power consumption is measured using 85 Hz waveform with following pattern transition:

3-1. For displaying with grayscale image, it is from horizontal 4 gray scale pattern to vertical 4 gray scale pattern without dithering process. (Note 6-2)

4. The standby power is the consumed power when the panel controller is in standby mode.

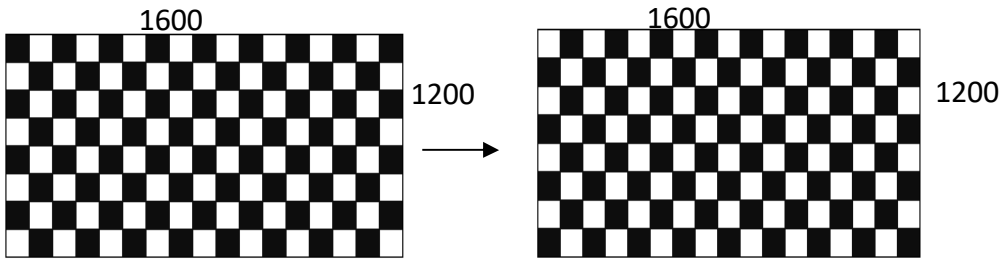
5. The Maximum Currents are measured using 85 Hz waveform with following pattern transition in both B/W from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.

6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.

7. Vcom is recommended to be set in the range of assigned value ± 0.1 V

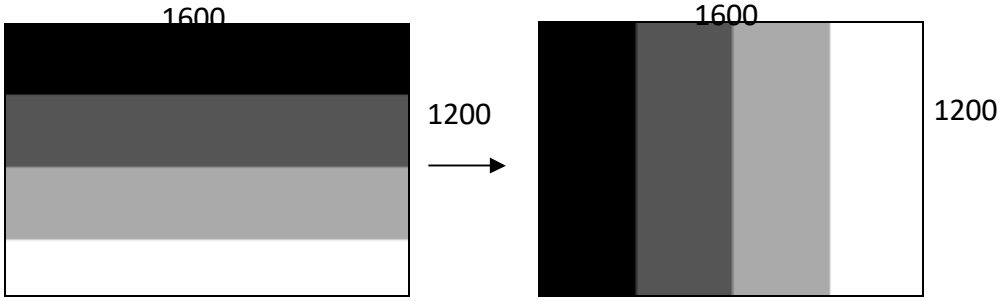
Note6-1

The maximum average current and Maximum Currents for B/W display



Note6-2

The typical power consumption for B/W display



Note6-3

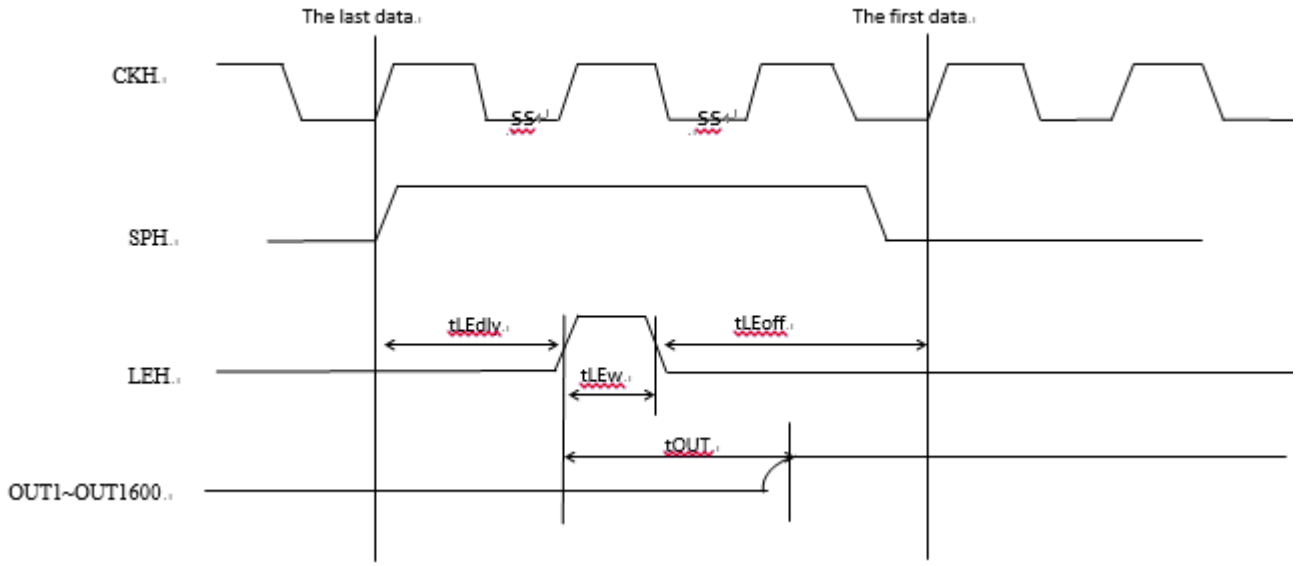
The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
ISH	4.7uF /25Vx 2pcs / ±10%
ISL	4.7uF /25Vx 2pcs / ±10%
IGH	2.2 uF /50Vx 1 pcs / ±10%
IGL	4.7uF /25Vx 1 pcs / ±10%
IDD	4.7uF /25Vx 1 pcs / ±10%

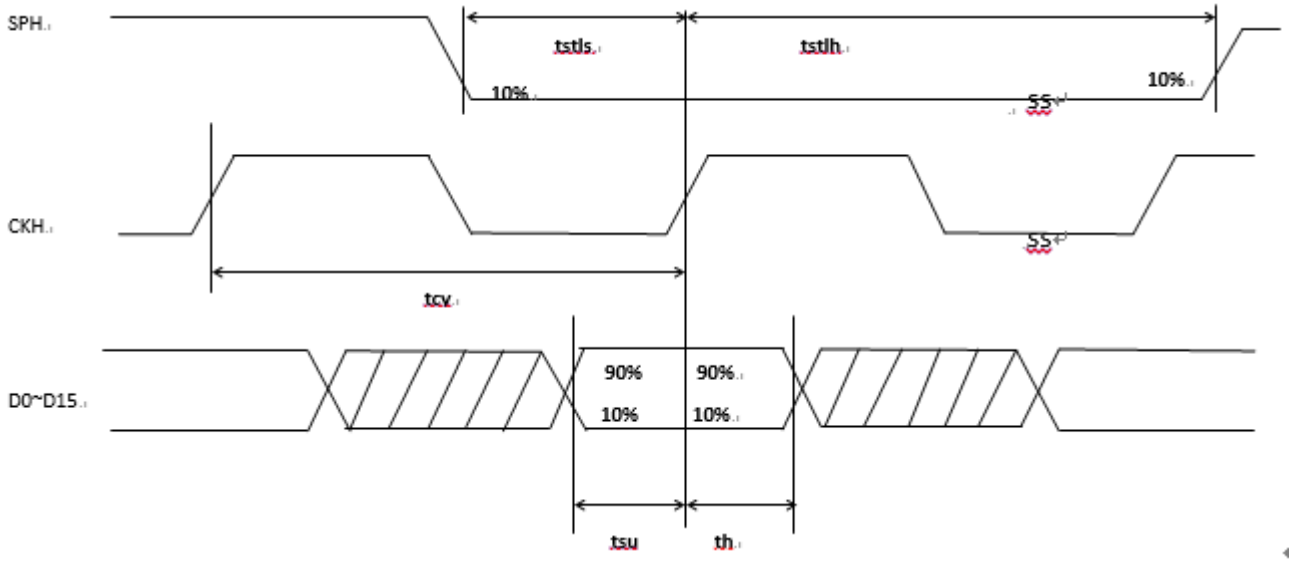
6-3) Panel AC characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum "L" clock pulse width (for VDD=1.8V)	twL	1000	-	-	ns
Minimum "H" clock pulse width (for VDD=1.8V)	twH	1000	-	-	ns
Minimum "L" clock pulse width (for VDD=3.3V)	twL	500			ns
Minimum "H" clock pulse width (for VDD=3.3V)	twH	500			ns
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock CKH cycle time (for VDD=1.8V)	tcy	20.83	-	-	ns
Clock CKH cycle time (for VDD=3.3V)	tcy	16.67	-	-	ns
D0 .. D15 setup time (for VDD=1.8V)	tsu	10	-	-	ns
D0 .. D15 setup time (for VDD=3.3V)	tsu	8	-	-	ns
D0 .. D15 hold time (for VDD=1.8V)	th	10	-	-	ns
D0 .. D15 hold time (for VDD=3.3V)	th	8	-	-	ns
SPH setup time	tstls	0.5* tcy	-	0.8* tcy	ns
SPH hold time	tstlh	0.5* tcy	-		ns
LEH on delay time (for VDD=1.8V)	tLEdly	10.5* tcy	-	-	ns
LEH on delay time (for VDD=3.3V)	tLEdly	10.5* tcy	-	-	ns
LEH high-level pulse width (When VDD=1.7V to 2.5V)	tLEw	300	-	-	ns
LEH high-level pulse width (When VDD=2.5V to 3.6V)	tLEw	300	-	-	ns
LEH off delay time (for VDD=1.8V)	tLEoff	200	-	-	ns
LEH off delay time (for VDD=3.3V)	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	20	us

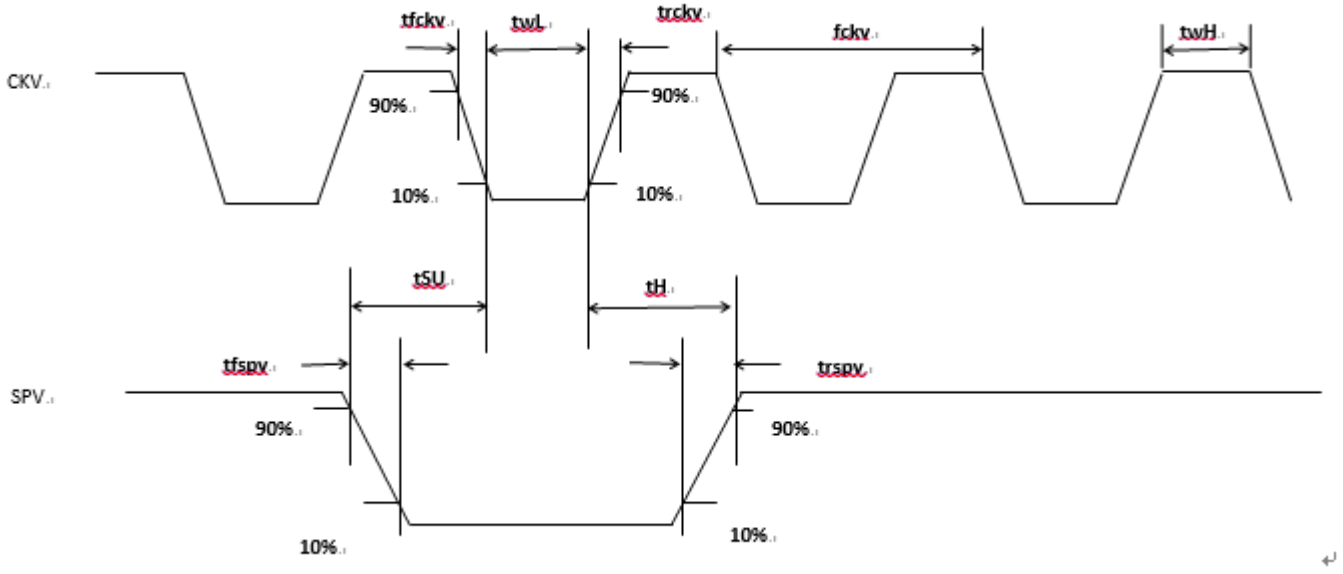
OUTPUT LATCH CONTROL SIGNALS



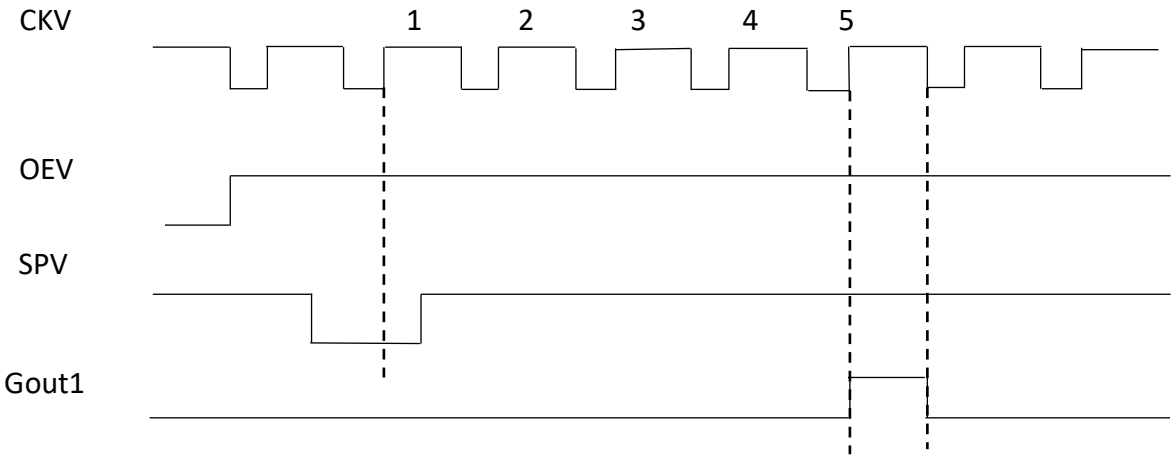
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note：The 1st Gate line(Gout1) is output based on above timing of "GATE OUTPUT TIMING".

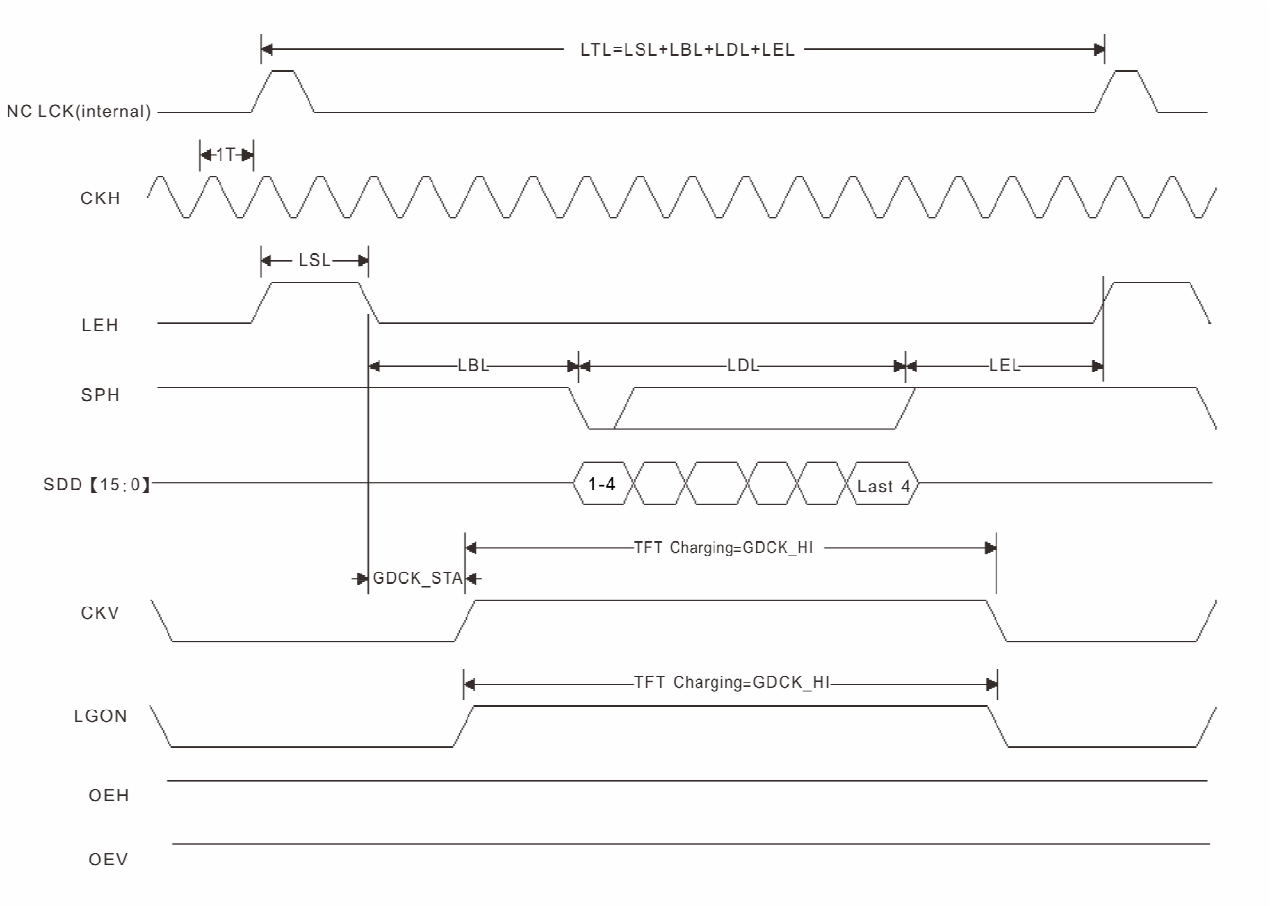
6-4) Refresh Rate

The module applied at a maximum refresh rate of 85 Hz.

	Min	Max
Refresh Rate	-	85 Hz

6-5) Controller Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (OEH) and Gate Driver Clock (CKV). Note, that in this mode LGON follows CKV timing



Note: LCK is an internal signal and it is shown for reference only

Figure 1

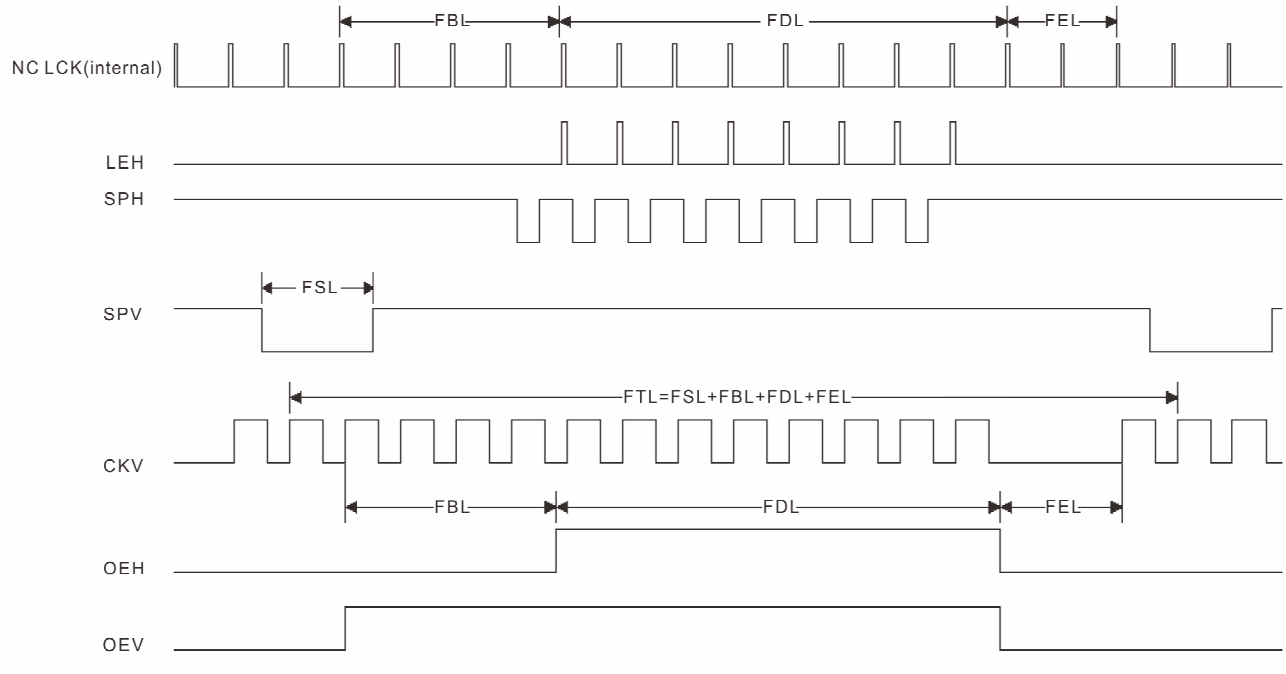


Figure 2

Timing Parameters Table

Mode	3	Resolution 1600x1200				
CKH【MHz】	30.00					
Pixels Per CKH	8					
Line Parameters【CKH】	LSL	LBL	LDL	LEL	GDCK _STA	LGONL
	10	7	200	73	15	243
Line Parameters【us】	-	-	-	-	-	-
	0.33	0.23	6.67	2.43	0.50	8.10
Frame Parameters【lines】	FSL	FBL	FDL	FEL	-	FR【Hz】
	1	4	1200	12	-	85
Frame Parameters【us】					-	-
	9.67	38.67	11600.00	116.00	-	-

Note:

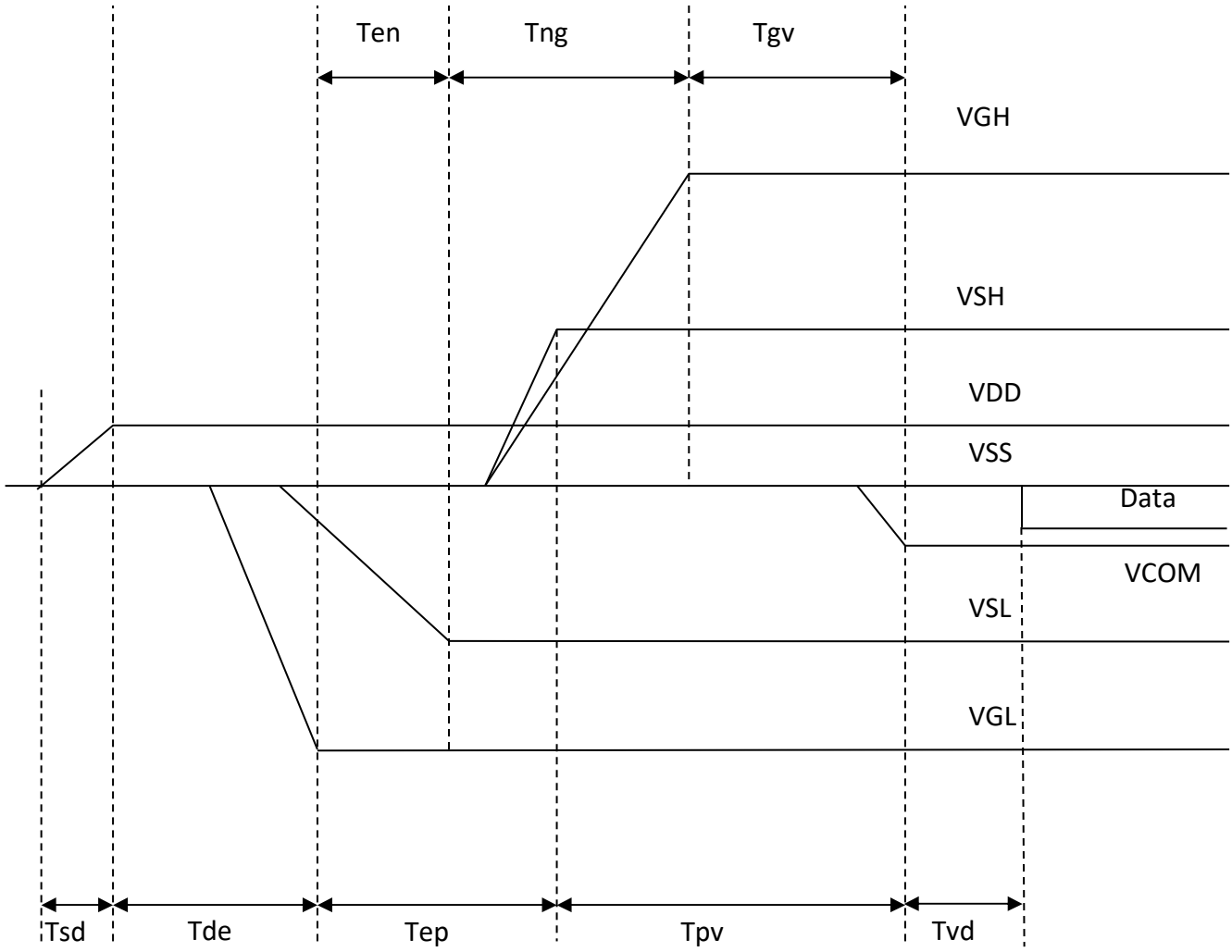
1. For parameters definition, see above Figure 1 and Figure 2.
2. For NXP SoC OEV Low pulse represent FSL and SPV pulses with the first period of FBL
3. The mapping of pins between controller timing and pin-assignment of panel:

7. Power Sequence

Power Rails must be sequenced in the following order：

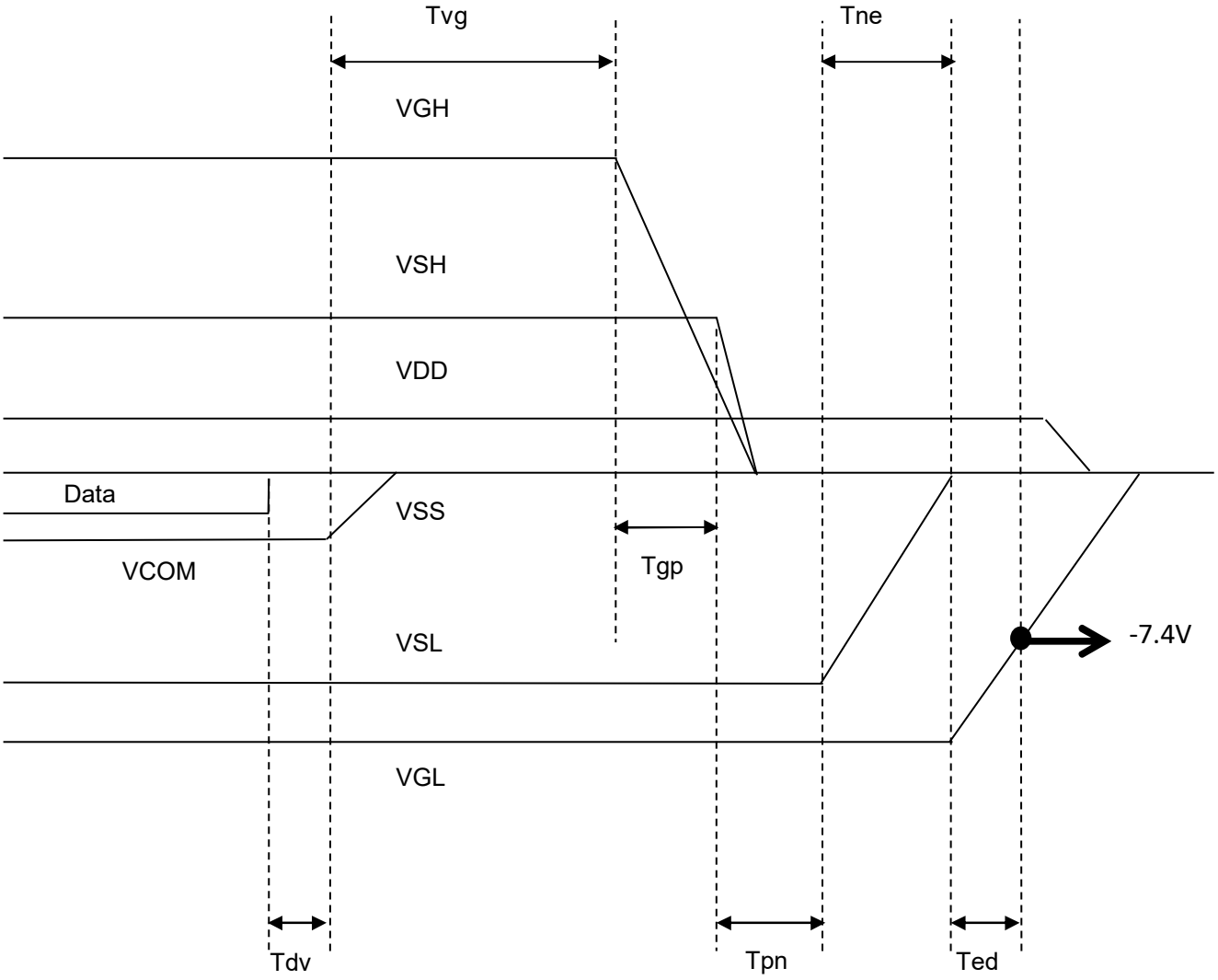
1. VSS → VDD → VSL → VSH (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

POWER ON



	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-
Tgv	100us	-

POWER OFF



	Min	Max	Remark
Tdv	100µs	-	-
Tvg	0µs	-	-
Tgp	0µs	-	-
Tpn	0µs	-	-
Tne	0µs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note:

1. Supply voltages decay through pull-down resistors.
2. VGL must remain negative of Vcom during decay period.

8. Optical characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

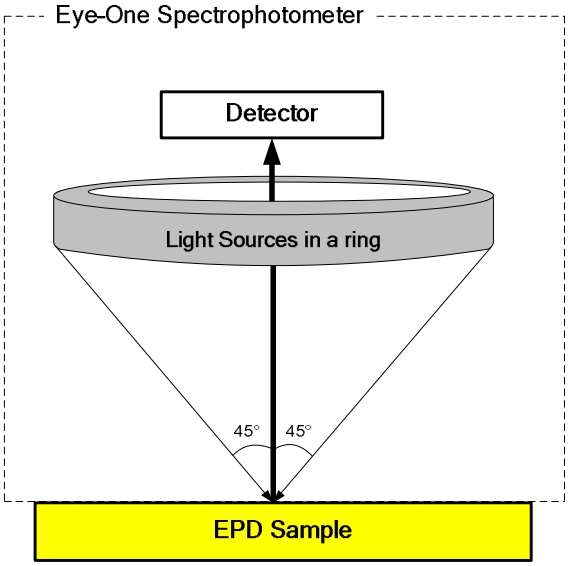
T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	35	45	-	%	Note 8-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)× n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	16	-		-

WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS
m:4、8、16 when 2、3、4 bits mode
Note 8-1: Luminance meter :Eye – One Pro Spectrophotometer.

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl / Rd



8-3) Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements and Remark

Warning
The Mobius display may damage when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains preliminary product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information
Where application information is given, it is advisory and does not form part of the specification.

Remark
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

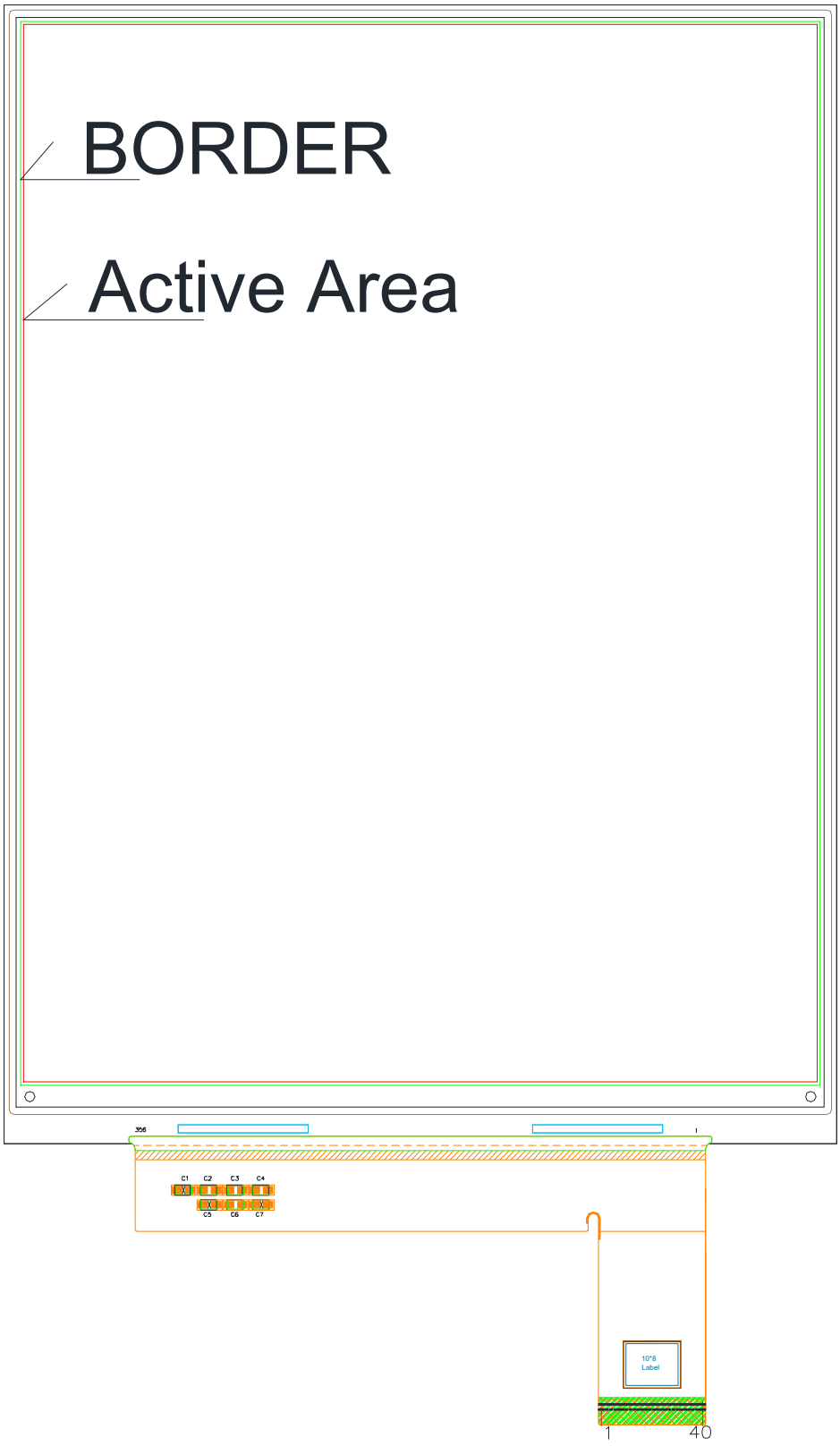
10. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Be	--
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-1Ae	--
3	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-78	
4	Low-Temperature Storage	T = -25°C for 240 hrs (Test in white pattern)	IEC 60 068-2-1Ab	
5	High Temperature High Humidity Storage	T=+60C RH=80% for 240hrs (Test in White Pattern)	IEC 60 068-2-78	
6	High Temperature Storage	T=+70C RH=40% for 240hrs (Test in White Pattern)	IEC 60 068-2-2 Bb	--
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min (Test in white pattern)	IEC 60 068-2-14Nb	--
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ (Test in white pattern)	IEC 60068-2-5Sa	--
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	--
10	Package Drop Impact	Drop from height of 100 cm on concrete surface. Drop sequence: 1 corner,3 edges,6 faces One drop for each.	Full packed for shipment	--
11	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179 IEC 62180	--

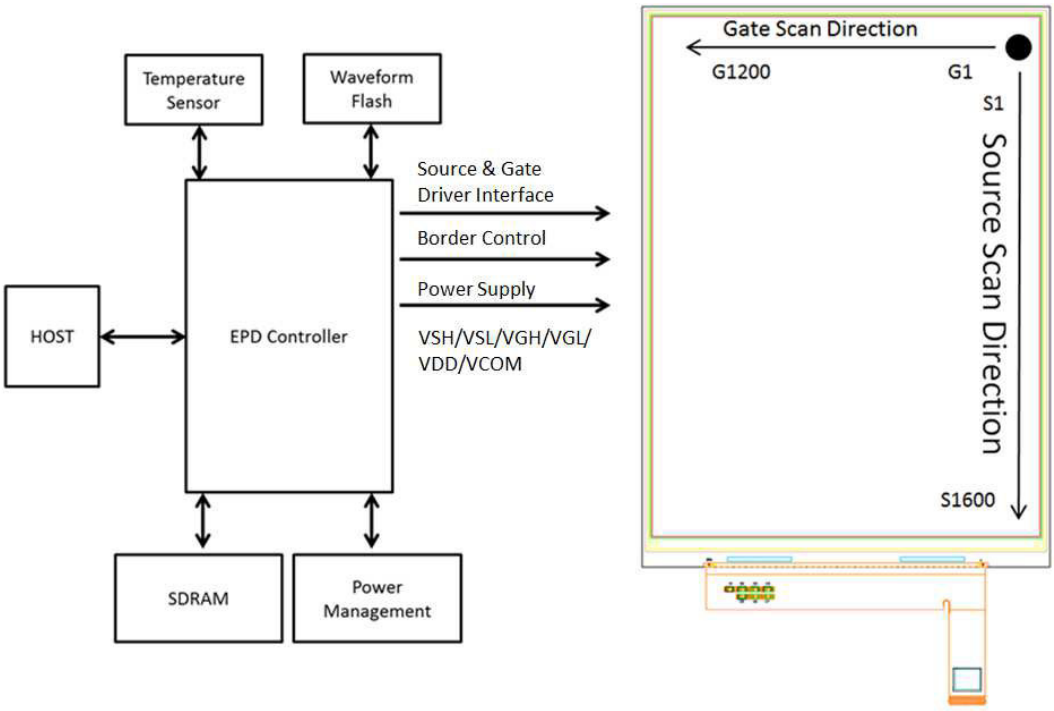
[Criteria]

In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

11. Border definition

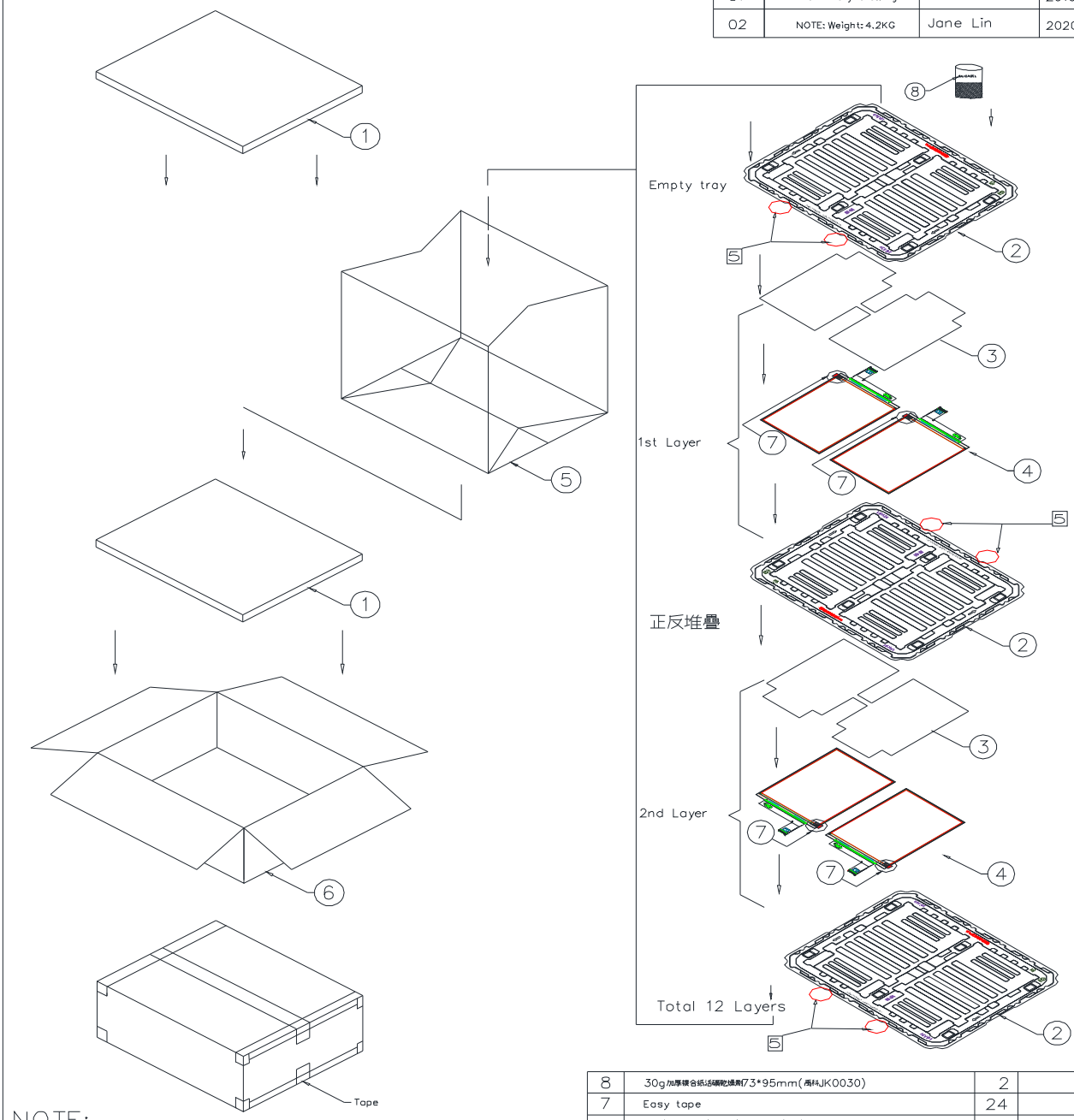


12. Block Diagram



13. Packing

REV	DESCRIPTION	DESIGN	DATE
01	Preliminary drawing	Jane Lin	20191127
02	NOTE: Weight: 4.2KG	Jane Lin	20200424



NOTE:

1. One layer include: 1 piece of cushion sheet, 2 pcs module & 1 piece of tray.
2. Q'TY: 24 pcs panel/carton.
3. Dimension: 455*375*190mm
4. Weight: 4.2KG
5. Tray 180°堆疊, 堆疊後可從側邊檢視圓弧防呆方向是否正確

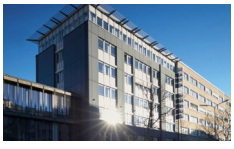
ITEM	DESCRIPTION	QTY	REMARK
8	30g加厚鑽合紙活磷乾燥劑73*95mm(商科JK0030)	2	
7	Easy tape	24	
6	CARTON INTERNAL	1	
5	摺口袋450*380*700mm	1	抗靜電
4	ED100UC1	24	
3	EPE CUSHION SHEET	12	抗靜電
2	TRAY	13	抗靜電
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.

APPROVE	Kevin Cheng	UNIT	SHEET	DWG. TITLE	
CHECK	Jane Lin	mm	1 OF 1	ED100UC1 Packing Draw	A4 SIZE
DESIGN	Jane Lin				

DATA MODUL

ALL TECHNOLOGIES. ALL COMPETENCIES. ONE SPECIALIST.



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