DATA MODUL

SPECIFICATION

ED113TC1

11.3”, 2400x1034

Version: 2.0
Date: 15.03.2018

Note: This specification is subject to change without prior notice

www.data-modul.com

Version: 2.0

TECHNICAL SPECIFICATION

MODEL NO: ED113TC1

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

☐ Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

Approved By _____

Confirmed By _____

Prepared By _____

Revision History

Rev.	Issued Date	Revised Contents
1.0	Dec. 21 2017	Formal version.
2.0	Mar. 15 2018	Modify power on sequence. Modify power off sequence. Remove discharge time sequence.

TECHNICAL SPECIFICATION

CONTENTS

1. General description

11.3” glass is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 11.3” active area with 2400(H) x 1034(V) pixels, the display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

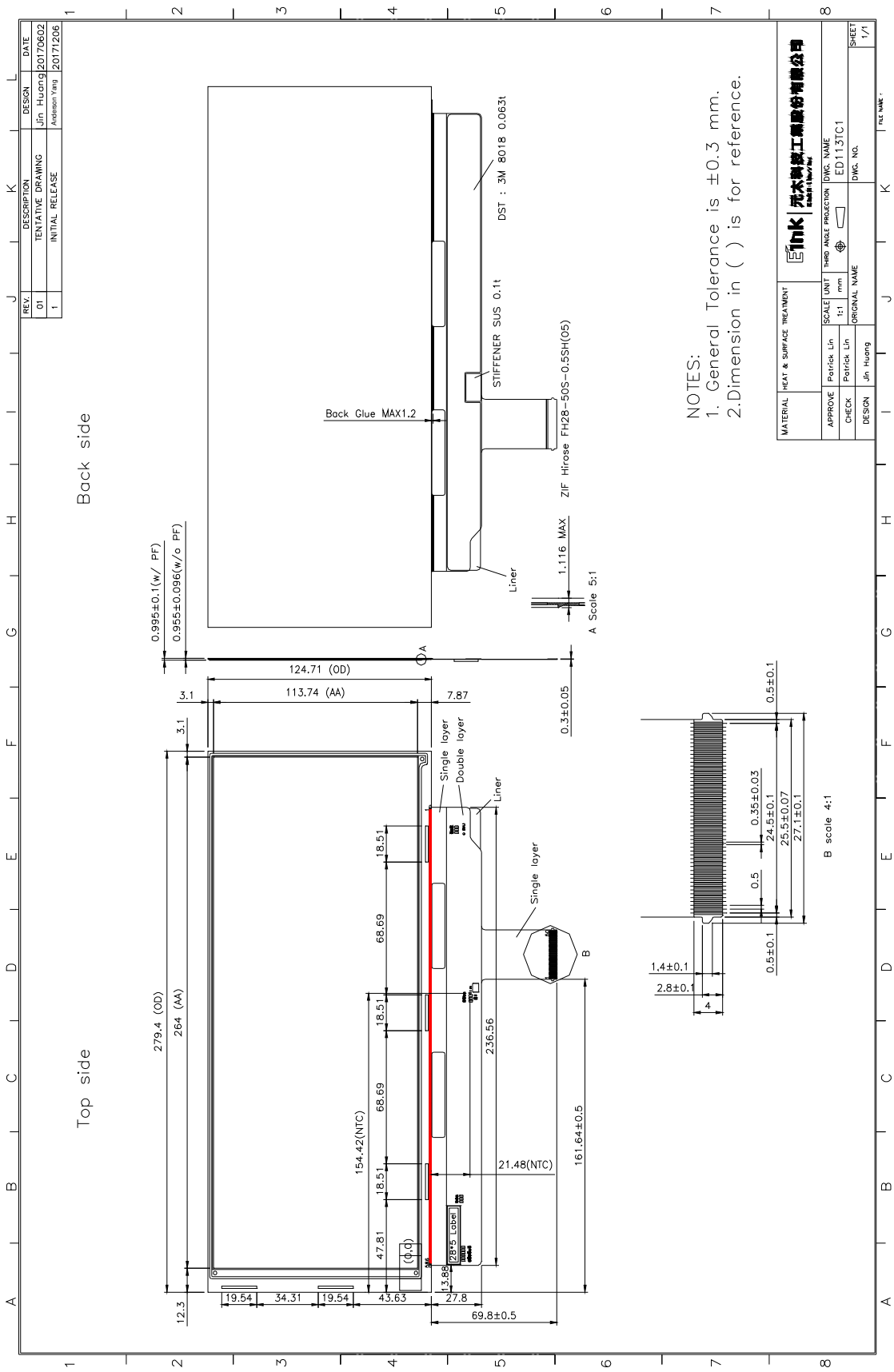
2. Features

- High contrast reflective/electrophoretic technology
- 2400(H) x 1034(V) display
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape
- Antiglare hard-coated front-surface

3. Mechanical specifications

Parameter	Specifications	Unit	Remark
Screen Size	11.3	Inch	
Display Resolution	2400(H) x 1034(V)	Pixel	
Active Area	264.0(H) x 113.74(V)	mm	
Pixel Pitch	0.110(H) x 0.110(V)	mm	
Pixel Configuration	Square		
Outline Dimension	279.4(H) x 124.71(V) × 0.973 (D)	mm	
Module Weight	67	g	Typ
Number of Gray	16 Gray Level (monochrome)		
Display operating mode	Reflective mode		
Surface treatment	Anti-glare treatment for protective sheet		

4.Mechanical drawing of EPD module



5.Input/Ouput Terminals

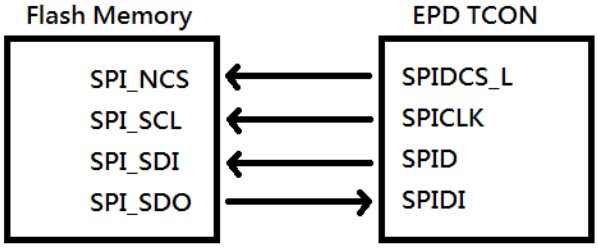
5-1)Pin out list

FPC connector: Hirose FH28-50S-0.5SH(05)

Pin #	Signal	Description	Remark
1	SPI_SDO	Serial Data Output for Flash memory	Note 5-1 Note 5-3
2	SPI_SDI	Serial Data Input for Flash memory	Note 5-1
3	SPI_NCS	Chip Select for Flash memory	Note 5-1
4	SPI_SCL	Serial Data Clock for Flash memory	Note 5-1
5	VDD2	SPI flash power supply	1.8V
6	VSS	Ground	
7	AGND	Thermistor analog Ground	Note 5-4
8	TS	Thermistor sensor pin	Note 5-4
9	MODE	Output mode selection gate driver	
10	TEST	E Ink test ping	Note 5-2
11	CKV	Clock gate driver	
12	SPV	Start pulse gate driver	
13	VSS	Ground	
14	VGH	Positive power supply gate driver	
15	VSS	Ground	
16	VEE	Negative power supply gate driver	
17	VSS	Ground	
18	XOE	Output enable source driver	
19	XLE	Latch enable source driver	
20	XSTL	Start pulse source driver	
21	VSS	Ground	
22	D15	Data signal source driver	
23	D14	Data signal source driver	
24	D13	Data signal source driver	
25	D12	Data signal source driver	
26	D11	Data signal source driver	
27	D10	Data signal source driver	
28	D9	Data signal source driver	
29	D8	Data signal source driver	
30	VSS	Ground	
31	XCL	Clock source driver	
32	VSS	Ground	
33	D7	Data signal source driver	
34	D6	Data signal source driver	
35	D5	Data signal source driver	
36	D4	Data signal source driver	

37	D3	Data signal source driver	
38	D2	Data signal source driver	
39	D1	Data signal source driver	
40	D0	Data signal source driver	
41	VDD	Digital power supply drivers	3.3V
42	VSS	Ground	
43	VNEG	Negative power supply source driver	
44	VNEG	Negative power supply source driver	
45	VSS	Ground	
46	VPOS	Positive power supply source driver	
47	VPOS	Positive power supply source driver	
48	VCOM	Common voltage	
49	VSS	Ground	
50	BORDER	Border connection	

Note 5-1

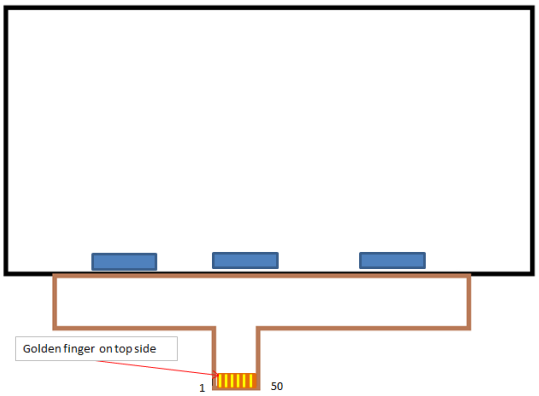


Note 5-2

Please connect to VDD voltage by 10K resistance.

Note 5-3

1st pin direction. (Top side)

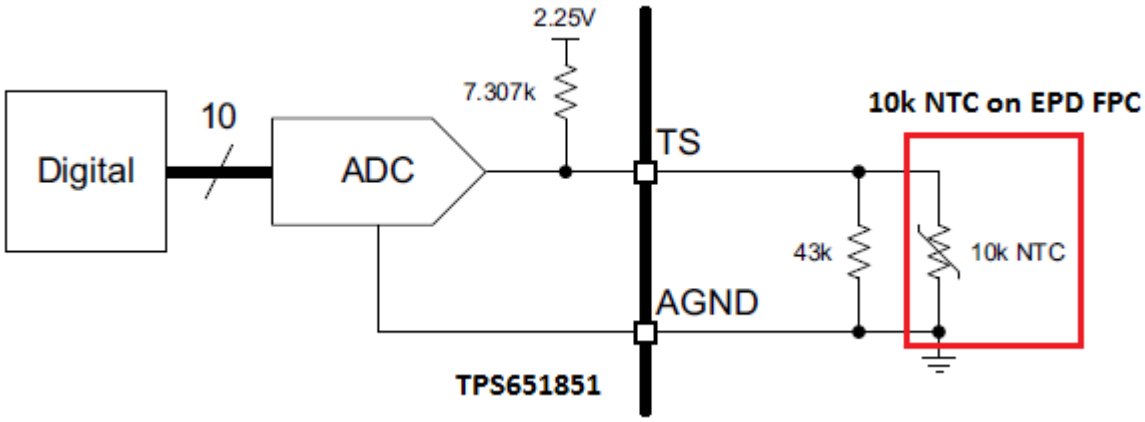


Golden finger on top side.

Note 5-4

TS(NTC) part number: MURATA NCP15XH103F03RC (10KΩ)

Reference circuit for TS & AGND:



6.Electrical Characteristics

6-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VDD	-0.3 to +7	V
SPI Supply Voltage	VDD2	+1.65 to +2.0	V
Positive Supply Voltage	V_{POS}	-0.3 to +18	V
Negative Supply Voltage	V_{NEG}	+0.3 to -18	V
Max .Drive Voltage Range	V_{POS} - V_{NEG}	36	V
Supply Voltage	VGH	-0.3 to +55	V
Supply Voltage	VGL	-32 to +0.3	V
Supply Range	VGH-VGL	-0.3 to +55	V
Operating Temp. Range	TOTR	0 to +50	℃
Storage Temperature	TSTG	-25 to +70	℃

6-2) Panel DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		3.0	3.3	3.6	V
	I_{VDD}	V_{DD}=3.3V	-	3	7	mA
SPI Supply Voltage	V_{DD2}		1.75	1.8	1.85	V
	I_{VDD2}	V_{DD2}=1.8V(Read)			7	mA
Gate Negative supply	VGL		-21	-20	-19	V
	I_{GL}		-	3	3	mA
Gate Positive supply	VGH		24	25	26	V
	I_{GH}		-	3	3	mA
Source Negative supply	V_{NEG}		-15.4	-15	-14.6	V
	I_{NEG}	V_{NEG} = -15V		3	148	mA
Source Positive supply	V_{POS}		14.6	15	15.4	V
	I_{POS}	V_{POS} = 15V		3	143	mA
Border supply	V_{COM}		-4	Adjusted	-0.2	V
Asymmetry source Common voltage	V_{Asym}	VPOS+VNEG	-800	0	800	mV
	V_{COM}		-4	Adjusted	-0.2	V
	I_{COM}		-	1	-	mA
Panel Power	P			235	4524	mW
Standby power panel	P_{STBY}		-	-	0.4	mW

The maximum power consumption is measured using 75 Hz waveform with following pattern transition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 7-1)

The Typical power consumption is measured using 75 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 7-2)

The standby power is the consumed power when the panel controller is in standby mode.

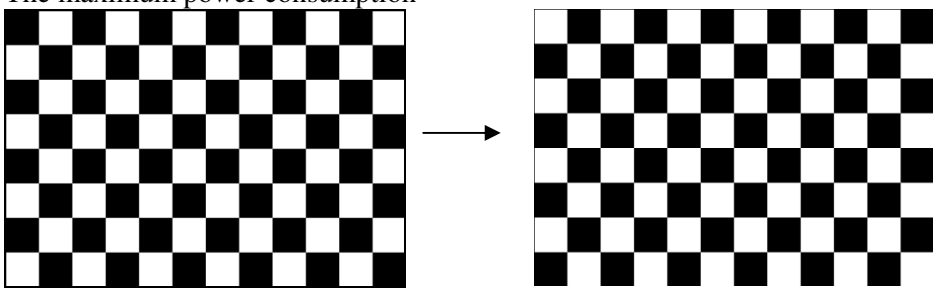
The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink.

Vcom is recommended to be set in the range of assigned value ± 0.1 V

The maximum ICOM inrush current is about 2000 mA

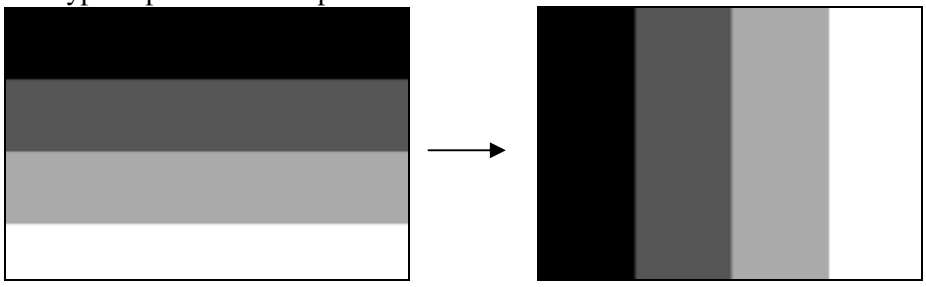
Note6-1

The maximum power consumption



Note6-2

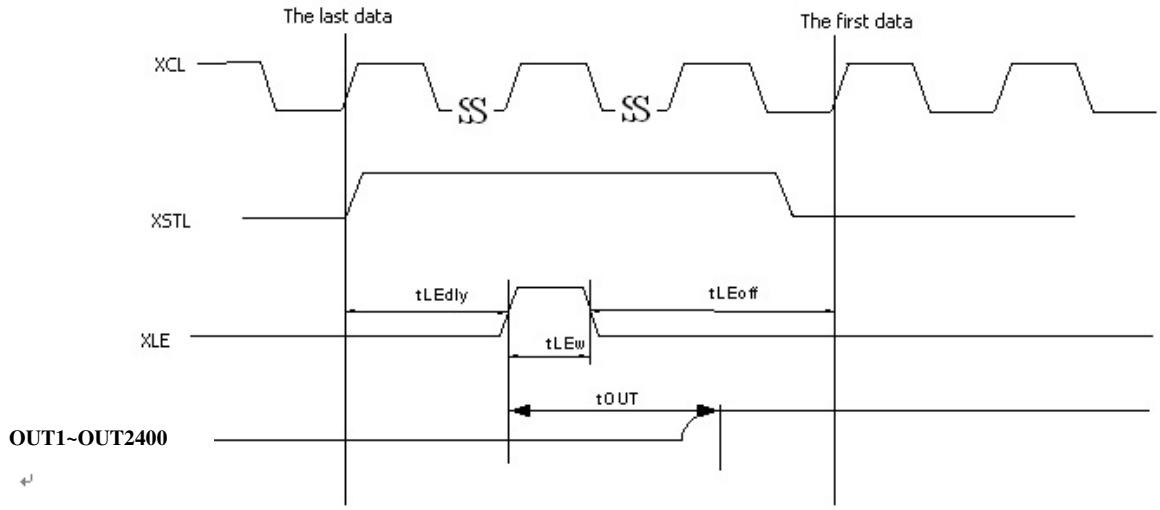
The typical power consumption



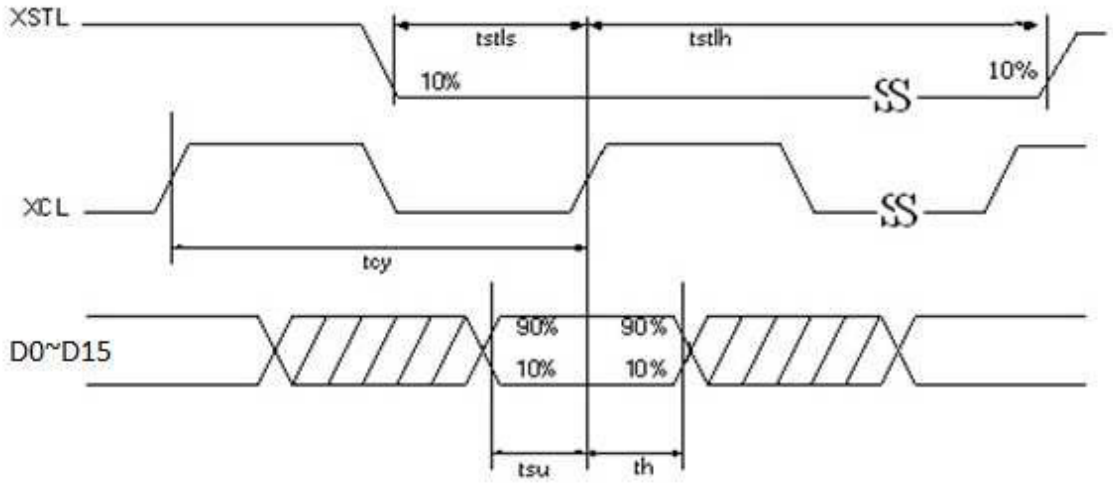
6-3)Panel AC characteristics

VDD=3.0V to 3.6V, unless otherwise specified.

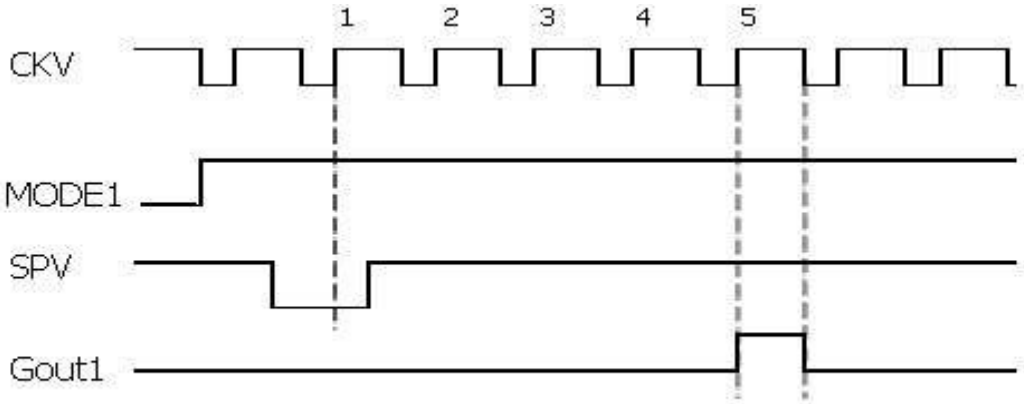
Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum “L” clock pulse width	twL	0.5	-	-	us
Minimum “H” clock pulse width	twH	0.5	-	-	us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns
SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv			100	ns
Pulse fall time	tfspv			100	ns
Clock XCL cycle time	tcy	16.7	20	DC	ns
D0 .. D7 setup time	tsu	8	-	-	ns
D0 .. D7 hold time	th	8	-	-	ns
XSTL setup time	tstls	8	-	-	ns
XSTL hold time	tstlh	8	-	-	ns
XLE on delay time	tLEdly	40	-	-	ns
XLE high-level pulse width	tLEw	40	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	12	us



OUTPUT LATCH CONTROL SIGNALS



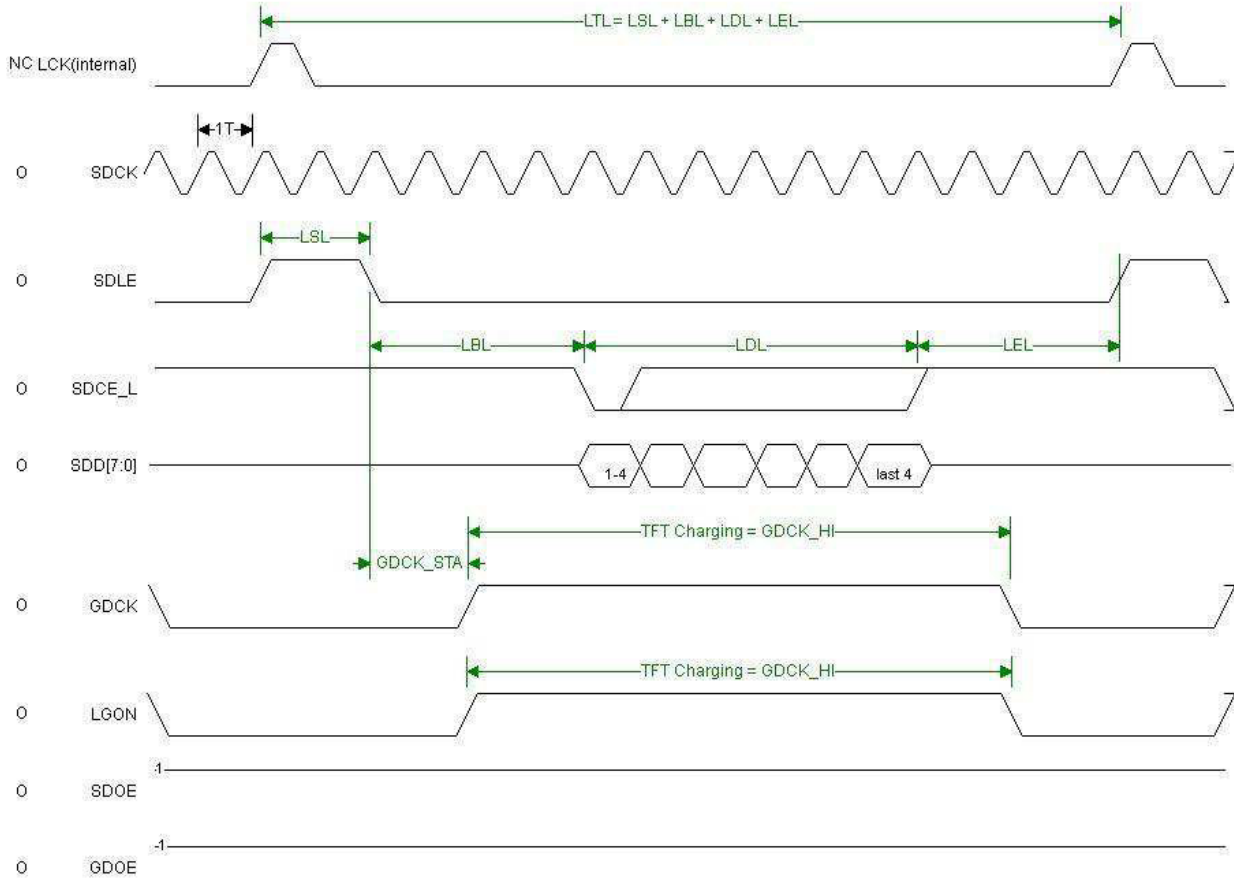
SOURCE CLOCK & DATA TIMING



GATE OUTPUT TIMING
Note: First gate line on timing

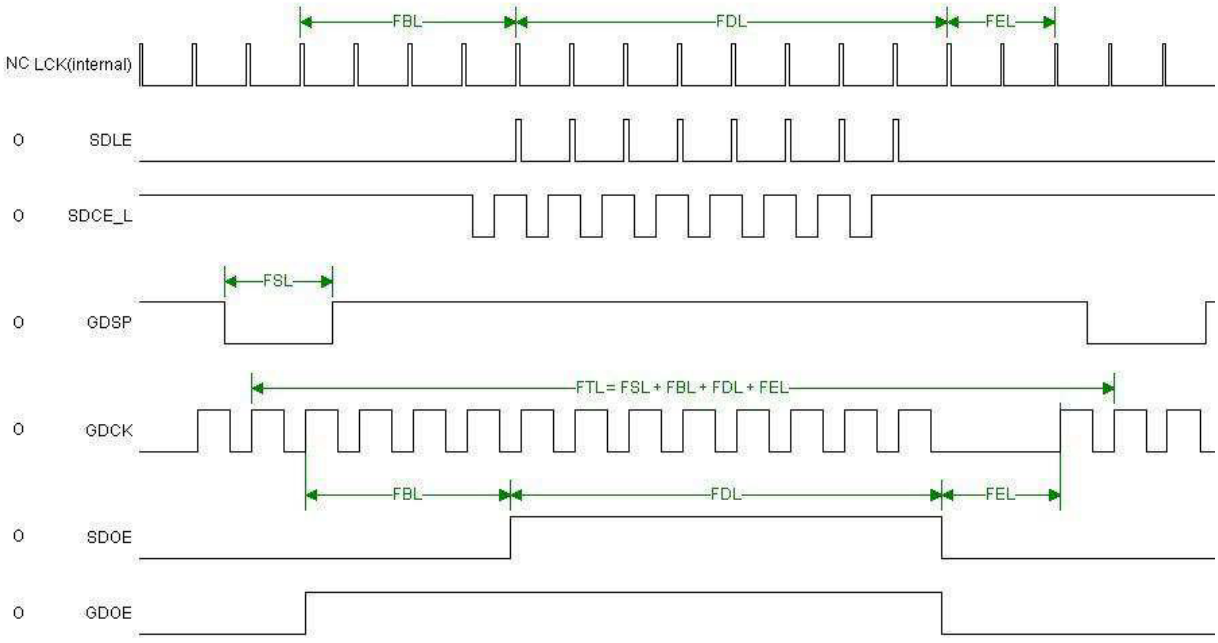
6-4) Controller Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, that in this mode LGON follows GDCK timing



Line Timing in Mode 3

Note: LCK is an internal signal and it is shown for reference only.



Frame Timing in Mode 3

Mode	3	Resolution 2400x1034				
SDCK [MHz]	30					
Pixels Per SDCK	8					
Line Parameters[SDCK]	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
	2	7	300	71	10	256
Line Parameters[us]	-	-	-	-	-	-
	0.07	0.23	10.00	2.37	0.33	8.53
Frame Parameters [lines]	FSL	FBL	FDL	FEL	-	FR [Hz]
	1	4	1034	14	-	74.97
Frame Parameters [us]	-	-	-	-	-	-
	12.67	50.67	13097.33	177.33	-	-

Timing Parameters Table

Note 1 : For parameters definition , see Section 6. Active Matrix Electronic Paper Display Timings

Note 2 : For Isis Controller GDCK_STA and LGONL are not settable parameters ; GDCK_STA=LBL, LGONL=LDL+0.5

Note 3 : For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

Note 4 :

SDCLK = XCL

SDD[7:0] = D0~D15

SDCE_L(in) = XSTL

GDCK = CKV

GDSP = SPV

GDOE = Mode 1

SDOE = XOE

6-5) Refresh rate

	Min	Max
Refresh Rate	-	75Hz

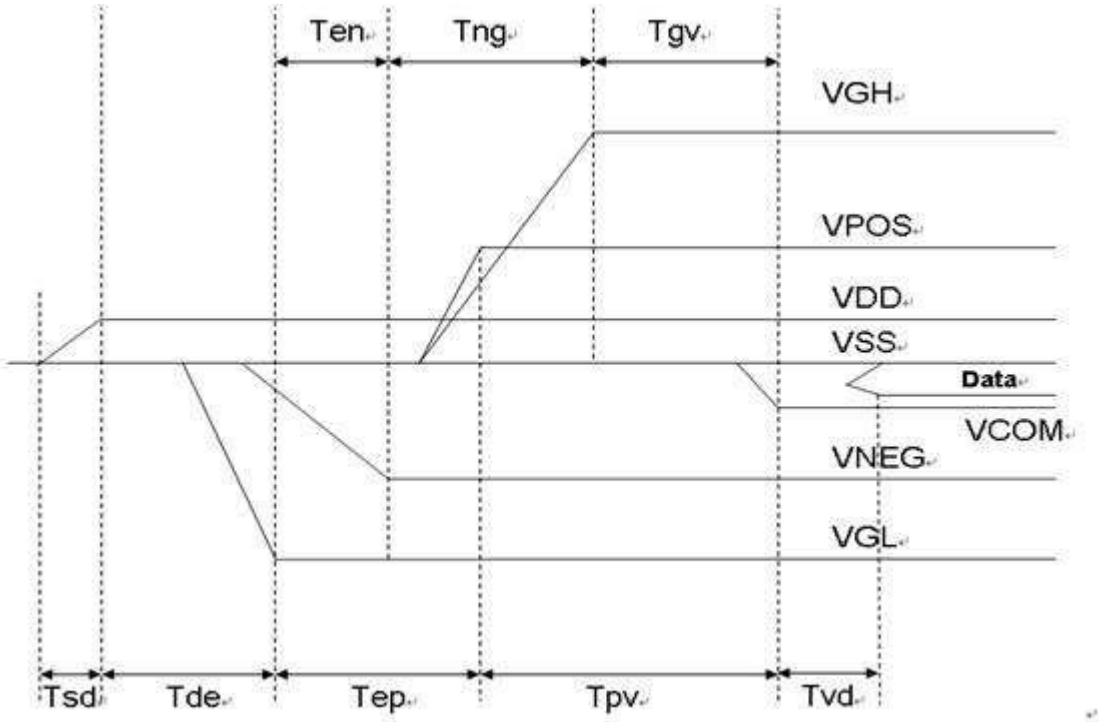
7. Power on sequence

Power Rails must be sequenced in the following order：

1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM

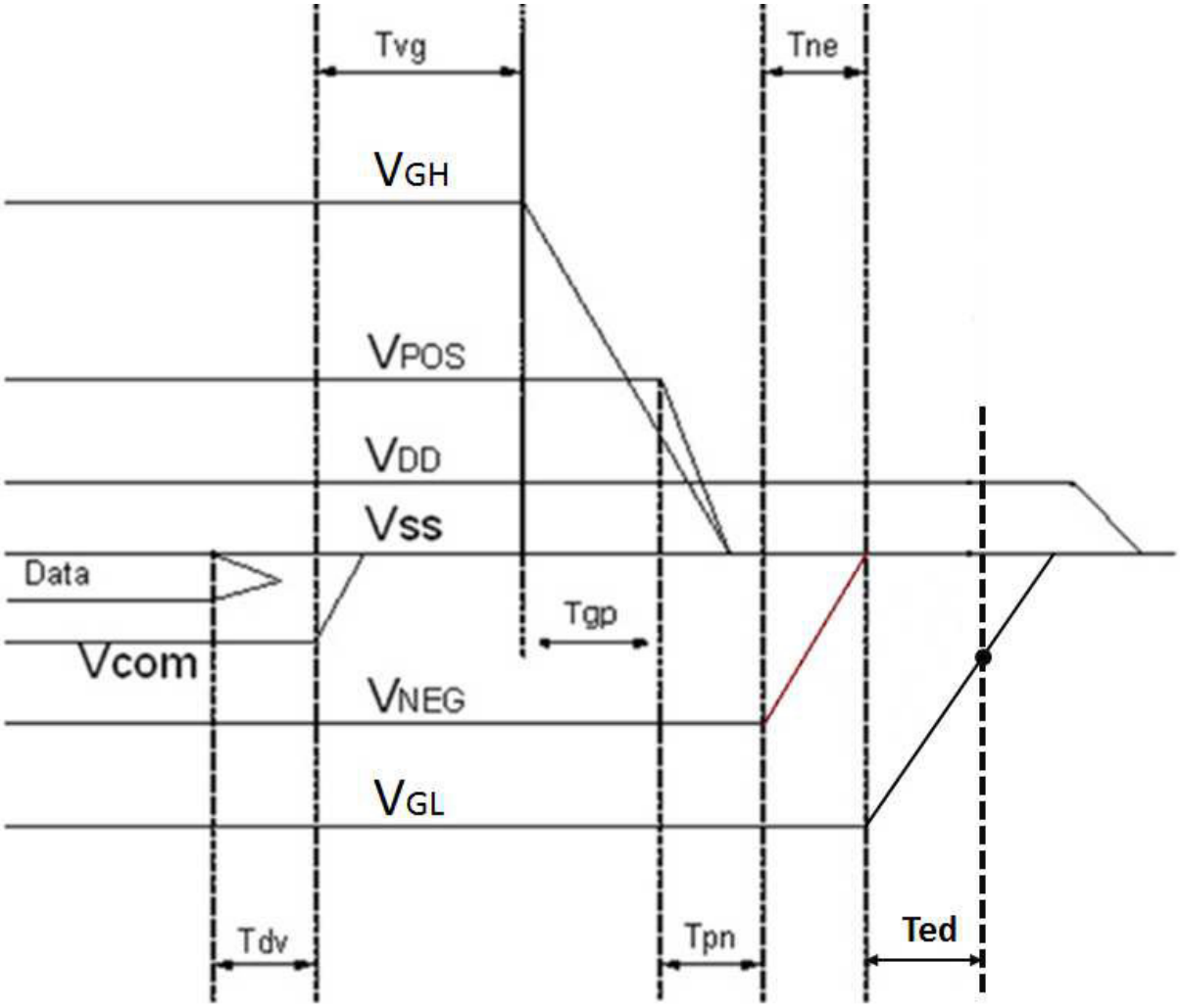
2. VSS → VDD → VEE → VGH (Gate driver)

POWER ON



	Min	Max
Tsd	30us	--
Tde	100us	--
Tep	1000us	--
Tpv	100us	--
Tvd	100us	--
Ten	0us	--
Tng	1000us	--
Tgv	100us	--

POWER DOWN



	Min	Max
Tdv	100µs	-
Tvg	0µs	-
Tgp	0µs	-
Tpn	0µs	-
Tne	0µs	-
Ted	0.5s	Discharged point @ -7.4 Volt
Tdv	100µs	-
Tvg	0µs	-

8. Optical characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T = 25°C

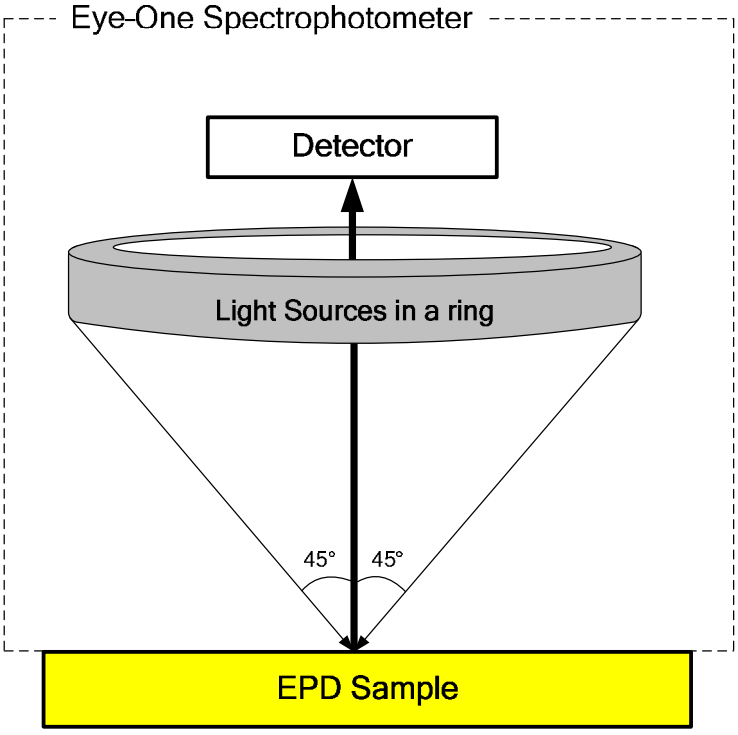
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 9-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS) ×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	12	-		-

WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS
m:4、8、16　when 2、3、4 bits mode

Note 9-1: Luminance meter :Eye – One Pro Spectrophotometer.

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd): CR = Rl / Rd



8-3) Reflection ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \quad x \quad (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9.HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

10. Reliability test

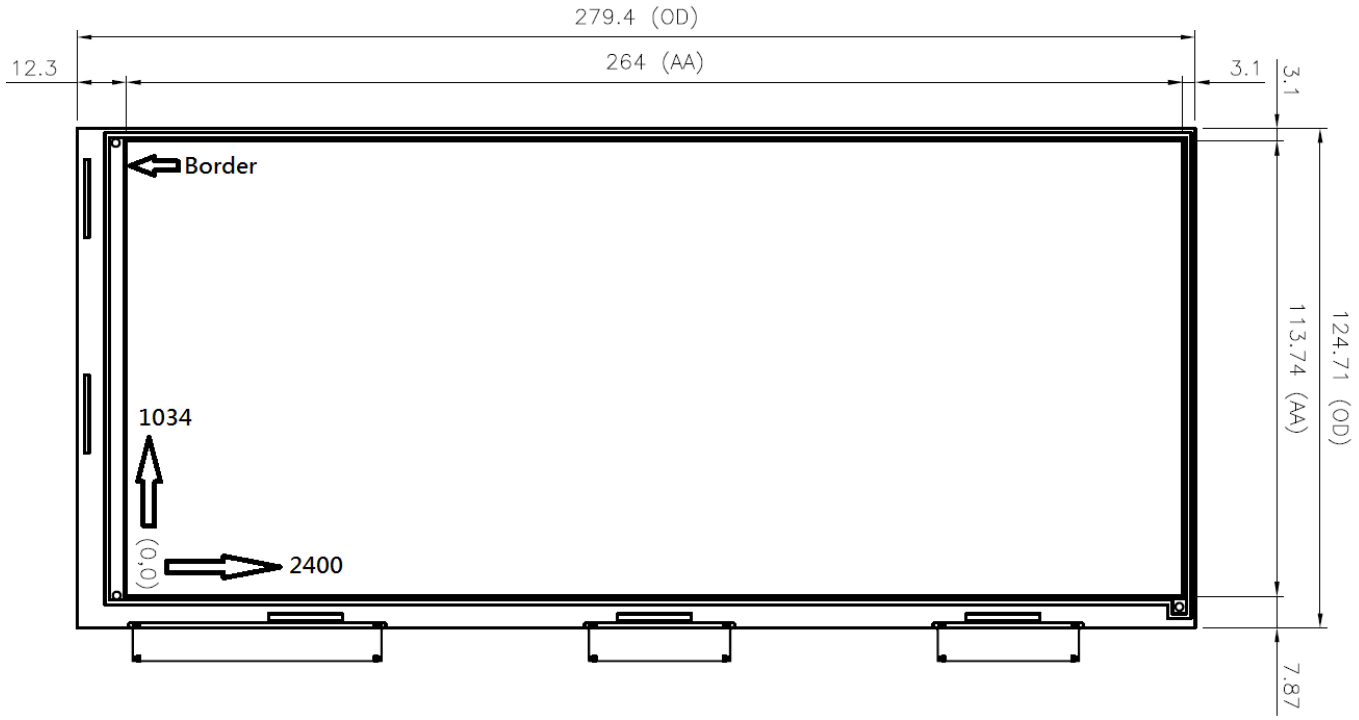
	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	--
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	--
3	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
4	Low-Temperature Storage	T = -25°C for 240 hrs (Test in white pattern)	IEC 60 068-2-1Ab	
5	High Temperature High Humidity Storage	T=+60C RH=80% for 240hrs (Test in White Pattern)	IEC 60 068 2-3CA	
6	High Temperature Storage	T=+70C RH=40% for 240hrs (Test in White Pattern)	IEC 60 068-2-2Bp	--
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min (Test in white pattern)	IEC 60 068-2-14	--
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ (Test in white pattern)	IEC60 068-2-5Sa	--
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	--
10	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner,3 edges,6 faces One drop for each.	Full packed for shipment	--
11	Stylus Tapping	POLYACETAL Pen: Top R:0.8mm Load: 300gf Speed: 30 times/min Total 13,500times,	--	Test with bezel and device to simulate full product test.
12	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	--

Note : The protective film must be removed before temperature test.

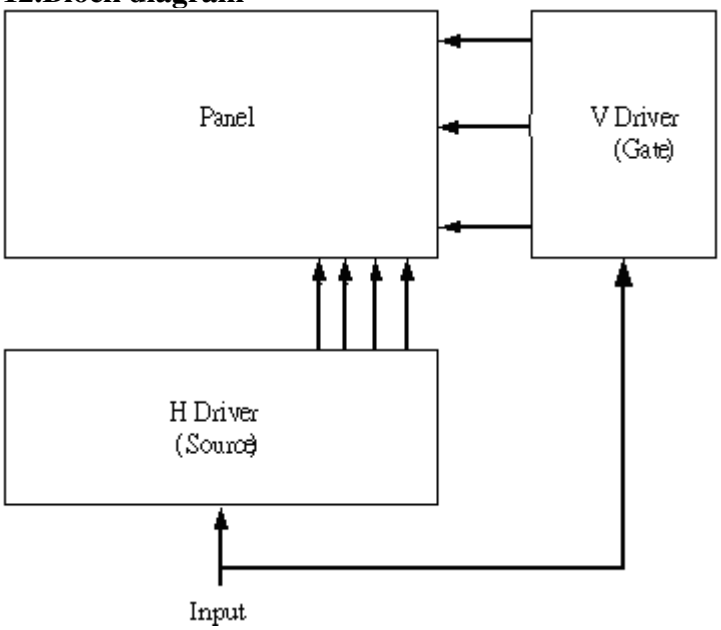
[Criteria]

In the standard conditions, there is not display function NG issue occurred. (Including：line defect, no image) All the cosmetic specification is judged before the reliability stress.

11. Border definition and scan direction

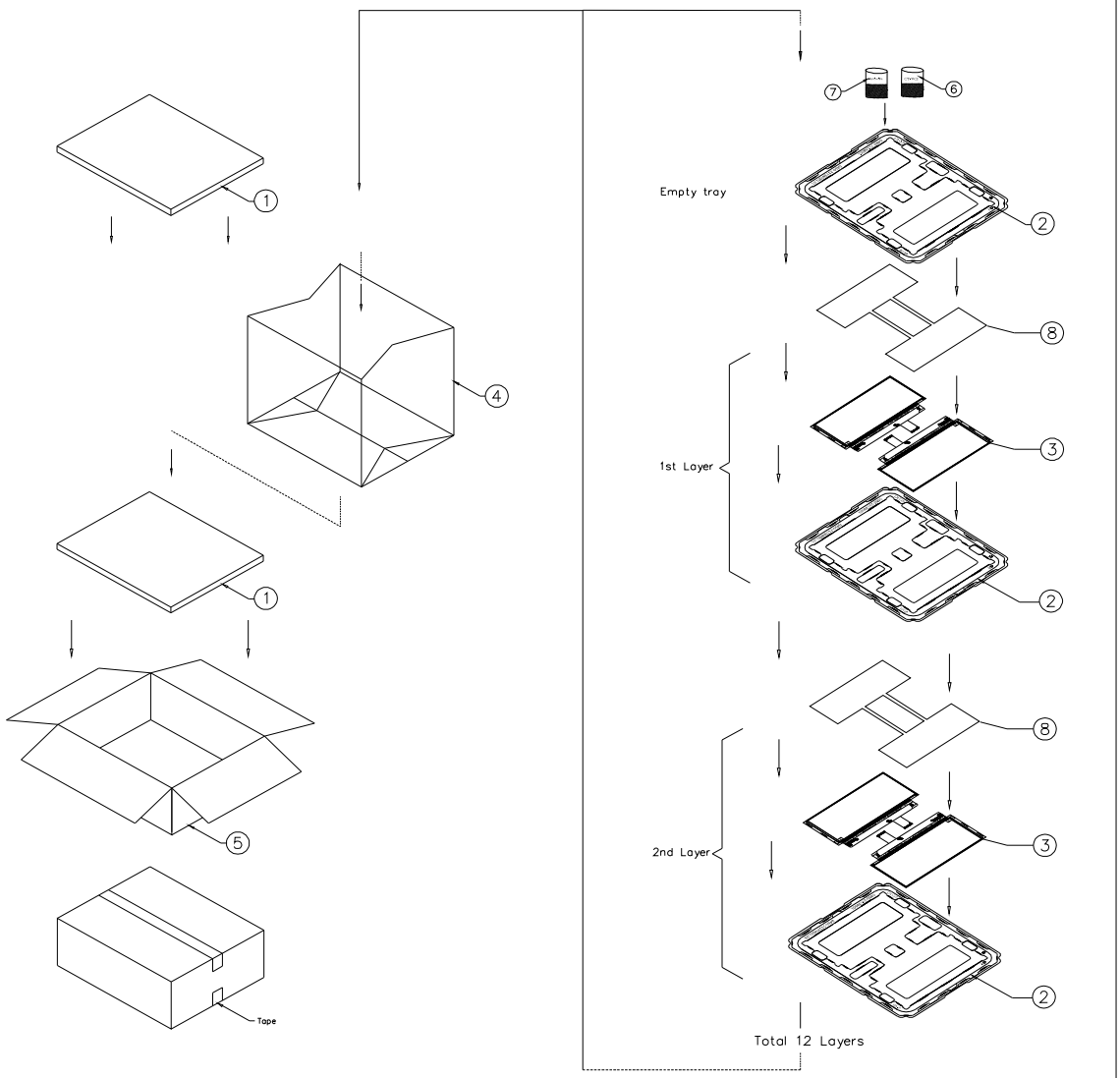


12.Block diagram



13.Packing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Jin Huang	2017/07/19



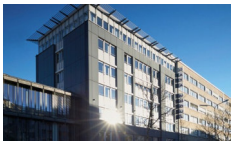
NOTE:
1. One layer include:
   2 pcs module & 1 piece of tray.
2. Q'TY: 24 pcs panel/carton.
3. Dimension: 445*365*170mm

ITEM	DESCRIPTION	Q'TY	REMARK
8	EPE CUSHION SHEET	12	抗靜電
7	30g乾燥劑	2	
6	防鏽劑(保護容積25L)	3	
5	CARTON INTERNAL	1	
4	摺口袋450*380*580mm	1	抗靜電
3	ED113TC1	24	
2	TRAY	13	抗靜電
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ±5.0mm ANGLE ROUGHNESS	REMARK	E Ink 元太科技工業股份有限公司			
APPROVE	Patrick Lin	2017/07/19	SCALE 1:1	UNIT mm	SHEET 1 OF 1	DWG.TITLE ED113TC1 PACKING
CHECK	Patrick Lin	2017/07/19	MTL.NO.		DWG.NO.	A4 SIZE
DESIGN	Jin Huang	2017/07/19				

DATA MODUL

ALL TECHNOLOGIES. ALL COMPETENCIES. ONE SPECIALIST.



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