Hardware Documentation

armStone™A9

Version 104
(2020-07-17)

Elektronik Systeme

Untere Waldplätze 23
D-70569 Stuttgart
Phone: +49(0)711-123722-0
Fax: +49(0)711-123722-99

About This Document

This document describes how to use the arnStone™A9 board with mechanical and electrical information. The latest version of this document can be found at:

http://www.fs-net.de.

ESD Requirements

All F&S hardware products are ESD (electrostatic sensitive devices). All products are handled and packaged according to ESD guidelines. Please do not handle or store ESD-sensitive material in ESD-unsafe environments. Negligent handling will harm the product and warranty claims become void.

History

Date	V	Platform	A,M,R	Chapter	Description	Au
2013-02-19	0.01	ASA9	A	*	First Preliminary version	KW
2013-11-15	0.02	ASA9	M	4 5.1	Correct signal name conventions, correct pins for COM Adjust TDP	KW
2014-03-06	0.03	ASA9	A M	4 0	Connector layout additions	KW
2014-03-14	0.04	ASA9	A	4.11.5 2,3	Add note it is optional Add SATA with limitations	KW
2014-08-15	0.04	ASA9	M	*	Change to New Company CI	JG
2014-10-02	0.05	ASA9	A A A	5-2 0 4	Add cooling notes Add backlight wiring description Note for JILI30 pin 1	KW
2014-10-14	0.06	ASA9	A	4.11.5 5.2	Correct to ADS1015 Add electrical data for 3.3V IO	KW
2014-10-16	0.06	ASA9	A	4.11.4	Information about I2C interfaces	HF
2014-10-18	0.07	ASA9	A	4.11.4	Correct information about SPI	HF
2014-12-02	0.07	ASA9	M	4.8	Correct article numbers for touch modules	JG
2014-12-10	0.08	ASA9	M	4.6.1	Correct pin 24	KW
2015-01-08	0.09	ASA9	M	4.6.14.11 4.11.10	Remove the optional CAN Transceiver	KW
2015-02-05	0.10	ASA9	M	0	Add notice for pull-up at touch con.	HF
2015-06-15	0.11	ASA9	A	5.1	Add TDP for Solo and Duallight	KW
2016-10-16	0.12	ASA9	M A	4.11.7 6,7,8	Correct PU to COL Add some chapter for Storage, ROHS, Barcode Sticker	KW
2017-01-03	100	ASA9	A	4.6.2 4.6,5.1	Add missing I2C signals Add VLCD max current	KW
2017-11-13	101	ASA9	M		Index refreshed	HF
2018-09-14	102	ASA9	A	6	Extend thermal specification	HF
2020-06-08	103	ASA9	M	2	Corrct PCB thickness and update to new F&S Layout	MW
2020-07-17	104	ASA9	A	7	Add ADP-NT24V2	MW

V	Version
A,M,R	Added, Modified, Removed
Au	Author

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1 Block diagram

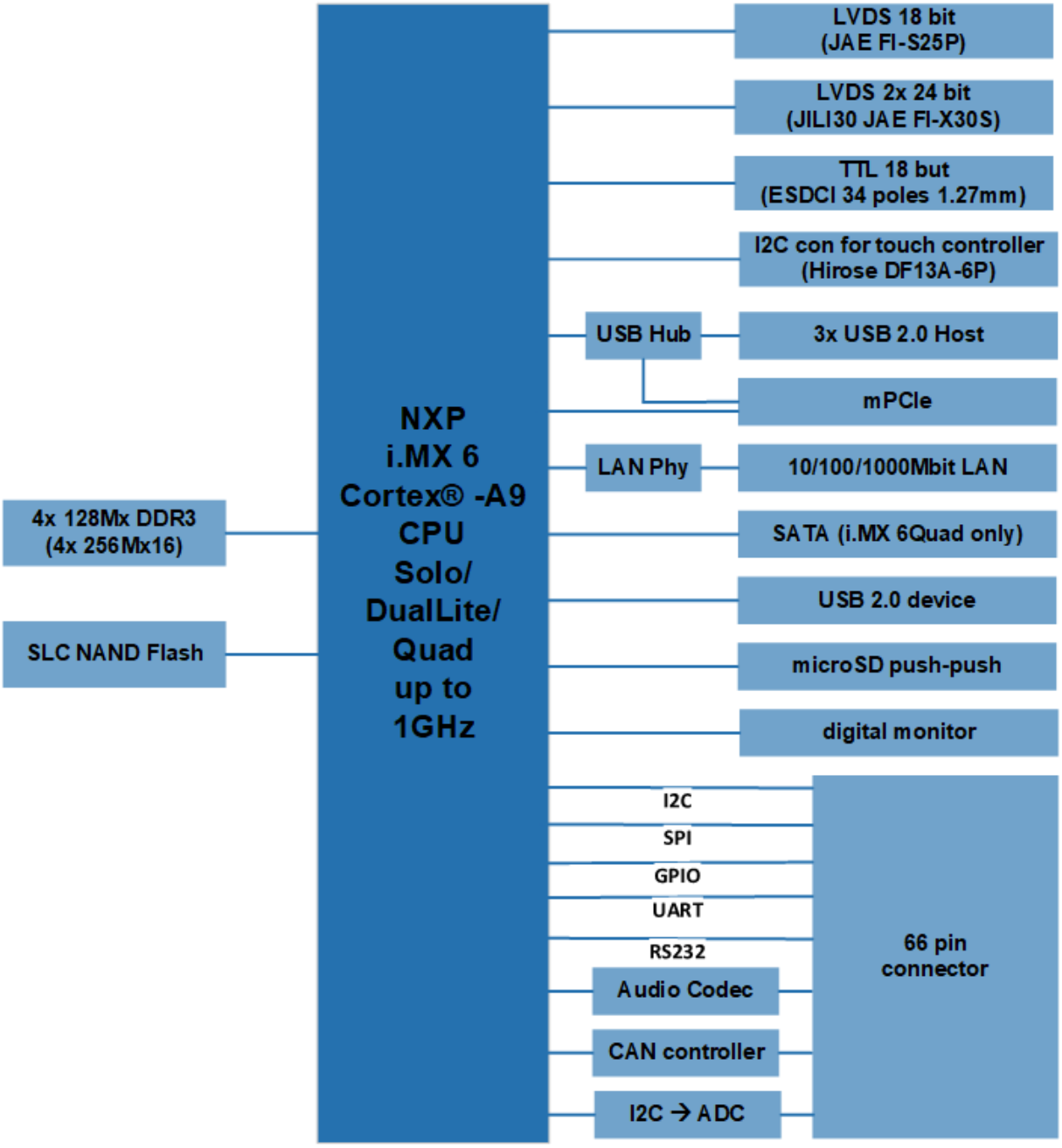


Figure 1: Block Diagram

2 Mechanical Dimension

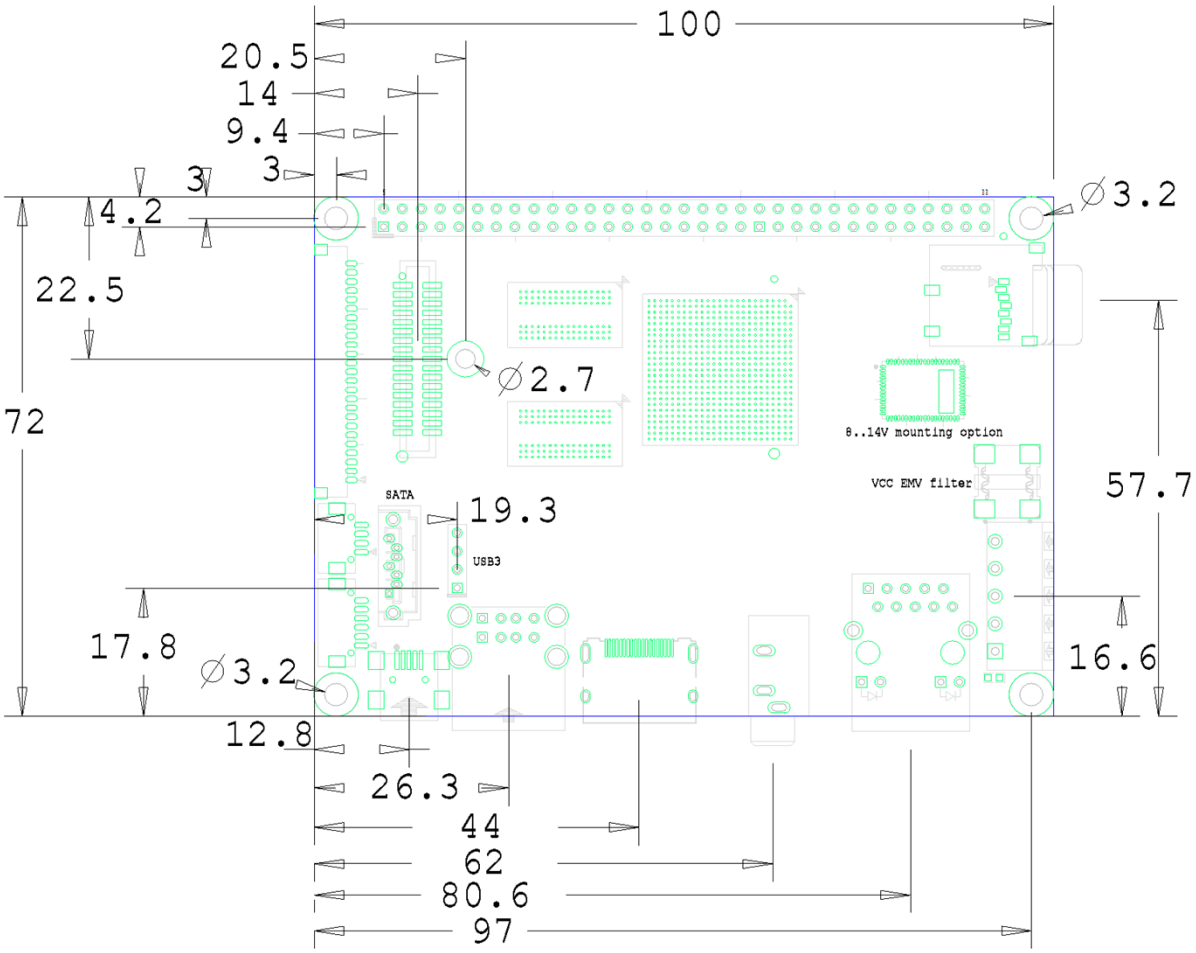


Figure 2: Mechanical Dimension

Dimensions	Description
Size	472mm x 100mm (picoITX)
PCB Thickness	1.6mm ± 0.1mm
Height of the parts on the top side	Max. 15mm
Height of the parts on the bottom side	Max. 16mm

Table 1: Mechanical Dimensions

3D Step model available, please contact support@fs-net.de

3 Technical Data armStoneA9

3.1 Technical Data

Power supply:	5V DC ±5%, optional 8..14V DC
Interfaces:	1x Ethernet 10/100/1000Mbit
	4x USB 2.0 Host
	1x USB 2.0 Device
	1x digital monitor
	1x microSD card connector push-push
	1x mPCIe
	1x SATA (only with quad core CPU)
	1x I2C for touch module
	1x stereo Audio LineIn, LineOut, Mic
	2x serial port RS232
	1x serial port TTL
	4x ADC In (10 bit, 500kSPS, optional on custom version)
	3x PWM out
	1x I2C
	1x SPI
	17x GPIO
LCD-interfaces:	1x 18bit LVDS F&S JAY FI-S25P
	1x 2x 24bit LVDS JILI30
	1x 18bit TTL ESDCI
Memory:	1 GByte DDR3 DRAM (optional 2GB)
	128 MByte NAND Flash (optional up to 32 GByte)
CPU:	Freescale i.MX6 Solo, DualLite or Quad Core
	(Optional several temperature and frequency)

3.2 Thermal Specification

	Min	Typ	Max	Unit
Operating temperature	0		+70[1]	°C
Operating temperature (“I”)[2]	-20		+85[1]	°C
Junction temperature i.MX6	-20		+105	°C
Junction temperature i.MX6 (“I”) [2]	-20		+105	°C
Junction to Top of i.MX6 (Psi-JT)[3]		2		°C/W

Table 2: Thermal Specification

[1] Depending on cooling solution. See also:

[2] Optional

[3] Temperature difference between package top and the junction temperature per JEDEC JESD51-2.

4 Interfaces

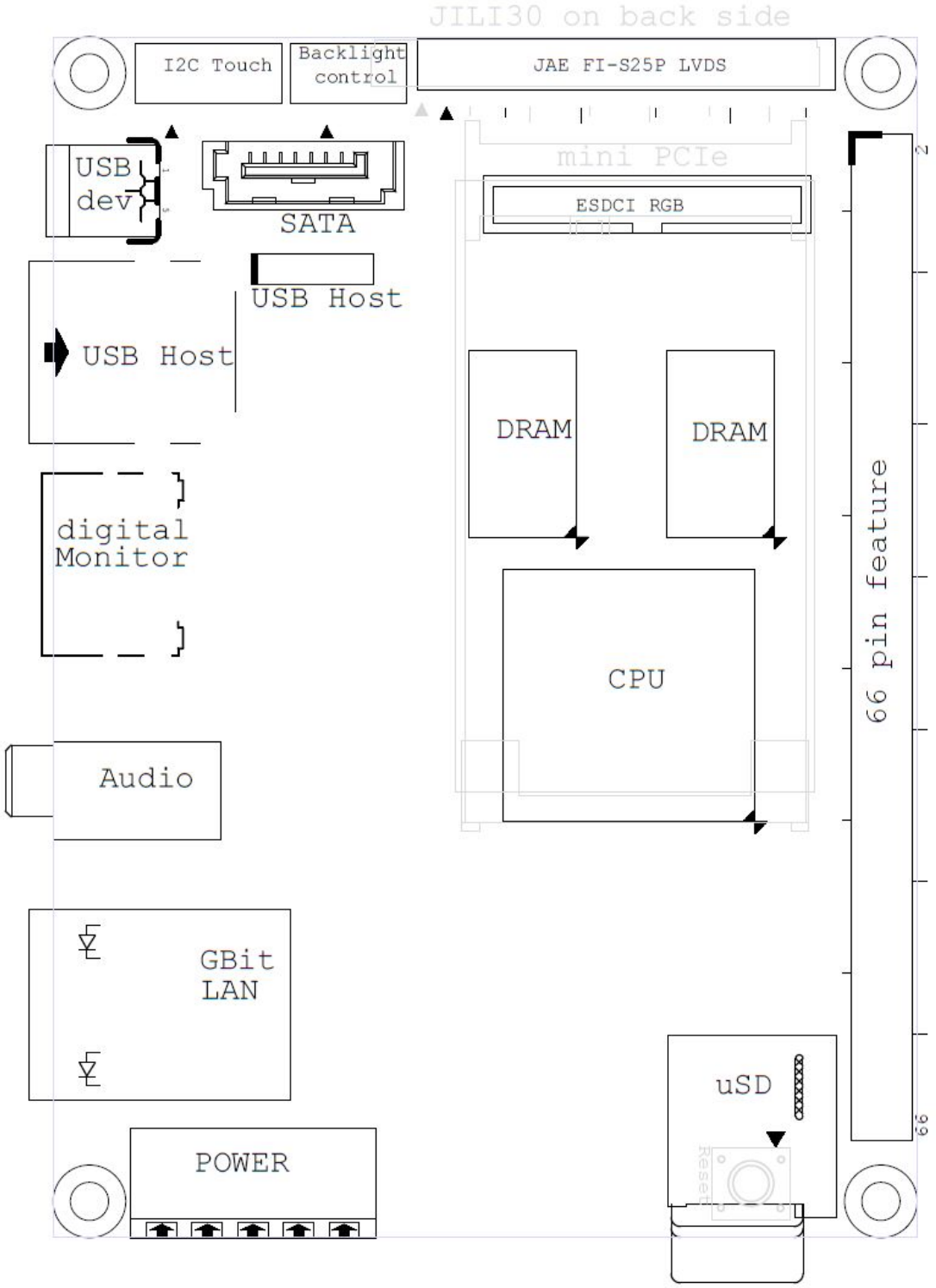


Figure 3: Connector Layout

Note: there is a wrong pin 1 marker on the JILI30 connector on back side. The inner pin is pin 1. The picture above is right. This marking failure will occur up to PCB Rev 1.10.

4.1 Gbit Ethernet LAN

The LAN1 connector does support 10, 100 and 1000 Mbit LAN.

4.2 USB Hoct Connector

The double USB Host connector does support USB2.0 connection with High speed up to 480Mbit/s and also full and low speed devices.

The on-board pin connector for internal USB does have the following pin out.

Pin	Signal	I/O	Voltage	Remarks
1	+5V	PWR	5.0V	shared with resettable fuse from front port connector
2	USB3-	I/O		
3	USB3+	I/O		
4	GND	PWR		

Table 3: USB OTG & Host Interface Connections

The signals on the internal connector doesn't have EMV filter.

The power on the 5V line is equipped with a resettable fuse with 1100mA for both front connected port and the internal port together. At 70°C the summary current is limited to 650mA.

Current consuming summary of all ports shouldn't exceed maximum power consuming limit on the 5V path.

4.3 USB Device Connector

The USB device connects the armStoneA9 as device on a PC.

4.4 Digital Monitor Connector

A digital monitor can connected to the board. This interface supports up to 1080p 60Hz.

4.5 microSD Connector

The microSD push-push connector supports the SD Standard Host Specification Version 2.0 standard.

4.6 LVDS Connectors

4.6.1 F&S JAE FI-S25P connector on top side

The single channel LVDS display port on top side can be direct connected to a LVDS 18 or 24 bit display.

The VLCD voltage is 3.3V and switched on the baseboard. The current limit is 1.2 A.

Connector is a JAE FI-S25P-HFE. Matching connector on display cable is a crimp connector FI-S25S housing and a cable with FI-C3-A1-15000 crimp contacts.

This connector is used because a wide range of displays does have a JAE FI-S series connector (with different pinouts) and it's easy to handle identical crimp contacts for the cable manufacturer.

LCD FI-S25S Connector				
Pin	Signal	I/O	Voltage	Remarks
1	VLCD	PWR	3.3V	Switched, max. 300mA
2	VLCD	PWR	3.3V	Switched, max. 300mA
3	GND	PWR		
4	GND	PWR		
5	LVDS0_DATA0-	O		
6	LVDS0_DATA0+	O		
7	GND	PWR		
8	LVDS0_DATA1-	O		
9	LVDS0_DATA1+	O		
10	GND	PWR		
11	LVDS0_DATA2-	O		
12	LVDS0_DATA2+	O		
13	GND	PWR		
14	LVDS0_CLK-	O		
15	LVDS0_CLK+	O		
16	GND	PWR		
17	LVDS0_DATA3-	O		
18	LVDS0_DATA3+	O		
19	GND	PWR		
20	n.c.	-		
21	n.c.	-		
22	GND	PWR		
23	n.c.	-		
24	Backlight on	O	3.3V	High active CMOS logic
25	Backlight PWM	O	3.3V	CMOS logic

Table 4: Single channel LVDS connector

Pin 1 is marked on the connector with an arrow and also marked on PCB.

The single channel LVDS port can be direct connected to a LVDS 18 bit display.

Unused signals should be left unconnected.

4.6.2 JILI30 JAE FI-X30S connector on bottom side

The dual channel LVDS display port can be direct connected to a LVDS 18 or 24 bit single channel or dual channel display.

The signals for the first channel are shared with the other connector 4.6.1.

By connecting 2 single channel displays to the board we recommend to use the top connector for the first channel and the second channel of the bottom connector for the second display.

LCD FI-X30P Connector				
Pin	Signal	I/O	Voltage	Remarks
1	LVDS0_DATA0-	O		shared with FI-S25P on top side
2	LVDS0_DATA0+	O		shared with FI-S25P on top side
3	LVDS0_DATA1-	O		shared with FI-S25P on top side
4	LVDS0_DATA1+	O		shared with FI-S25P on top side
5	LVDS0_DATA2-	O		shared with FI-S25P on top side
6	LVDS0_DATA2+	O		shared with FI-S25P on top side
7	GND	PWR		
8	LVDS0_CLK-	O		shared with FI-S25P on top side
9	LVDS0_CLK+	O		shared with FI-S25P on top side
10	LVDS0_DATA3-	O		shared with FI-S25P on top side
11	LVDS0_DATA3+	O		shared with FI-S25P on top side
12	LVDS1_DATA0-	O		
13	LVDS1_DATA0+	O		
14	GND	PWR		
15	LVDS1_DATA1-	O		
16	LVDS1_DATA1+	O		
17	GND	PWR		
18	LVDS1_DATA2-	O		
19	LVDS1_DATA2+	O		
20	LVDS1_CLK-	O		
21	LVDS1_CLK+	O		
22	LVDS1_DATA3-	O		
23	LVDS1_DATA3+	O		
24	GND	PWR		
25	I2C_C_DAT	I/O	3.3V	4,7kΩ Pull Up onboard
26	Backlight on	O	3.3V	High active CMOS logic
27	I2C_C_CLK	I/O	3.3V	4,7kΩ Pull Up onboard
28	VLCD	PWR	3.3V	Switched, max. 300mA
29	VLCD	PWR	3.3V	Switched, max. 300mA
30	VLCD	PWR	3.3V	Switched, max. 300mA

Table 5: JILI30 dual channel LVDS connector

4.7 ESDCI RGB connector

Connector is a 1.27mm pitch shrouded header for 1.27mm pitch IDC connector.

All signals have 3.3V level. I2C signals are for touch controller and to control the backlight on display adapter.

Pin	Signal	I/O	Voltage	Remarks
1	+V3.3	PWR	3.3V	Max. 100mA
2	+V5.0	PWR	5.0V	Max. 100mA
3	GND	PWR		
4	LCD_CLK	O		
5	LCD_HSYNC	O		
6	LCD_VSYNC	O		
7	GND	PWR		
8	LCD_R0	O		
9	LCD_R1	O		
10	LCD_R2	O		
11	LCD_R3	O		
12	LCD_R4	O		
13	LCD_R5	O		
14	GND	PWR		
15	LCD_G0	O		
16	LCD_G1	O		
17	LCD_G2	O		
18	LCD_G3	O		
19	LCD_G4	O		
20	LCD_G5	O		
21	GND	PWR		
22	LCD_B0	O		
23	LCD_B1	O		
24	LCD_B2	O		
25	LCD_B3	O		
26	LCD_B4	O		
27	LCD_B5	O		
28	GND	PWR		
29	LCD_DE	O		
30	VLCD	PWR	3.3V	Switched, max. 300mA, usable as VLCDON
31	VLCD	PWR	3.3V	Switched, max. 300mA, usable as VLCDON
32	I2C_DAT	I/O	3.3V	shared with I2C connector for touch module, 4,7kΩ PullUp onboard

33	I2C_IRQ	I	3.3V	shared with I2C connector for touch module
34	I2C_CLK	I/O	3.3V	shared with I2C connector for touch module, 4,7kΩ PullUp onboard

Table 6: Digital RGB display connector

4.8 Backlight control connector

The connector is a Hirose 4 pin connector, model no. DF13A-4P-1.25H, mounted on the QBlissA8 module. Pin 1 is marked on PCB.

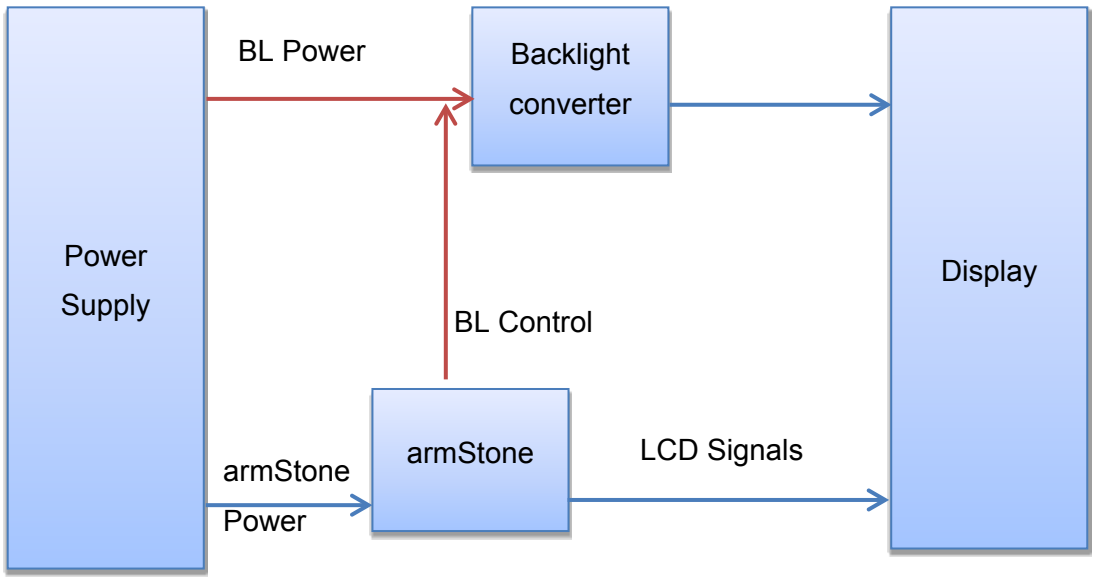
Matching connector is a Hirose DF13-4S-1.25C with DF13-2630SCF crimping contacts.

Unused signals should be left unconnected.

Pin	Signal	I/O	Voltage	Remarks
1	VLCDON	O	3.3V	3.3V TTL level control signal; not used for backlight
2	Backlight On	O	3.3V	3.3V TTL level control signal, no power out
3	Backlight PWM	O	3.3V	3.3V TTL level control signal
4	LCD_CLK	PWR		

Table 7: Backlight control connector

4.8.1 Solution with a single cable with 3 connectors



Cable with 3 connector

Figure 4: backlight connection with single cable

4.8.2 Solution with 2 cable with 2 connectors each

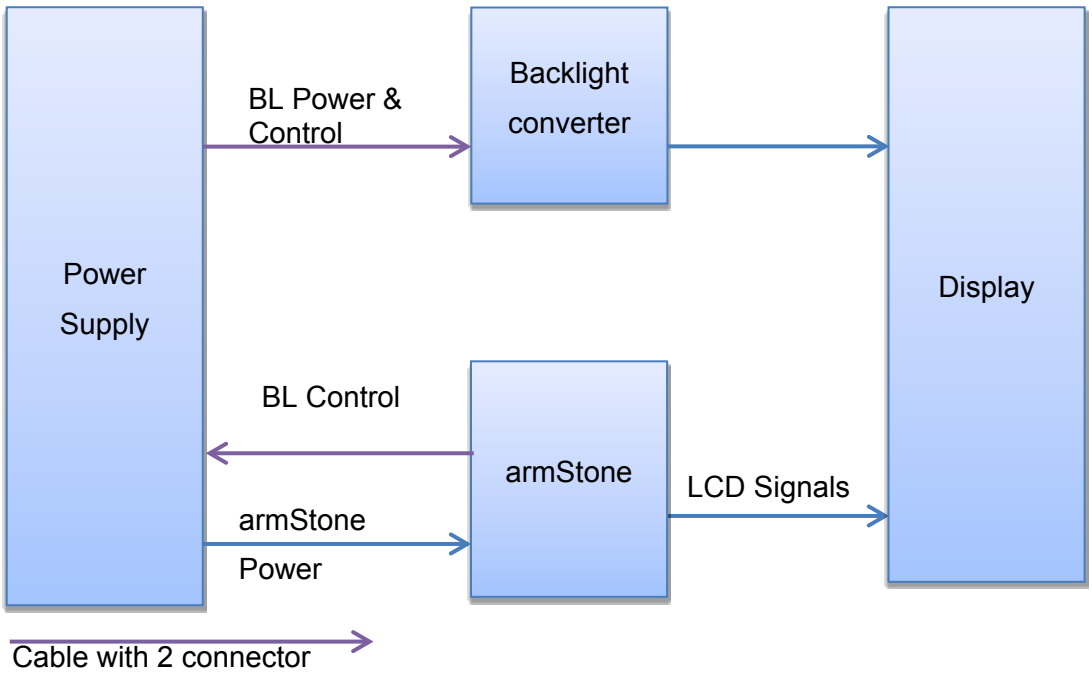


Figure 5: backlight connection with 2 cable

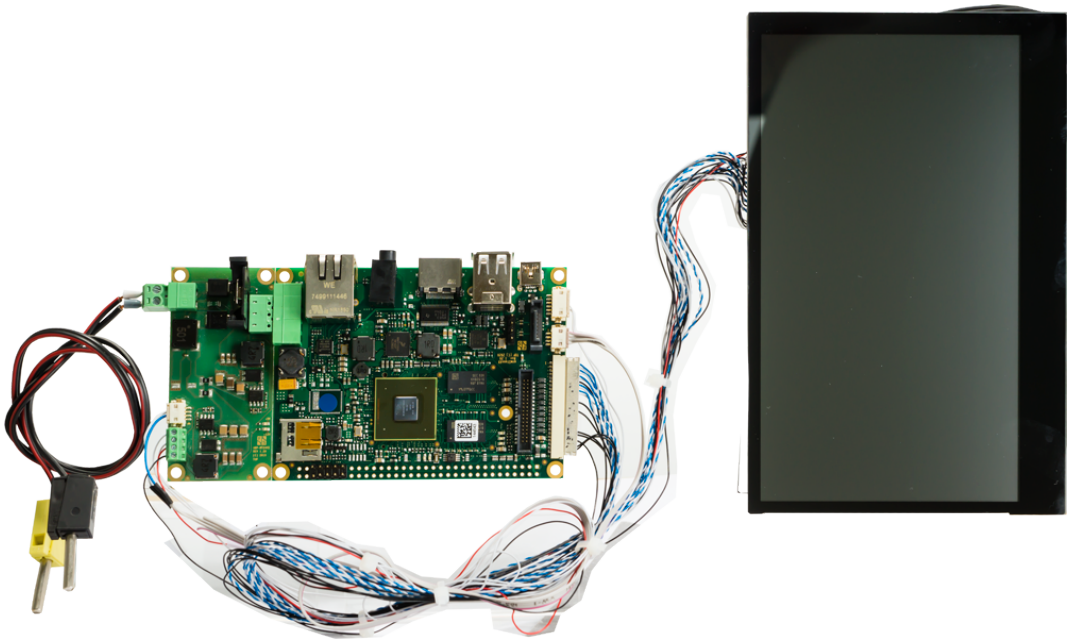


Figure 6: backlight connection with single cable

4.9 I2C connector for touch module

This connector is to connect the F&S SINTF-ADP-CTOUCH or SINTF-ADP-RTI2C. SINTF-ADP-CTOUCH module is based on Atmel mXT224 maxTouch chip working with several capacitive touch glasses.

The SINTF-ADP-RTI2C is based on Semtech SX8655 for 4 and 5 wire touch.

The connector is a Hirose 6 pin connector, model no. DF13A-6P-1.25H, mounted on the armStoneA9 module. Pin 1 is marked on PCB.

Matching connector is a Hirose DF13-6S-1.25C with DF13-2630SCF crimping contacts.

Signals are shared with I2C interface on ESDCI RGB connector for the same functionality..

Unused signals should be left unconnected.

Pin	Signal	I/O	Voltage	Remarks
1	VCC	PWR	3.3V	
2	I2C_DAT	I/O	3.3V	
3	I2C_CLK	I/O	3.3V	
4	I2C_RST	O	3.3V	Active LOW Signal
5	I2C_IRQ	I	3.3V	Active LOW Signal
6	GND	PWR		

Table 8: I2C Touch Interface

4.10 Mini PCI Express

One 52 pin Mini-PCI-Express socket for a full-size 30x50,95 mm card is mounted on the armStoneA9. This socket does provide a PCIe channel x1 and one USB port.

4.11 66 Pin Feature connector

This 2.54mm connector supports CAN, RS232, Audio, ADC Input, PWM output, TTL serial ports, keyboard matrix and GPIOs.

Pin	Signal	I/O	Voltage	Remarks
1	VCC 3.3V	PWR	3.3V	
2	VCC 5.0V	PWR	5.0V	
3	XGPIO0/COL0	I/O	3.3V	
4	XGPIO1/COL1	I/O	3.3V	
5	XGPIO2/COL2	I/O	3.3V	
6	XGPIO3/COL3	I/O	3.3V	
7	XGPIO4/COL4	I/O	3.3V	
8	XGPIO5/COL5	I/O	3.3V	
9	XGPIO6/COL6	I/O	3.3V	
10	XGPIO7/COL7	I/O	3.3V	
11	GND	PWR		
12	XGPIO8/SPI_CLK	I/O	3.3V	
13	TX1/GPIO0	I/O	3.3V	
14	XGPIO9/SPI_CSn	I/O	3.3V	Active LOW Signal
15	RX1/GPIO1	I/O	3.3V	
16	I2CLK/SPI_MOSI	I/O	3.3V	
17	I2DAT/SPI_MISO	I/O	3.3V	
18	XGPIO10/ROW0	I/O	3.3V	
19	XGPIO11/ROW1	I/O	3.3V	
20	XGPIO12/ROW2	I/O	3.3V	
21	XGPIO13/ROW3	I/O	3.3V	
22	XGPIO14/ROW4	I/O	3.3V	
23	XGPIO15/ROW5	I/O	3.3V	
24	XGPIO16/ROW6	I/O	3.3V	
25	XGPIO17/ROW7	I/O	3.3V	
26	XGPIO18	I/O	3.3V	
27	GND	PWR		
28	PWMOUT0	O	3.3V	
29	ADC_IN0	I	3.3V	
30	PWMOUT1	O	3.3V	
31	ADC_IN1	I	3.3V	
32	PWMOUT2	O	3.3V	
33	ADC_IN2	I	3.3V	
34	Backlight On	O	3.3V	

35	ADC_IN3	I	3.3V	
36	RXD2	I	3.3V	RS232 Signal
37	GND	PWR		
38	TXD2	o	3.3V	RS232 Signal
39	VCC 3.3V	PWR	3.3V	
40	VCC 5.0V	PWR	5.0V	
41	MIC1	I		Audio Pin 1
42	GND	PWR		
43	n.c.			
44	LINEIN_R	I		
45	LINEOUT_R	O		
46	GND	PWR		
47	GND	PWR		
48	LINEIN_L	I		
49	LINOUT_L	O		
50	GND	PWR		
51	RESETBTN	I	3.3V	
52	VCC 3.3V	PWR	3.3V	
53	n.c.	-	-	COM Pin1
54	n.v.	-	-	
55	RXD0	I	3.3V	
56	RTS0	O	3.3V	
57	TXD0	O	3.3V	
58	CTS0	I	3.3V	
59	n.c.	-	-	
60	n.c.	-	-	
61	GND	PWR		
62	VCC 5.0V	PWR	5.0V	
63	CANRX	I	3.3V	
64	CANTX	O	3.3V	
65	BOOTSEL	I	3.3V	
66	VCC 3.3V	PWR	3.3V	

Table 9: armStone Feature Connector

On default a 9 pin connector is mounted on pin 53..61 to use a COM port standard adapter cable. *Italic signals does have a 4k7 pull-up on the module.*

4.11.1 Audio

The connector does provide Stereo Line in, Stereo Line out and microphone.

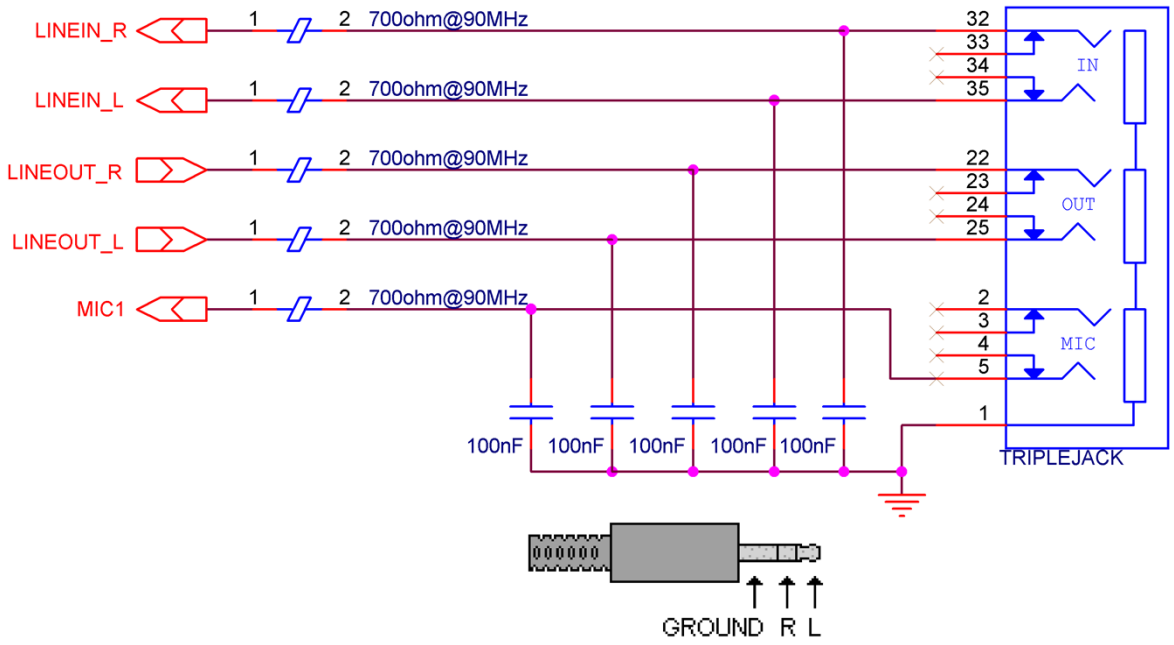


Figure 7: Audio connection

4.11.2 RS232 COM port

A 9 pin double row connector is mounted in pin 53..61. That allows attaching a standard 9pin to DSUB9 adapter cable for debug output of boot loader and kernel with TX and RX to a terminal.

An additional RX/TX COM port pair is on pin 36&38.

4.11.3 TTL COM port

There is an additional serial ports with 3.3V TTL level on pin 13&15.

4.11.4 I2C/ SPI

The module supports two I2C interfaces at feature connector. Only one is compatible with armStone standard. Signals are 3.3V compliant and do have 4.7k pull-ups on module

There is also a HS SPI interface as alternative function available on these pins.

armStoneA9 Feature Connector I2C Interfaces				
Pin	I2C	Standard	Optional	Remarks
12	-	GPIO	GPIO, SPI_CLK	4,7kΩ PullUp onboard
14	-	GPIO	GPIO, SPI_CS	4,7kΩ PullUp onboard
16	Soft I2C_SCL	I2C_SCL	GPIO, SPI_MOSI	4,7kΩ PullUp onboard
17	Soft I2C_SDA	I2C_SDA	GPIO, SPI_MISO	4,7kΩ PullUp onboard
18	I2C1_SCL	GPIO	GPIO, ROW0	
26	I2C1_SDA	GPIO	GPIO	

Table 10: I2C/ SPI Interfaces

[2)] These IO-Pins can be reconfigured as GPIO.

[3)] Alternate pin configuration function in software. Please refer the software manual or ask our technical support. There is no compatibility to other armStone using this alternative function.

4.11.5 ADC In

4 ADC inputs (ADC_IN0..3)

Created by an on board mounted TI ADS1015.

This feature is just available on a custom version.

4.11.6 PWM out

3 programmable PWM outputs (PWMOUT0..2) with 3.3V level in 16.1kHz up to 33 MHz frequency range

4.11.7 Matrix keyboard

8x8 keyboard matrix (ROW0..7, COL0..1) with 3.3V level. The COL signals in pin 3..10 does have 4.7k pull-ups on board.

4.11.8 GPIOs

GPIOs are programmable as Input or Output with 3.3V TTL level. The default maximum driver current is 10mA (sink and source).

XGPIO0..9 do have 4.7k pull-up on module.

4.11.9 MISC signals, power

RESETBTN	3.3V TTL low active RESET input; use pushbutton to GND or open collector driver to pull low. Don't drive with high level.
VCC3.3, VCC5	voltage outputs for external logic, max. 100mA per pin
	for external chips and functions
Backlight On	3.3V TTL high active output to switch on LCD backlight. Same signal as on 4.6.1 and 4.7
Bootsel	only used for production. Don't use.

4.11.10 CAN Bus

The module does provide the CAN bus transmit and receive TTL signal without any termination in standard version (CANRX, CANTX). Both signals are working with 3.3V level.

Needs a interface chip to the CAN bus showing below. If not used, please left signals unconnected.

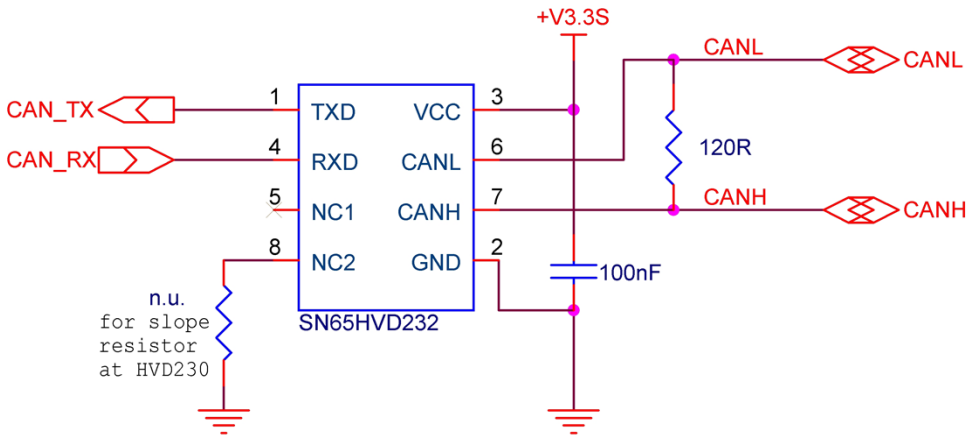


Figure 8: CAN transceiver circuit

4.12 Power connector

A 5 pin power connector is mounted on the module.

Connector type

- Phoenix contact MC 1,5/ 5-G-3,81 1803303
- Würth Elektronik order no. 691 322 310 005

For matching connectors please refer the connector manufacturer website.

Pin	Signal	I/O	Voltage	Remarks
1	n.c.	-	-	
2	RTC Battery	PWR		for RTC battery, don't connect if not used
3	VCC IN	PWR	5.0V	
4	GND IN	PWR		
5	VCC OUT	PWR	3.3V	Power output for external logic, max. current 50mA

Table 11: Power Connector

If an external 3.3V power supply is used for external logic, we recommend to use the "VCC Out 3.3V" as enable signal for this power supply to avoid backdrive leak current thru IO pins.

5 Electrical characteristic

5.1 Absolute maximum ratings

Description	Min	Max	Unit
Input Voltage range 3.3V IO pins	-0.3	OVDD*+0.3	V
Voltage on any IO with VIN off		0.3	V
USB VBUS	-0.3	5.6	V
Maximum power consumption VDD_VBAT at 25°C		10	µA
Maximum output current VLCD		300	mA
Thermal design power (summary all chips) (with 1GHz Quad CPU)*		10.6	W
Thermal design power (summary all chips) (with 1GHz DualLite CPU)*		7	W
Thermal design power (summary all chips) (with 1GHz Solo CPU)*		6	W

Table 12: Absolute Maximum Ratings

* Power consumption of connected devices like display, USB devices, SD card, miniPCIe card has to be added for power calculation.

5.2 DC Electrical Characteristics

Parameter	Description	Condition	Min	Max	Unit
VIN	Module main power		4.7	5.5	V
VBAT	RTC power		0.9	5.5	V
USB_OTG*_VBUS	USB supply voltage		4.4	5.5	
OVDD	On module 3.3V DCDC		3.15	3.45	V
V_{ih}	High Level Input Voltage		0.7*OVDD	OVDD	V
V_{il}	Low Level Input Voltage		0	0.3*OVDD	V
V_{oh}	High Level Output Voltage	I_{oh}=0.1mA	OVDD-0,15		V
V_{ol}	Low Level Output Voltage	I_{ol}=0.1mA		0.15	V
I_o	Output current IOs	3.3V		5	mA

OVDD = power on pin 3.3V from on module DCDC

Table 13: DC Electrical Characteristics

6 Thermal Specification

Description	Min	Typ	Max	Unit
Operating temperature i.MX6 (“C-Temp”)	0		+70[1]	°C
Operating temperature i.MX6 (“I-Temp”)[2]	-20		+85[1]	°C
Junction temperature i.MX6 (“C-Temp”)	-20		+105	°C
Junction temperature i.MX6 (“I-Temp”)[2]	-20		+105	°C
Junction to Package Top of i.MX6 (Psi-JT)[3]		2		°C/W

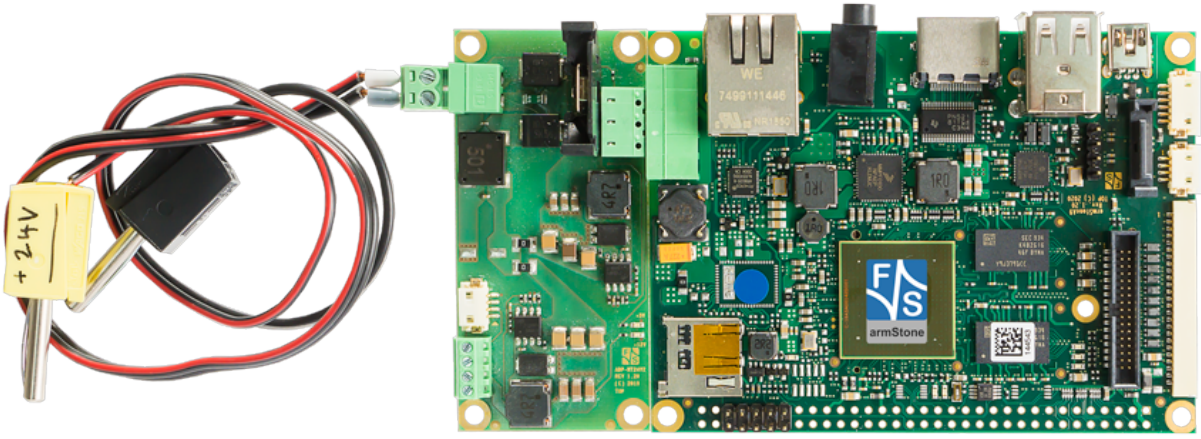
[1] Depending on cooling solution. See also: *Power consumption and cooling*

[2] Optional

[3] Temperature difference between package top and the junction temperature per JEDEC JESD51-2.

7 ADP-NT24V2

To power the armStoneA9 with 7,5-36V F&S provide ADP-NT24V2:



The extension board is designed to plug it into the power Connector of the armStone.
For more information check the F&S website:
https://www.fs-net.de/de/produkte/zubehoer/power-adapter-2/

8 Review service

F&S provide a schematic review service for your baseboard implementation. Please send your schematic as searchable PDF to support@fs-net.de.

9 Second source rules

F&S qualifies their second sources for parts autonomously, as long as this does not touch the technical characteristics of the product. This is necessary to guarantee delivery times and product life. A setup of release samples with released second sources is not possible.

F&S does not use broker components without the consent of the customer.

10 Power consumption and cooling

Depend you product version you will have different temperature range and power consumption of the module.

The operating temperature can be measured on the mounting holes on top of the module and **shouldn't exceed the maximum operating temperature of the board** (85°C).

The maximum power consumption of the board could be **t.b.d.** Watt. This value is with 100% working of cores and full working graphic engines. Calculating with this scenario does need an expensive cooling.

Depend your application and your worst case scenario the maximum power consumption is much lower. This will save money on your cooling solution. We recommend to measure this with your application. We see values between max. **t.b.d.** and **t.b.d.** Watt on different custom applications.

Because the different environments for air temperature, airflow, thermal radiation, power consumption of the board on your application and the power consumption of other components like power supply and LCD inside the system you have to calculate a working cooling solution for the board.

Just cooling the CPU with 70-90% of the power consumption of the entire board is the best way to cool the board.

To calculate your cooling we recommend this helpful literature and the CPU datasheet

- AN4579 from NXP: Thermal management guidelines
- fischerelektronik.de/web_fisch…eKataloge/Heatsinks/#/18/
- http://www.eetimes.com/document.asp?doc_id=1276748
- http://www.eetimes.com/document.asp?doc_id=1276750

11 Storage conditions

Maximum storage on room temperature with non-condensing humidity: 6 months
Maximum storage on controlled conditions 25 ±5 °C, max. 60% humidity: 12 months
For longer storage we recommend vacuum dry packs.

12 ROHS and REACH statement

All F&S designs are created from lead-free components and are completely ROHS compliant.

The products we supply do not contain any substance on the latest candidate list published by the European Chemicals Agency according to Article 59(1,10) of Regulation (EC) 1907/2006 (REACH) in a concentration above 0.1 mass %.
Consequently, the obligations in No. 1 and 2 paragraphs in Annex are not relevant here.
Please understand that F&S is not performing any chemical analysis on its products to testify REACH compliance and is therefore not able to fill out any detailed inquiry forms.

13 Packaging

All F&S ESD-sensitive products are shipped either in trays or bags.
The modules are shipped in trays. One tray can hold 20 boards. An empty tray is used as top cover.

14 Matrix Code Sticker

All F&S hardware is shipped with a matrix code sticker including the serial number. Enter your serial number here https://www.fs-net.de/en/support/serial-number-info-and-rma/ to get information on shipping date and type of board.

Figure 9: Matrix Code Sticker

15 Appendix

Important Notice

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