DATA MODUL

SPECIFICATION

DM3S4G18AB2-SEMAY
4GB DDR3 1866MHz SODIMM I-Temp
K4B4G1646E-BMMA

DDR3- 1866, 4Gb (512*8), PCB: KO8096

Version: 1.0
Date: 09.11.2020

Note: This specification is subject to change without prior notice

DATA MODUL

Nomenclature for Data Modul DIMMs

max lenght of P/N 18 digits

DM	4	S	4G	266	B	6	-	ND	HR	I

DM

DM-	:	Data Modul

Technology

0	:	SDR SDRAM
1	:	DDR SDRAM
2	:	DDR2 SDRAM
3	:	DDR3 SDRAM
4	:	DDR4 SDRAM
5	:	DDR5 SDRAM

Module Type

A	:	ECC DIMM (x72)
D	:	DIMM non ECC unbuffered
E	:	ECC SO-DIMM (x72)
F	:	fully buffered DIMM
L	:	LR DIMM (load reduced)
Q	:	ECC RDIMM
R	:	registered DIMM
S	:	SO-DIMM unbuffered
U	:	VLP DIMM non ECC unbuffered
V	:	VLP RDIMM
W	:	VLP ECC DIMM
O	:	others

Density

128	:	128 MB
256	:	256 MB
512	:	512 MB
1G	:	1 GB
2G	:	2 GB
4G	:	4 GB
8G	:	8 GB
16G	:	16 GB
32G	:	32 GB

Speed / Performance

x: PCB option

013	:	SDR PC 133
020	:	SDR PC 200
333	:	DDR1 300
400	:	DDR1 400
667 / 66x	:	DDR2 667
800 / 80x	:	DDR2 800
106 / 10x	:	DDR3 1066
133 / 13x	:	DDR3 1333
160 / 16x	:	DDR3 1600
186 / 18x	:	DDR3 1866
213 / 21x	:	DDR4 2133
240 / 24x	:	DDR4 2400
266 / 26x	:	DDR4 2666
293 / 29x	:	DDR4 2933
320 / 32x	:	DDR4 3200

Component Organisation

A	:	x4
B	:	x8
C	:	x16
D	:	other organisations

Number of Components

1	:	4 Chips
2	:	8 Chips
3	:	16 Chips
4	:	32 Chips
6	:	9 Chips
7	:	18 Chips
8	:	36 Chips

Separator btw Product and Componet Manufacturer Data

Component Mfr. Die Rev.

M	:	Micron
H	:	SK Hynix
N	:	Nanya
S	:	Samsung
E	:	Etron
W	:	Winbond

Speed / Performance of Component (as metioned on the DRAM)

Special Fuctions

Blank	:	not specified
I	:	industrial temperature
Y	:	low power & extended temperature
L	:	low power

09.11.2020 DMAR

Description

Data Modul Unbuffered Small Outline DDR3L SDRAM DIMMs (Unbuffered Small Outline Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR3L SDRAM devices. These Unbuffered DDR3L SDRAM SODIMMs are intended for use as main memory when installed in systems such as mobile personal computers.

Features

- Power Supply: VDD=±1.35V (1.283V to 1.45V)
- VDDQ=+1.35V (1.283V to 1.45V)
- VDDSPD=3.0V to 3.6V
- Backward compatible with 1.5V DDR3 Memory Module
- 8 internal banks
- Data transfer rates: PC3-10600, PC3-12800, PC3-14900
- Programmable CAS Latency: 6, 7, 8, 9, 10, 11, 13
- Programmable /CAS Write Latency (CWL) =5, 6, 7, 8, 9
- Bi-directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly: BL 8 or BC (Burst Chop) 4
- On Die Termination (ODT) supported
- This product is in Compliance with the RoHS directive
- Internal calibration through ZQ pin
- Asynchronous reset

Symbol	Parameter	Rating	Units
T_{OPR}	Operating temperature (ambient)	-40 to 95	°C
H_{OPR}	Operating humidity (relative)	10 to 90	%

		Rating	
T_{OPER}	Normal Operating Temperature Range	-40 to 95	°C
	Extended Temperature Range	85 to 95	

Pin Configurations

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	$V_{REF}DQ$	2	V_{SS}	53	DQ19	54	V_{SS}	105	V_{DD}	106	V_{DD}	157	DQ42	158	DQ46
3	V_{SS}	4	DQ4	55	V_{SS}	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{RAS}$	161	V_{SS}	162	V_{SS}
7	DQ1	8	V_{SS}	59	DQ25	60	V_{SS}	111	V_{DD}	112	V_{DD}	163	DQ48	164	DQ52
9	V_{SS}	10	$\overline{DQS0}$	61	V_{SS}	62	$\overline{DQS3}$	113	$\overline{WE}$	114	$\overline{S0}$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{CAS}$	116	ODT0	167	V_{SS}	168	V_{SS}
13	V_{SS}	14	V_{SS}	65	V_{SS}	66	V_{SS}	117	V_{DD}	118	V_{DD}	169	$\overline{DQS6}$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13[2]	120	ODT1	171	DQS6	172	V_{SS}
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{S1}$	122	NC	173	V_{SS}	174	DQ54
19	V_{SS}	20	V_{SS}	71	V_{SS}	72	V_{SS}	123	V_{DD}	124	V_{DD}	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	$V_{REF}CA$	177	DQ51	178	V_{SS}
23	DQ9	24	DQ13	75	V_{DD}	76	V_{DD}	127	V_{SS}	128	V_{SS}	179	V_{SS}	180	DQ60
25	V_{SS}	26	V_{SS}	77	NC	78	A15[2]	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{DQS1}$	28	DM1	79	BA2	80	A14[2]	131	DQ33	132	DQ37	183	DQ57	184	V_{SS}
29	DQS1	30	$\overline{RESET}$	81	V_{DD}	82	V_{DD}	133	V_{SS}	134	V_{SS}	185	V_{SS}	186	$\overline{DQS7}$
31	V_{SS}	32	V_{SS}	83	A12/$\overline{BC}$	84	A11	135	$\overline{DQS4}$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V_{SS}	189	V_{SS}	190	V_{SS}
35	DQ11	36	DQ15	87	V_{DD}	88	V_{DD}	139	V_{SS}	140	DQ38	191	DQ58	192	DQ62
37	V_{SS}	38	V_{SS}	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V_{SS}	195	V_{SS}	196	V_{SS}
41	DQ17	42	DQ21	93	V_{DD}	94	V_{DD}	145	V_{SS}	146	DQ44	197	SA0	198	$\overline{EVENT}$
43	V_{SS}	44	V_{SS}	95	A3	96	A2	147	DQ40	148	DQ45	199	VDD_{SPD}	200	SDA
45	$\overline{DQS2}$	46	DM2	97	A1	98	A0	149	DQ41	150	V_{SS}	201	SA1	202	SCL
47	DQS2	48	V_{SS}	99	V_{DD}	100	V_{DD}	151	V_{SS}	152	$\overline{DQS5}$	203	V_{TT}	204	V_{TT}
49	V_{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{CK0}$	104	$\overline{CK1}$	155	V_{SS}	156	V_{SS}				

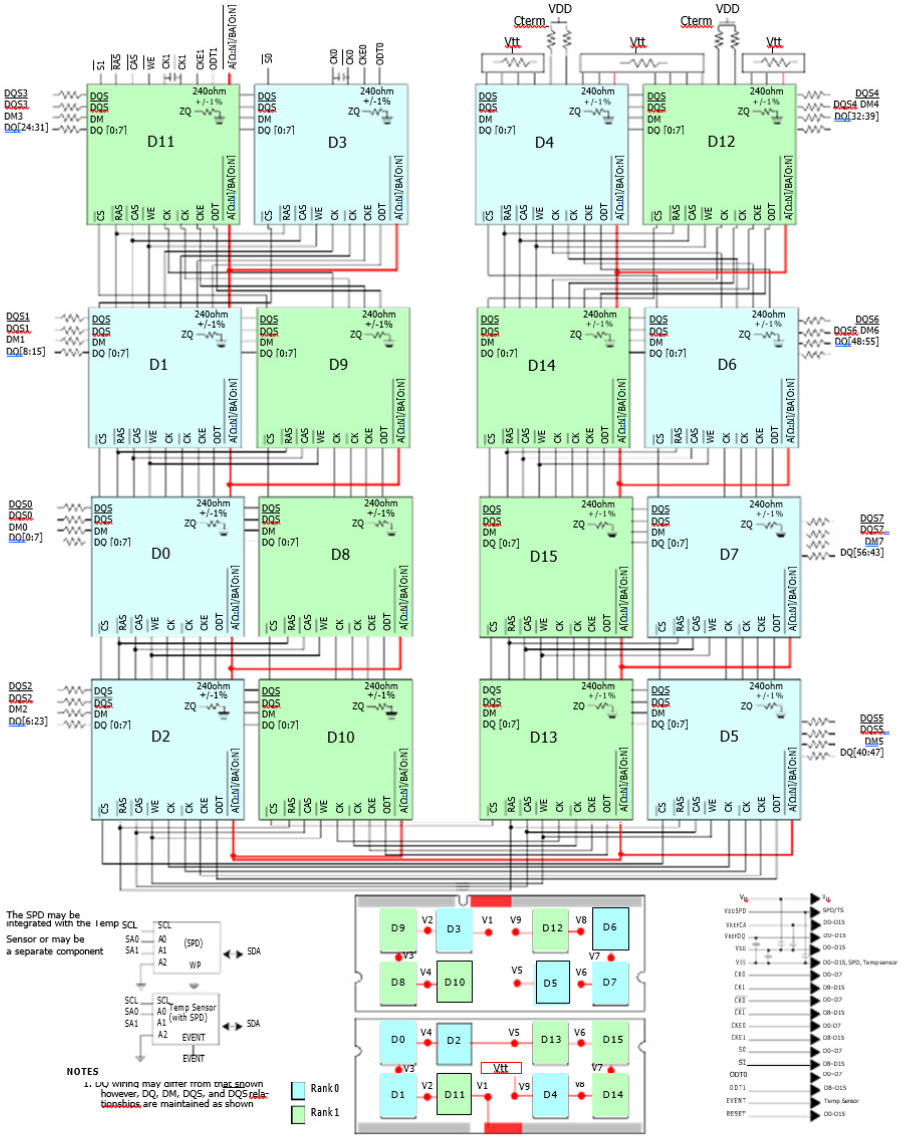
NC = No Connect; RFU = Reserved Future Use

1. TEST (pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
2. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

Pin Description

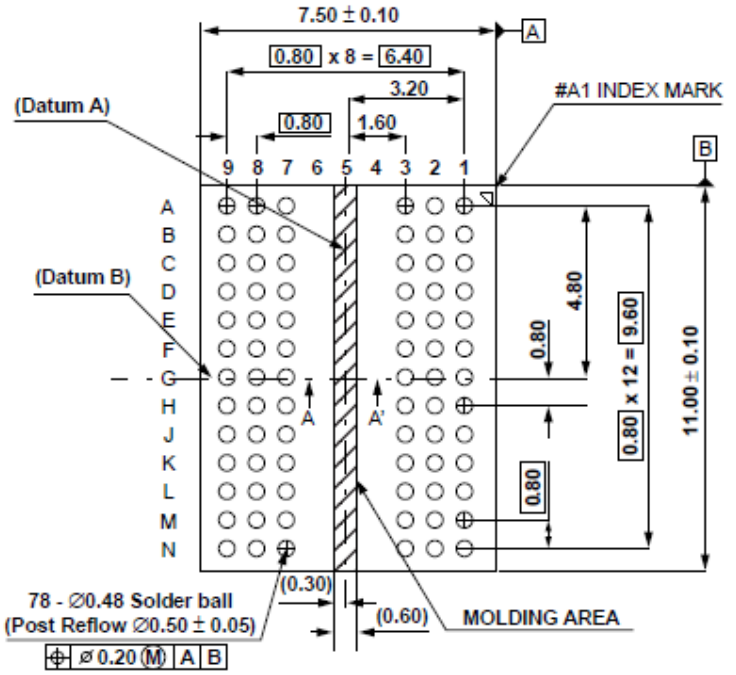
Pin Name	Description	Number	Pin Name	Description	Number
CK[1:0]	Clock Input, positive line	2	DQ[63:0]	Data Input/Output	64
$\overline{CK}$[1:0]	Clock Input, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS}$[7:0]	Data strobes, negative line	8
$\overline{CAS}$	Column Address Strobe	1	$\overline{EVENT}$	Temperature event pin	1
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{S}$[1:0]	Chip Selects	2	$\overline{RESET}$	Reset Pin	1
A[9:0],A11, A[15:13]	Address Inputs	14	V_{DD}	Core and I/O Power	18
A10/AP	Address Input/Autoprecharge	1	V_{SS}	Ground	52
A12/$\overline{BC}$	Address Input/Burst chop	1			
BA[2:0]	SDRAM Bank Addresses	3	V_{REFDQ}	Input/Output Reference	1
ODT[1:0]	On Die Termination Inputs	2	V_{REFCA}		1
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{TT}	Termination Voltage	2
SDA	SPD Data Input/Output	1	V_{DDSPD}	SPD Power	1
SA[1:0]	SPD Address Inputs	2	NC	Reserved for future use	2
				Total:	**204**

Functional Diagram

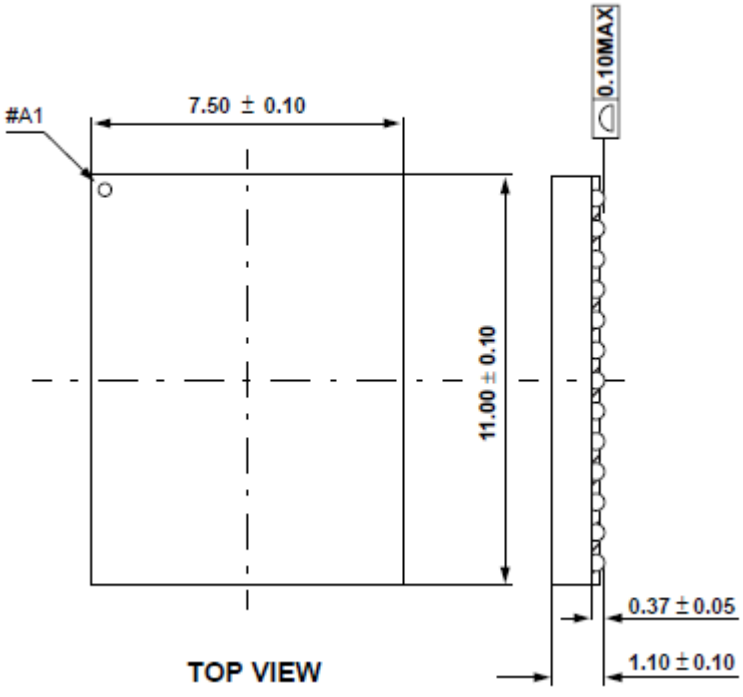


Package Dimension

Units : Millimeters

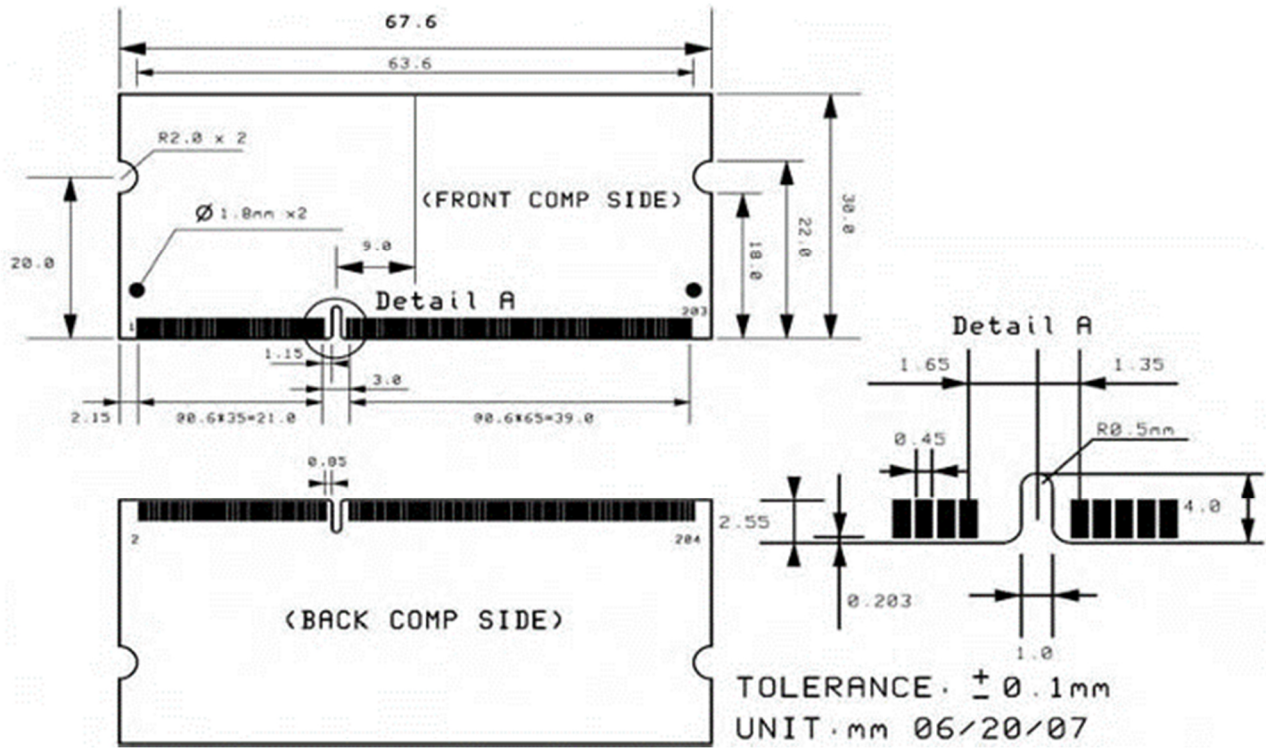


BOTTOM VIEW



TOP VIEW

PCB Panelization



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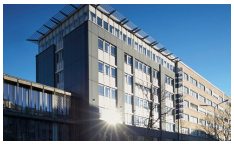

DATA MODUL AG

Landsberger Straße 322
DE-80687 Munich
Phone: +49-89-56017-0

DATA MODUL WEIKERSHEIM GMBH

Lindenstraße 8
DE-97990 Weikersheim
Phone: +49-7934-101-0

More information and worldwide locations can be found at

www.data-modul.com